Integrated
Circuit
Systems, Inc.

ICS9159C-02

Frequency Generator and Integrated Buffer for PENTIUM™

General Description

The **ICS9159C-02** generates all clocks required for high speed RISC or CISC microprocessor systems such as 486, Pentium, PowerPC,™ etc. Four different reference frequency multiplying factors are externally selectable with smooth frequency transitions. These multiplying factors can be customized for specific applications. A test mode is provided to drive all clocks directly.

High drive BCLK outputs provide typically greater than 1V/ns slew rate into 30pF loads. PCLK outputs provide typically better than 1V/ns slew rate into 20pF loads while maintaining +/–5% duty cycle.

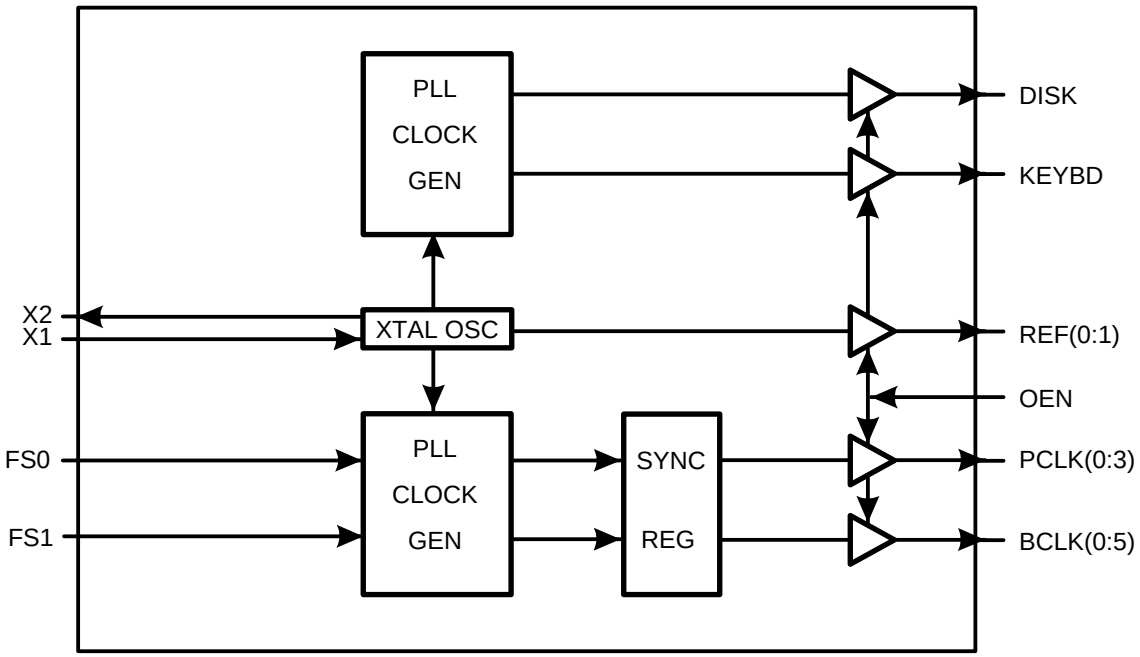
Features

- Generates up to four processor and six bus clocks, plus disk, keyboard and reference clocks
- Synchronous clocks skew matched to 250ps window on PCLKs and 500ps window on BCLKs
- Test clock mode eases system design
- Custom configurations available:
  Output frequency ranges to 100 MHz on options
  Selectable multiplying and processor/bus ratios
  Stop clock control stops clock glitch-free; available as mask option
- 3.0V - 5.5V supply range
- 28-pin SOIC package

Applications

- Ideal for high-speed RISC or CISC systems such as 486, Pentium, PowerPC, etc.

Block Diagram



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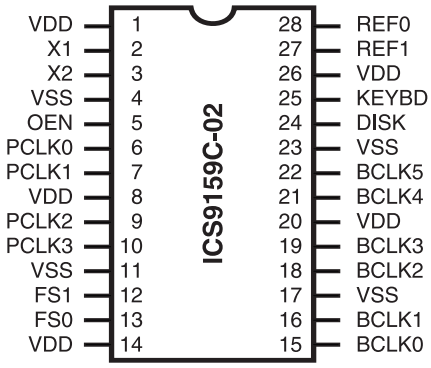
PowerPC is a trademark of Motorola Corporation

Pin Configuration



28-Pin SOIC

Functionality

FS1	FS0	*VCO	X1, REF (MHz)	CPU (MHz)
0	0	118/17xX1	14.318	50(49.7)
0	1	65/7xX1	14.318	66.6(66.5)
1	0	92/11xX1	14.318	60(59.9)
1	1	Test mode	TCLK	TCLK/2

*VCO range is limited from 60 - 200 MHz

PCLK(0,3)	BCLK(0,5)	DISK	KEYBD
VCO/2	PCLK/2	24 MHz	12 MHz
TCLK/2	TCLK/4	TCLK/4	TCLK/8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 8, 14, 20, 26	VDD	PWR	Power for logic, PCLK and fixed frequency output buffers.
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz crystal, nominally 14.31818 MHz.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
4, 11, 17, 23	VSS	PWR	Ground for logic, PCLK and fixed frequency output buffers.
6, 7, 9, 10	PCLK(0:3)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.
13, 12	FS(0:1)	IN	Frequency multiplier select pins. See table above. These inputs have internal pull-up devices.
15, 16, 18 19, 21, 22	BCLK(0:5)	OUT	Bus clock outputs are fixed at one half the PCLK frequency.
5	OEN	IN	OEN tristates all outputs when low. This input has an internal pull-up device.
24	DISK	OUT	The DISK controller clock is fixed at 24 MHz (with 14.318 MHz input).
25	KEYBD	OUT	The KEYBD clock is fixed at 12 MHz (with 14.318 MHz input).
28, 27	REF(0:1)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock nominally 14.31818 MHz.

Note: BCLK buffers cannot be supplied with 5 volts (pins 14 and 20) if CPU and fixed frequencies (pins 1, 8, and 26) are being supplied with 3.3 volts

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND - 0.5 V to VDD + 0.5 V

Ambient ..... Operating Temperature 0 to +70 C

Storage Temperature ..... 65 to +150 C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stess specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3 V

V_{DD} = 3.0 - 3.7 V, T_A = 0 - 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	0.2V_{DD}	V
Input High Voltage	V_{IH}		0.7V_{DD}	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-28.0	-10.5	-	mA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0	-	5.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V for PCLKS & BCLKS	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	VOL=2.0V for PCLKS & BCLKS	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	VOL=0.8V for fixed CLKs	25.0	38.0	-	mA
Output High Current[1]	I_{OH}	VOL=2.0V for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA for PCLKS & BCLKS	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA for PCLKS & BCLKS	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=12.5mA for fixed CLKs	-	0.3	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-20mA for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@66.5 MHz all outputs unloaded	-	55	110	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3 V

V_{DD} = 3.0 - 3.7 V, T_A = 0 - 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	Tr1	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.9	1.5	ns
Fall Time[1]	Tf1	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.8	1.4	ns
Rise Time[1]	Tr2	20pF load, 20% to 80% PCLK & BCLK	-	1.5	2.5	ns
Fall Time[1]	Tf2	20pF load, 80% to 20% PCLK & BCLK	-	1.4	2.4	ns
Duty Cycle[1]	Dt	20pF load @ VOUT=1.4V	45	50	55	%
Jitter, One Sigma[1]	Tj1s1	PCLK & BCLK Clocks; Load=20pF, FOUT>25 MHz	-	50	150	ps
Jitter, Absolute[1]	Tjab1	PCLK & BCLK Clocks; Load=20pF, FOUT >25 MHz	-250	-	250	ps
Jitter, One Sigma[1]	Tj1s2	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	Tjab2	Fixed CLK; Load=20pF	-5	2	5	%
Input Frequency[1]	Fi		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	CIN	Logic input pins	-	5	-	pF
Crystal Oscillator[1] Capacitance1	CINX	X1, X2 pins	-	18	-	pF
Power-on Time[1]	ton	From VDD=1.6V to 1st crossing of 66.5 MHz VDD supply ramp<40ms	-	2.5	4.5	ms
Frequency Settling Time[1]	ts	From 1st crossing of acquisition to <1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	Tsk1	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window	Tsk2	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	Tsk3	PCLK to BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0 V

V_{DD} = 4.5 - 5.5 V, T_A = 0 - 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL		-	-	0.8	V
Input High Voltage	VIH		2.4	-	-	V
Input Low Current	IIL	VIN=0V	-45	-15	-	mA
Input High Current	IIH	VIN=VDD	-5.0	-	5.0	mA
Output Low Current[1]	IOL	VOL=0.8V; for PCLKS & BCLKS	36.0	62.0	-	mA
Output High Current[1]	IOH	VOH=2.0V; for PCLKS & BCLKS	-	-152	-90.0	mA
Output Low Current[1]	IOL	VOL=0.8V; for fixed CLKs	30.0	50.0	-	mA
Output High Current[1]	IOH	VOL=2.0V; for fixed CLKs	-	-110.0	-65.0	mA
Output Low Voltage[1]	VOL	IOL=20mA; for PCLKS & BCLKS	-	0.25	0.4	V
Output High Voltage[1]	VOH	IOH=-70mA; for PCLKS & BCLKS	2.4	4.0	-	V
Output Low Voltage[1]	VOL	IOL=15mA; for fixed CLKs	-	0.2	0.4	V
Output High Voltage[1]	VOH	IOH=-50mA; for fixed CLKs	2.4	4.7	-	V
Supply Current	IDD	@66.5 MHz; all outputs unloaded	-	80.0	160.0	mA

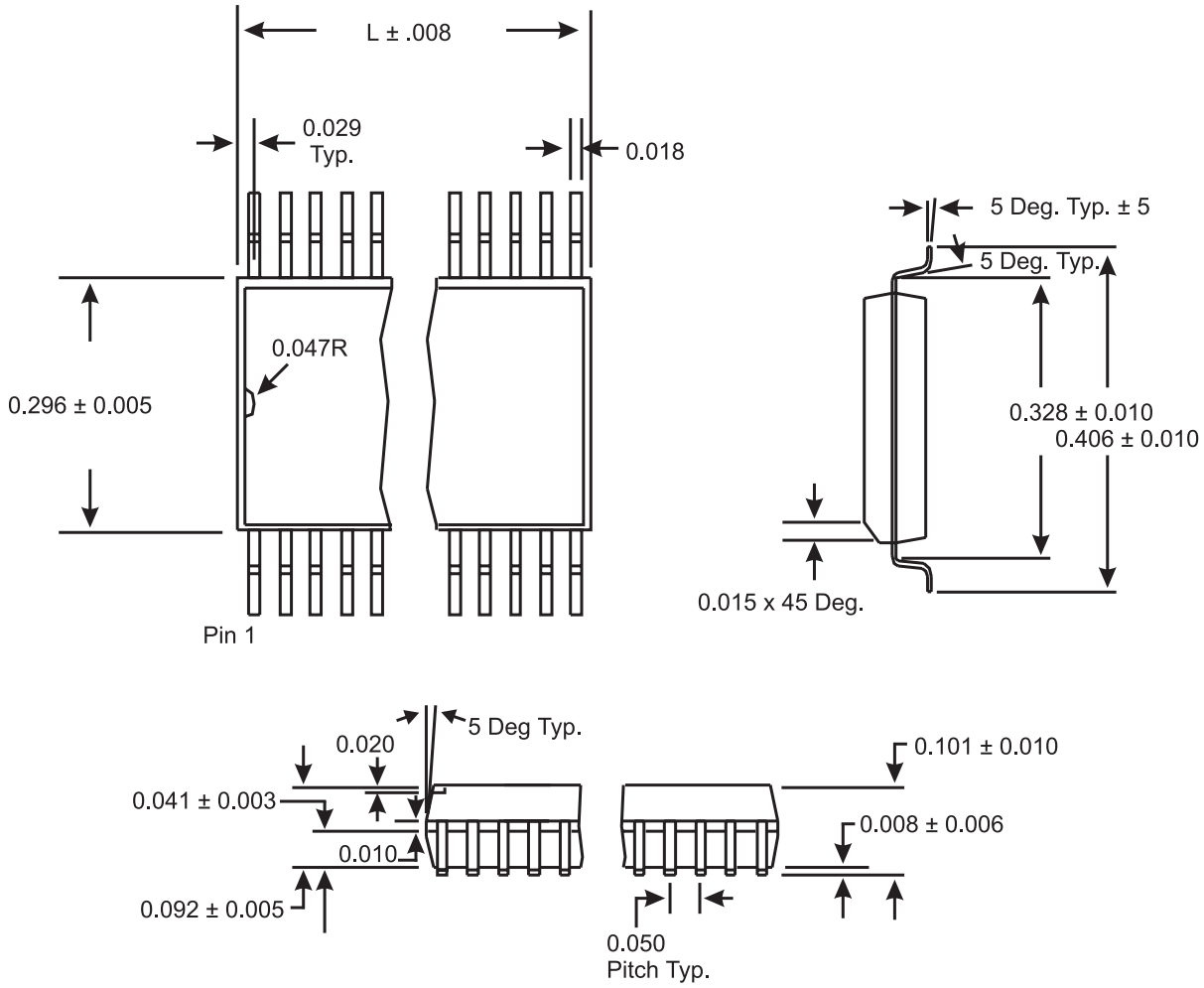
Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 5.0 V

V_{DD} = 4.5 - 5.5 V, T_A = 0 - 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	Tr1	20pF load, 0.8 to 2.0V PCLK & BCLK	-	0.55	0.95	ns
Fall Time[1]	Tf1	20pF load, 2.0 to 0.8V PCLK & BCLK	-	0.52	0.90	ns
Rise Time[1]	Tr2	20pF load, 20% to 80% PCLK & BCLK	-	1.2	2.1	ns
Fall Time[1]	Tf2	20pF load, 80% to 20% PCLK & BCLK	-	1.1	2.0	ns
Duty Cycle[1]	Dt	20pF load @ VOUT=50%	45	50	55	%
Duty Cycle[1]	Dt2	20pF load @ VOUT=1.4V				%
Jitter, One Sigma[1]	Tj1s1	PCLK & BCLK Clocks; Load=20pF, RS=33 FOUT>25 MHz	-	50	150	ps
Jitter, Absolute[1]	Tjab1	PCLK & BCLK Clocks; Load=20pF, RS=33 FOUT>25 MHz	-250	-	250	ps
Jitter, One Sigma[1]	Tj1s2	Fixed CLK; Load=20pF RS=33	-	1	3	%
Jitter, Absolute[1]	Tjab2	Fixed CLK; Load=20pF RS=33	-5	2	5	%
Input Frequency[1]	Fi		12.0	14.318	16.0	MHz
Logic Input Capacitance[1]	CIN	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance1	CINX	X1, X2 pins	-	18	-	pF
Power-on Time[1]	ton	From VDD=1.6V to 1st crossing of 66.5 MHz VDD supply ramp<40ms	-	2.5	4.5	ms
Frequency Settling Time[1]	ts	From 1st crossing of acquisition to <1% settling	-	2.0	4.0	ms
Clock Skew Window[1]	Tsk1	PCLK to PCLK; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	Tsk2	BCLK to BCLK; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	Tsk3	PCLK to BCLK; Load=20pF; @1.4V	1	2.6	5	ns

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.



SOIC Package

Ordering Information

ICS9159C-02CW28

Example:

ICS XXXX - PPP XX ##

Lead Count
Lead Count=1,2 or 3 digits

Package Type
CW = 0.3" Body SOIC, CS = 0.15 Body SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type
(consists of 3 or 4 digit numbers and one alpha code on some parts.)

Prefix
ICS, AV=Standard Device; GSP=Genlock device