Integrated
Circuit
Systems, Inc.

ICS9159-05

Frequency Generator for Pentium™/OPTi VIPER Systems

General Description

The **ICS9159-05** is a low cost frequency generator designed specifically for Pentium/Pentium Pro systems. The integrated buffer minimizes skew and provides the early CPU clock required by some chipsets such as the OPTi VIPER. A 14.318 MHz XTAL oscillator provides the reference clock to generate standard Pentium frequencies. The CPU clock makes gradual frequency transitions without violating the PLL timing of internal micro-processor clock multipliers.

The synchronous bus frequencies are selectable as CPU for local bus or CPU/2 for PCI bus support. Green PC systems are supported through power-down, doze, and glitch-free stop clock modes.

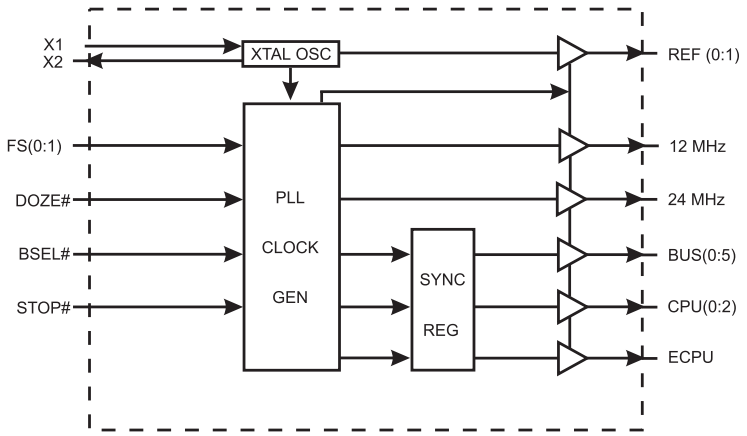
Features

- Four CPU clocks operate up to 66.6 MHz at 3.3V with glitch-free start and stop plus smooth transitions
- 3-6ns early CPU clock supports OPTi VIPER systems
- Selection of 6 frequencies, tristate, or power-down
- Six BUS clocks support local PCI bus operation
- Skew window between synchronous outputs
- Integrated buffer outputs drive up to 30pF loads
- 3.0V - 3.7V supply range
- 28-pin DIP or 28-pin 300-mil SOIC package

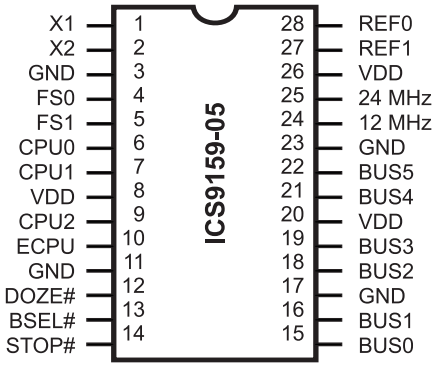
Applications

- Ideal for green Pentium/Pentium Pro and 486 PCI systems such as Pentium, PowerPC™ etc.

Block Diagram



Pin Configuration



28-Pin 300-mil SOIC

Pentium is a trademark of Intel Corporaton.
PowerPC is a trademark of Motorola Corporation.

Functionality

Assuming 14.318 MHz input, all frequencies in MHz. 14 MHz=14.318 MHz

STOP#	BSEL#	DOZE#	FS0	FS1	CPU (0:2) (MHz)	ECPU (MHz)	BUS (0:5) (MHz)	FIXED (MHz)
1	0	1	X	X	F	F	F	24, 12, 14
1	1	1	X	X	F	F	F	24, 12, 14
1	0	0	X	X	F/2	F/2	F/4	24, 12, 14
1	1	0	X	X	F/2	F/2	F/2	24, 12, 14
0	1	1	Select	Select	Stop	Run	Run	24, 12, 14
0	0	1	X	X	Stop	Stop	Stop	24, 12, 14
0	0	0	X	X	Low	Low	Low	L, L, 14
0	1	0	X	X	Tristate	Tristate	Tristate	Tristate

Notes:
1. Where F is Frequency selected by FS (0:1)
2. F value is 66.6, 60, 50 or 33.3.

STOP#	BSEL#	DOZE#	FS0	FS1	CPU (0:2) (MHz)	ECPU (MHz)	BUS (0:5) (MHz)	FIXED (MHz)
1	0	1	0	0	66.6	66.6	33.3	24, 12, 14
1	0	1	0	1	60	60	30	24, 12, 14
1	0	1	1	0	50	50	25	24, 12, 14
1	0	1	1	1	33.3	33.3	16.7	24, 12, 14
1	1	1	0	0	66.6	66.6	66.6	24, 12, 14
1	1	1	0	1	60	60	60	24, 12, 14
1	1	1	1	0	50	50	50	24, 12, 14
1	1	1	1	1	33.3	33.3	33.3	24, 12, 14
1	0	0	0	0	33.3	33.3	16.7	24, 12, 14
1	0	0	0	1	30	30	15	24, 12, 14
1	0	0	1	0	25	25	12.5	24, 12, 14
1	0	0	1	1	16.7	16.7	8.3	24, 12, 14
1	1	0	0	0	33.3	33.3	33.3	24, 12, 14
1	1	0	0	1	30	30	30	24, 12, 14
1	1	0	1	0	25	25	25	24, 12, 14
1	1	0	1	1	16.7	16.7	16.7	24, 12, 14
1	1	1	Select[2]	Select[2]	F[3]	F[3]	F[3]	24, 12, 14
1	1	0	Select[2]	Select[2]	F/2	F/2	F/2	24, 12, 14
0	1	1	Select[2]	Select[2]	Stop	Run	Run	24, 12, 14
0	0	1	X	X	Stop	Stop	Stop	L, L, 14
0[1]	0[1]	0[1]	X	X	Low	Low	Low	L, L, 14
0	1	0	X	X	Tristate	Tristate	Tristate	Tristate

Notes:
1. 000 mode powers-down the PLL sections and forces the outputs low. To ensure glitch-free start and stop of the CPU and BUS clocks, enter 000 from 001 and exit 000 through 001.
2. Select is FS0, Fs1 = 00, 01, 10, 11.
3. F is the value of CPU, ECPU & BUS. F value is 66.6, 60, 50 or 33.3 as selected by FS(0:1).

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
8, 20, 26	VDD	PWR	Power for logic, CPU and fixed frequency output buffers.
1	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 4-20 MHz XTAL, normally 14.318 MHz.
2	X2	OUT	XTAL output which includes XTAL load capacitance.
3, 11, 23, 17	GND	PWR	Ground for logic, CPU and fixed frequency output buffers.
6, 7, 9	CPU(0:2)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table.
4, 5	FS(0:1)	IN	Frequency multiplier select pins. See table below. These inputs have internal pull-up devices.
10	ECPU	OUT	Early CPU clock. Transition precedes CPU clocks.
15, 16, 18, 19,21, 22	BUS(0:5)	OUT	Bus clock outputs are fixed at 1/2 the PCLK frequency.
12	DOZE#[1]	IN	Doze mode control. Reduces CPU and BUS clock frequencies by 1/2 when low.
13	BSEL#[1]	IN	BUS select for BSEL = 0, BUS = CPU/2 for BSEL = 1, BUS = CPU
14	STOP#[1]		Stop Clock. Stops all CPU clock outputs and forces them to a logic low level synchronously with their next low level transition.
24	KEYBD	OUT	12 MHz fixed clock (with 14.318 MHz input).
25	DISK	OUT	24 MHz fixed clock (with 14.318 MHz input).
27, 28	REF (0:1)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Note:
1. Internally pulled-up

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-25.0	-5	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0	-	5.0	µA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for CPU & BUS	30.0	47.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for CPU & BUS	-	-66.0	-42.0	mA
Output Low Current[1]	I_{OL}	V_{OL}=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current[1]	I_{OH}	V_{OL}=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage[1]	V_{OL}	I_{OL}=15mA; for CPU & BUS	-	0.30	.4	V
Output High Voltage[1]	V_{OH}	I_{OH}=-30mA; for CPU & BUS	2.4	2.8	-	V
Output Low Voltage[1]	V_{OL}	I_{OL}=12.5mA; for fixed CLKs	-	0.30	.4	
Output High Voltage[1]	V_{OH}	I_{OH}=-20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@ 66.6 MHz; all outputs unloaded	-	55	110	mA
	I_{DDPD}	@ 000 mode (power-down)		8	20	a
	I_{DDS}	@ 001 mode (stop)		35	70	a

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	T_{r1}	20pF load, 0.8 to 2.0V CPU & BUS	-	0.9	1.5	ns
Fall Time[1]	T_{f1}	20pF load, 2.0 to 0.8V CPU & BUS	-	0.8	1.4	ns
Rise Time[1]	T_{r2}	20pF load, 20% to 80% CPU & BUS	-	1.5	2.5	ns
Fall Time[1]	T_{f2}	20pF load, 80% to 20% CPU & BUS	-	1.4	2.4	ns
Duty Cycle[1]	D_t	20pF load @ V_{OUT}=1.4V	45	50	55	%
Jitter, One Sigma[1]	T_{j1s1}	CPU & BUS Clocks; Load=20pF, Rs=33Ω	-	40	150	ps
Jitter, Absolute[1]	T_{jab1}	CPU & BUS Clocks; Load=20pF, Rs=33Ω	-300	-	300	ps
Jitter, One Sigma[1]	T_{j1s2}	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	T_{jab2}	Fixed CLK; Load=20pF	-	2	5	%
Input Frequency[1]	F_i		4.0	14.318	20.0	MHz
Logic Input Capacitance[1]	C_{IN}	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1]	C_{INX}	X1, X2 pins	-	18	-	pF
Clock Skew Window[1]	T_{sk1}	CPU to CPU; Load=20pF; @1.4V	-	150	250	ps
Clock Skew Window[1]	T_{sk}	BUS to BUS; Load=20pF @1.4V	-	300	500	ps
Clock Skew Window[1]	T_{sk3}	ECPU to CPU; Load=20pF; @1.4V	3.0	-	6.0	ns
Clock Skew Window[1]	T_{SR4}	CPU to BUS; Load=20pF; @1.4v	0.5	1.0	3.0	ns

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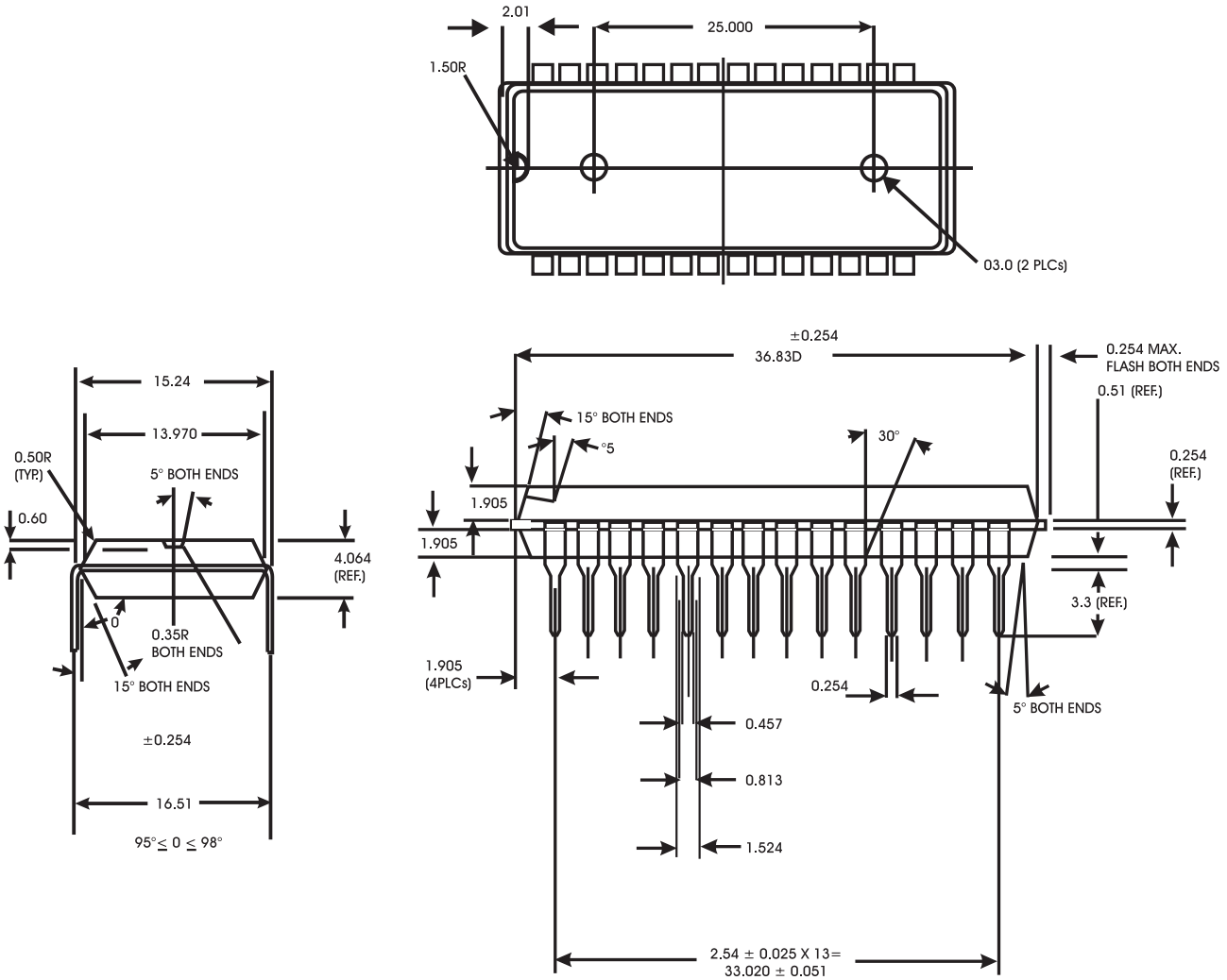


28-Pin DIP Package

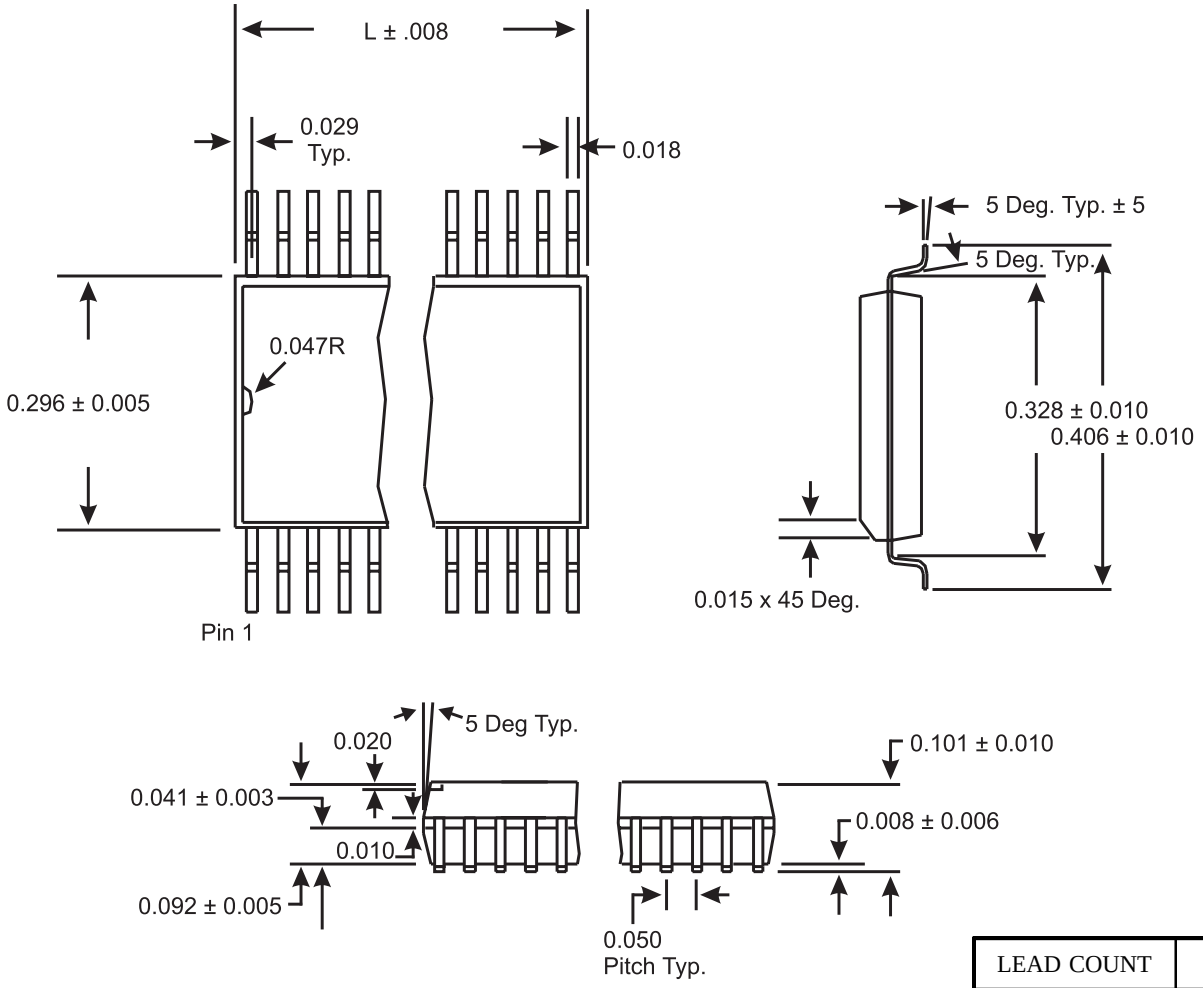
Ordering Information

ICS9159N-05

Example:

ICS XXXX N-PPP

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  N=DIP (Plastic)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS=Standard Device



LEAD COUNT	28L
DIMENSIONL	0.704

SOIC Package

Ordering Information

ICS9159M-05

Example:

ICS XXXX M-PPP

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC, SOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS=Standard Device