Integrated Circuit Systems, Inc.

ICS9148-27

Pentium/Pro™ System Clock Chip

General Description

The **ICS9148-27** is a Clock Synthesizer chip for Pentium and PentiumPro CPU based Desktop/Notebook systems that will provide all necessary clock timing.

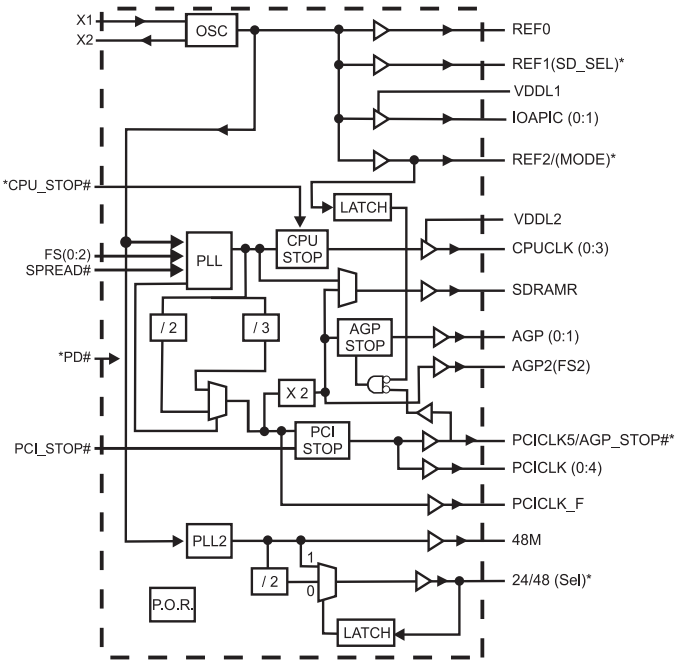
Features include four CPU, seven PCI and three AGP clocks. Three reference outputs are available equal to the crystal frequency. Additionally, the device meets the Pentium power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up.

PD# pin allows low power mode by stopping crystal OSC and PLL stages. For optional power management, CPU_STOP# can stop CPUCLK (0:3), CPUCLKR clock PCI_STOP# will stop PCICLK (0:5). If MODE input is latched low, AGP_STOP# can stop AGP clocks.

High drive CPUCLK and AGP outputs typically provide greater than 1 V/ns slew rate into 20pF loads. PCICLK outputs typically provide better than 1V/ns slew rate into 30pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

The **ICS9148-27** accepts a 14.318MHz reference crystal or clock as its input and runs on a 3.3V core supply.

Block Diagram

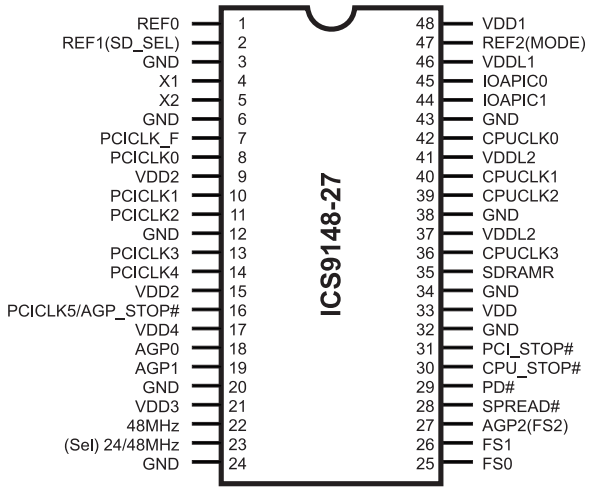


*240K pull-up to VDD on all inputs except FS2 = 240K pull-down to GND.

Features

- Generates system clocks for CPU, AGP, IOAPIC, PCI, plus 14.314 MHz REF (0:2), USB, Plus Super I/O
- Supports single or dual processor systems
- Supports Spread Spectrum Modulation for CPU, AGP & PCI clocks down spread 0/-1%
- Skew from CPU to PCI 1.5±0.5ns, CPU to AGP -500ps AGP to PCI 1.8±0.5ns clock (rising edges for 100/ 33.3MHz) (CPU early)
- Two fixed outputs, one 48MHz, second selectable 24 or 48MHz..
- Separate 2.5V and 3.3V supply pins
- 2.5V or 3.3V output: CPU, IOAPIC
- 3.3V outputs: PCI, REF, 48MHz, AGP, SDRAMR.
- No power supply sequence requirements
- Uses external 14.318MHz crystal, no external load cap required for C_L=18pF crystal
- 48 pin 300 mil SSOP

Pin Configuration



48-Pin SSOP

Power Groups

VDD = Supply for CPU PLL
VDD1 = REF (0:2), X1, X2
VDD2 = PCICLK_F, PCICLK (0:4)
VDD3 = 48MHz, 24/48MHz, Core, PLL2
VDDL1 = IOAPIC (0:1)
VDDL2 = CPUCLK (0:3)
VDD4 = AGP Clocks

Pentium is a trademark on Intel Corporation.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF0	OUT	14.318MHz clock output
2	REF1	OUT	14.318MHz clock output
	SD_SEL	IN	Latched input at power on which selects either CPU or AGP clock for SDRAM reference.
3	GND	PWR	Ground for REF outputs
4	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
5	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
6, 12	GND	PWR	Ground for PCI outputs
7	PCICLK_F	OUT	Free Running PCI output
8, 10, 11, 13, 14	PCICLK (0:4)	OUT	PCI clock outputs. TTL compatible 3.3V
9, 15	VDD2	PWR	Power for PCICLK outputs, nominally 3.3V
16	AGP_STOP#	IN	Input for AGP Stop control, only if MODE input is Latched as a Low (0=MOBILE) mode.
	PCICLK5	OUT	PCI output if MODE=High latched
17	VDD4	PWR	Power for AGP outputs, nominally 3.3V
18, 19, 27	AGP (0:2)	OUT	AGP outputs defined as 2X PCI
33	VDD	PWR	Isolated power for core, nominally 3.3V
20, 32	GND	PWR	Isolated ground for core
21	VDD3	PWR	Power for 48MHz outputs, nominally 3.3V
22	48MHz	OUT	48MHz outputs
23	(SEL) 24/48MHz	OUT	USB or Super IO output selected at power_on by latched input resistor, to GND=24 MHz to VDD=48MHz
24	GND	PWR	Ground for 48MHz outputs
25, 26	FS (0:1)	IN	Frequency Select pins, has pull-up to VDD
27	AGP2	OUT	Free running AGP output
	FS2	IN	Latched input at power on, has pull-down to GND
28	SPREAD#	IN	Enables Spread Spectrum feature when LOW
29	PD#	IN	Powers down chip, active low
30	CPU_STOP#	IN	Halts CPU clocks at logic "0" level when low
31	PCI_STOP#	IN	Halts PCI Bus at logic "0" level when low
35	SDRAMR	OUT	CPU/AGP reference clock for SDRAM zero delay buffer
37, 41	VDDL2	PWR	Power for CPU outputs, nominally 2.5V
34, 38	GND	PWR	Ground for CPU outputs.
36, 39, 40, 42	CPUCLK (3:0)	OUT	CPU and Host clock outputs @ 2.5V
43	GND	PWR	Ground for IOAPIC outputs
44, 45	IOAPIC (1:0)	OUT	IOAPIC outputs (14.318MHz) @ 2.5V
46	VDDL1	PWR	Power for IOAPIC outputs, nominally 2.5V
47	REF2	OUT	14.31818 clock output
	MODE Latch	IN	Latched input at power on for MODE control of PCICLK5/AGP_STOP# pin
48	VDD1	PWR	Power for REF (0:2), X1, X2, nominally 3.3V

Select Functions

Functionality	CPU	SDRAMR	AGP	PCI, PCI_F	REF	IOAPIC	48 MHz Selection	24MHz Selection
Tristate	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z
Testmode	TCLK/2[1]	TCLK/2 or 3[1,4]	TCLK/3	TCLK/6[1]	TCLK[1]	TCLK[1]	TCLK/2[1]	TCLK/4[1]
Spread Spectrum	Modulated[2]	Modulated[2]	Modulated[2]	Modulated[2]	14.318MHz	14.318MHz	48.0MHz	24MHz

Frequency Select[3]

FS2	FS1	FS0	CPU	SDRAM		AGP	PCI
				= 1	= 0		
0	0	0	Tristate	Tristate	Tristate	Tristate	Tristate
0	0	1	100	100	66.6	66.6	33.3
0	1	0	68.5	68.5	68.5	68.5	34.25
0*	1*	1*	66.6	66.6	66.6	66.6	33.3
1	0	0	TCLK/2	TCLK/2	TCLK/3	TCLK/3	TCLK/6
1	0	1	95.25	95.25	63.5	63.5	31.75
1	1	0	83	83	55.4	55.4	27.7
1	1	1	75	75	75	75	37.5

Notes:

1. TCLK is a test clock driven on the X1 (crystal in pin) input during test mode.
2. 0 to -1% modulation down spread from the selected frequency.
3. SDRAMR clock is selected by the latched (SD_SEL) REF1 pin. With SD_SEL = "1" SDRAMR clock = CPU, with SD_SEL = "0" SDRAMR clock = AGP.
4. Test Mode output M SDRAMR depends on SD_SEL latched value.

Technical Pin Function Descriptions

VDD(1,2,3)
This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:2), PCICLK, 48/24MHzA/B and SDRAM.

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2
This is the power supplies for the CPUCLK and IOAPCI output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

X1
This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. With a nominal value of 33pF no external load cap is needed for a C_L=17 to 18pF crystal.

X2
This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor nominally 33pF.

CPUCLK (0:3)
These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks are controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

48MHz
This is a fixed frequency Clock output that is typically used to drive Super I/O devices. Outputs 0 and 1 are defined as 48MHz.

(Sel) 24/48
This is a fixed frequency clock output that is typically used to drive Super I/O devices. It defines the function of 24/48 bidirectional pin. Has pullup to VDD.

Mode
Input is latched at power-up to define function of PCICLK5/ AGP_STOP# bidirectional pin. Has pullup to VDD.

IOAPIC (0:1)
This Output is a fixed frequency Output Clock that runs at the Reference Input (typically 14.31818MHz) . Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

REF(0:2)
The REF Outputs are fixed frequency Clocks that run at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F
This Output is equal to PCICLK(0:5) and is FREE RUNNING, and will not be stopped by PCI_STP#.

PCICLK (0:4)
These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency.

PCICLK5
This bidirectional Input/Output is equal to PCICLK5 if MODE latched input is 1. Output is Tristated if MODE is latched a 0 (becomes AGP_STOP# Input)

PWR_DWN#
This is an asynchronous active Low Input pin used to Power Down the device into a Low Power state by not removing the power supply. The internal Clocks are disabled and the VCO and Crystal are stopped. Powered Down will also place all the Outputs in a low state at the end of their current cycle. The latency of Power Down will not be greater than 3ms.

AGP
This output pin is the clock that drives AGP or other related circuitry. The voltage swing, of this clock is controlled by the voltage level applied to the VDDH pin. This output frequency is defined as 2X PCICLK, see frequency select table.

AGP_STOP#
This bidirectional pin is an input for Stop control of the AGP clocks if the MODE is latched a 0. Has a pullup to VDD.

CPU_STOP#
This is a synchronous active Low Input pin used to stop the CPUCLK clocks in an active low state. All other Clocks including SDRAM clocks will continue to run while this function is enabled. The CPUCLK's will have a turn ON latency of at least 3 CPU clocks. This input pin only valid when MODE=0 (Power Management Mode)

PCI_STOP#
This is a synchronous active Low Input pin used to stop the PCICLK clocks in an active low state. It will not effect PCICLK_F nor any other outputs. This input pin only valid when MODE=0 (Power Management Mode)

Power Management

Clock Enable Configuration

AGP STOP	CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	AGP (0:1)	PCICLK (0:5)	PCI_F AGP2 REF, IOAPICs, 48 MHz 24/48 MHz	Crystal	VCOs	SDRAMR
x	X	X	0	Low	Low	Low	Stopped	Off	Off	Low
1	0	0	1	Low	Running	Low	Running	Running	Running	Running
1	0	1	1	Low	Running	Running	Running	Running	Running	Running
1	1	0	1	Running	Running	Low	Running	Running	Running	Running
1	1	1	1	Running	Running	Running	Running	Running	Running	Running
0	1	1	1	Running	Low	Running	Running	Running	Running	Running

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PWR PD# select pin will not cause clocks of a short or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

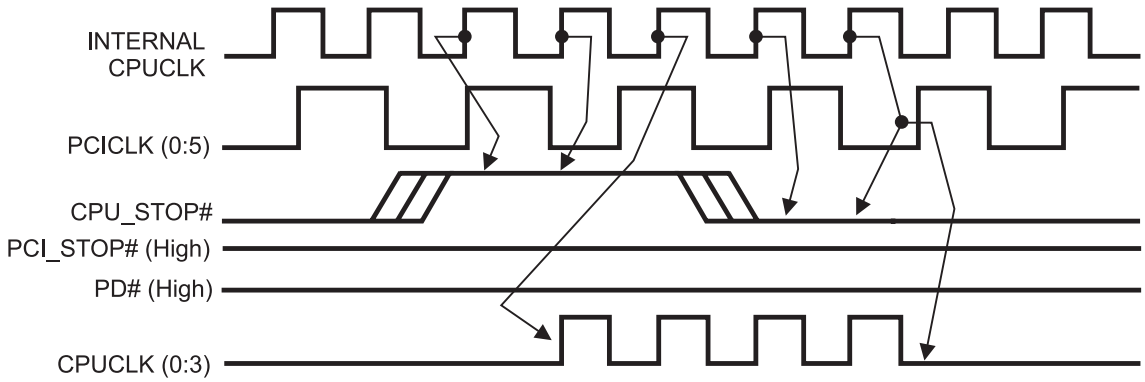
ICS9148-27 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency No. of rising edges of free running PCICLK
CPU_ STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PCI_STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PWR_DWN#	1 (Normal Operation)[3]	3ms
	0 (Power Down)[4]	2max
AGP_STOP	0 (Disabled)[2]	0
	1 (Enabled)[1]	0

Notes.
1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.
   The REF and IOAPIC will be stopped independant of these.

CPU_STOP# Timing Diagram

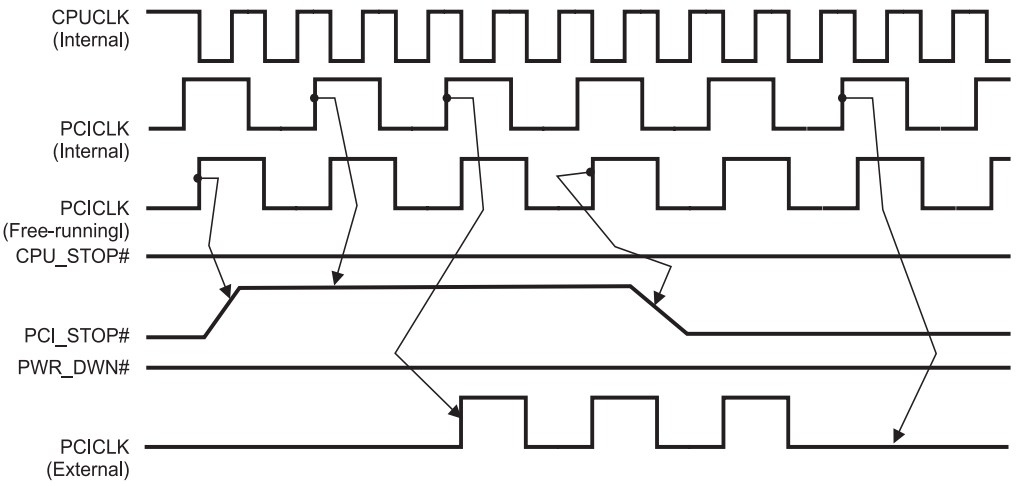
CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9148-27**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9148-27**.
3. All other clocks continue to run undisturbed including SDRAMR.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

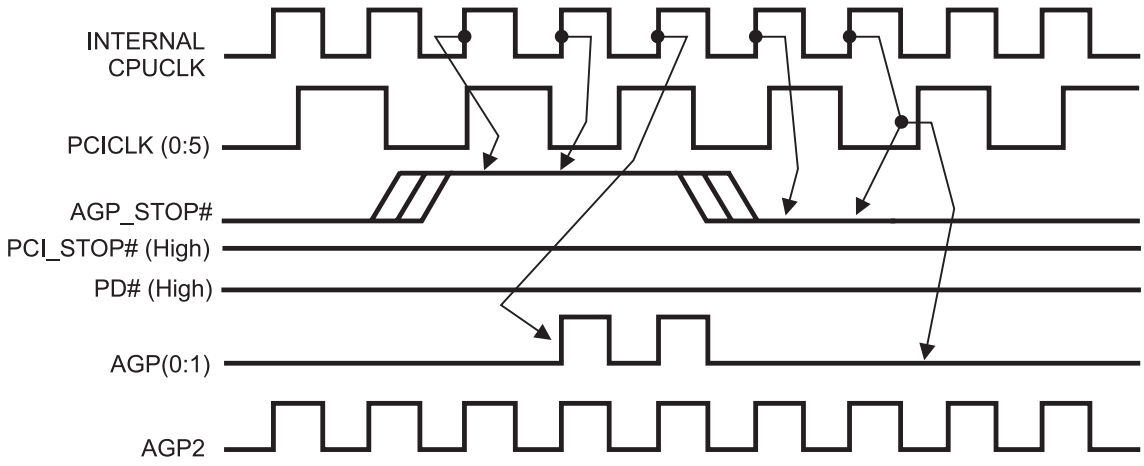
PCI_STOP# is an asynchronous input to the **ICS9148-27**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9148-27** internally. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

AGP_STOP# Timing Diagram

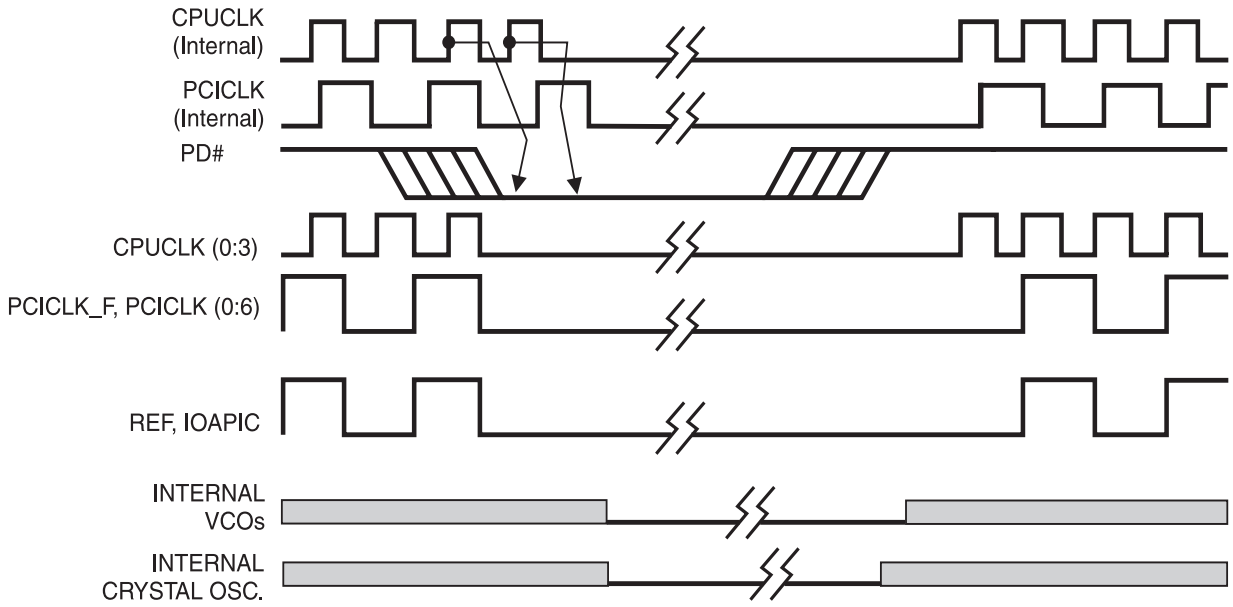
AGP_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the AGP (0:1) clocks. for low power operation. AGP_STOP# is synchronized by the **ICS9148-27**. The AGP2 clock is free-running and is not affected by AGP_STOP#. All other clocks will continue to run while the AGPCLKs are disabled. The AGPCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. AGPCLK on latency is less than AGPCLK and AGPCLK off latency is less than 4 AGPCLKs. This function is available only with MODE pin latched low.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. AGP_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9148-27**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.
5. Only applies if MODE pin latched 0 at power up.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the **ICS9148-27** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3mS. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9148.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz		60	170	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz		66	170	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND		3	600	µA
Input frequency	F_i	V_{DD} = 3.3 V;	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{AGP-PCI1}$	V_T = 1.5 V;	1.3	1.85	2.3	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP66}$	C_L = 0 pF; Select @ 66.8 MHz		16	72	mA
	$I_{DD2.5OP100}$	C_L = 0 pF; Select @ 100 MHz		23	100	mA
Power Down Supply Current	$I_{DD2.5PD}$	C_L = 0 pF; With input address to Vdd or GND		10	100	mA
Skew[1]	$t_{CPU-AGP}$		-0.5	-0.4	0	ns
	$t_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V	1	1.5	2	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48 MHz

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	3		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.14	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-44	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	42		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	52	55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		1	3	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V		3	5	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.3		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.2	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-41	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	37		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.25	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	48	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		100	175	ps
Jitter, Single Edge Displacement	t_{jseD}	V_T = 1.25 V		150	200	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V		40	150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250	140	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -18 mA	2	2.2		V
Output Low Voltage	V_{OL4B}	I_{OL} = 18 mA		0.33	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-41	-28	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	29	37		mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.3	1.6	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.1	1.6	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45	54	55	%
Skew[1]	t_{sk4B}[1]	V_T = 1.25 V		60	250	ps
Jitter, One Sigma[1]	T_{j1s4B}	V_T = 1.25 V		1	3	%
Jitter, Absolute[1]	T_{jabs4B}	V_T = 1.25 V	-5		5	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.1	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-62	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	57		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		140	500	ps
Jitter, One Sigma[1]	t_{j1s1}	V_T = 1.5 V		17	150	ps
Jitter, Absolute[1]	t_{jabs1}	V_T = 1.5 V	-500	70	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6	3.1		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.17	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-44	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	29	42		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jitter, One Sigma[1]	t_{j1s5}	V_T = 1.5 V		1	3	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V		3	5	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAMR, AGP

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -18 mA	2.4	2.6		V
Output Low Voltage	V_{OL3}	I_{OL} = 18 mA		0.3	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-62	-40	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	40	55		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45	50	55	%

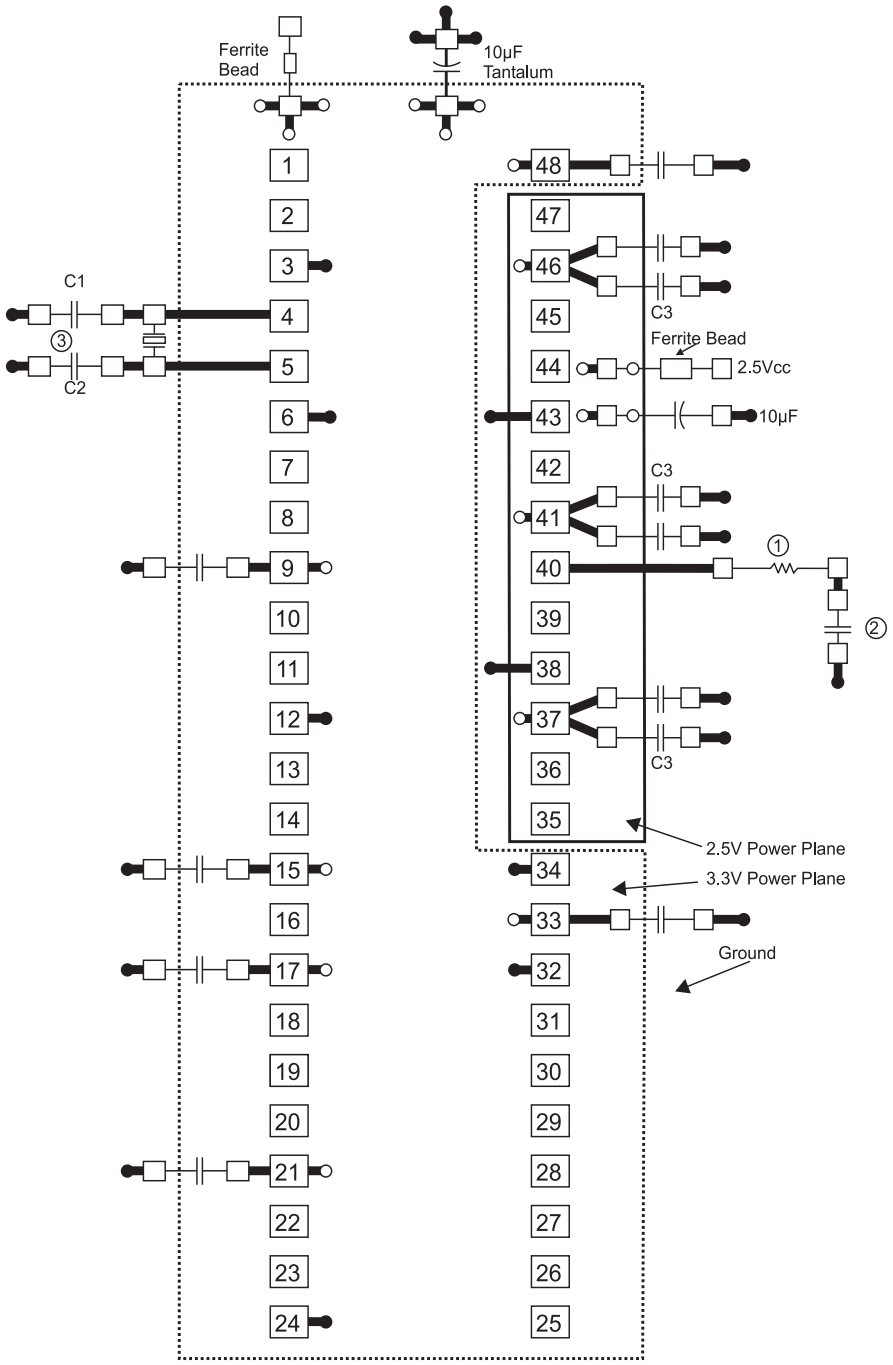
[1]Guarenteed by design, not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
3 Optional crystal load capacitors are recommended.



Capacitor Values:

C1, C2 : Crystal load values determined by user

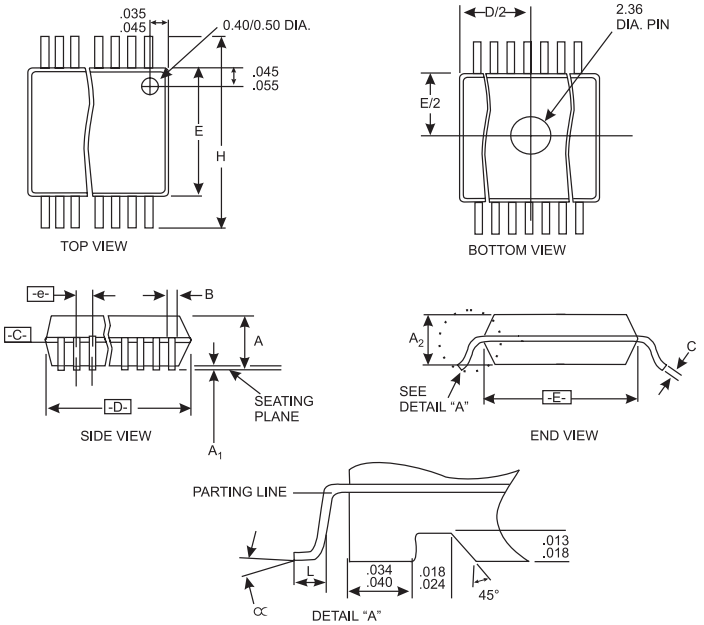
C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic

● = Ground Plane Connection

○ = Power Plane Conncetion

□ = Solder Pads



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	.006	.0085					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

This table in inches

Ordering Information

ICS9148F-27

Example:

ICS XXXXy F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator**
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device