

HiPerFET™ Power MOSFETs

IXFB 50N80Q2

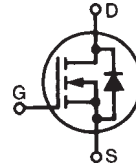
N-Channel Enhancement Mode
Avalanche Rated, Low Q_g , Low Intrinsic R_g
High dV/dt , Low t_{rr}

$$V_{DSS} = 800 \text{ V}$$

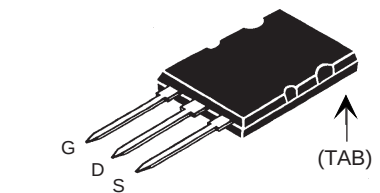
$$I_{D25} = 50 \text{ A}$$

$$R_{DS(on)} = 0.15 \Omega$$

$$t_{rr} \leq 300 \text{ ns}$$



PLUS 264™ (IXFB)



G = Gate
S = Source

D = Drain
TAB = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	800	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	800	V
V_{GS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	50	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	200	A
I_{AR}	$T_C = 25^\circ\text{C}$	50	A
E_{AR}	$T_C = 25^\circ\text{C}$	60	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	5.0	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$ $T_J \leq 150^\circ\text{C}$, $R_G = 2 \Omega$	20	V/ns
P_D	$T_C = 25^\circ\text{C}$	890	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6 mm (0.063 in.) from case for 10 s	300	$^\circ\text{C}$

Features

- Double metal process for low gate resistance
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- easy to drive and to protect
- Fast intrinsic rectifier

Applications

- DC-DC converters
- Switched-mode and resonant-mode power supplies, >500kHz switching
- DC choppers
- Pulse generation
- Laser drivers

Advantages

- PLUS 264™ package for clip or spring mounting
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 1 \text{ mA}$	800		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8 \text{ mA}$	3.0		5.0 V
I_{GSS}	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0 \text{ V}$			50 μA 3 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 \cdot I_{D25}$ Note 1			0.15 Ω

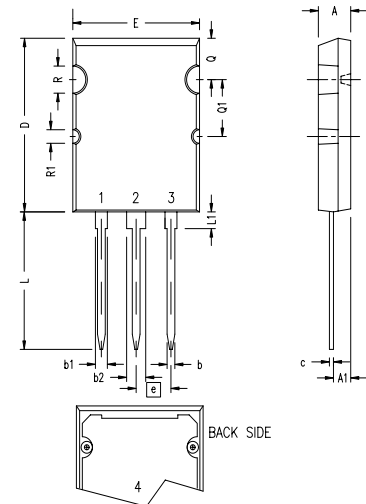
Symbol	Test Conditions		Characteristic Values (T _J = 25°C, unless otherwise specified)		
			min.	typ.	max.
g_{fs}	V _{DS} = 20 V; I _D = 0.5 • I _{D25}	Note 1	32	48	S
C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz			7200	pF
C_{oss}				1200	pF
C_{rss}				230	pF
t_{d(on)}	V _{GS} = 10 V, V _{DS} = 0.5 • V _{DSS} , I _D = 0.5 • I _{D25} R _G = 1 Ω (External)			26	ns
t_r				25	ns
t_{d(off)}				60	ns
t_f				13	ns
Q_{G(on)}	V _{GS} = 10 V, V _{DS} = 0.5 • V _{DSS} , I _D = 0.5 • I _{D25}			260	nC
Q_{GS}				56	nC
Q_{GD}				120	nC
R_{thJC}				0.14	K/W
R_{thCK}				0.13	K/W

Source-Drain Diode

Symbol	Test Conditions		Characteristic Values (T _J = 25°C, unless otherwise specified)		
			min.	typ.	max.
I_S	V _{GS} = 0 V				50 A
I_{SM}	Repetitive; pulse width limited by T _{JM}				200 A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Note 1				1.5 V
t_{rr}	I _F = 25A -di/dt = 100 A/μs V _R = 100 V			1.1	300 ns
Q_{RM}					μC
I_{RM}					A

Note: 1. Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %

PLUS 264™ Outline



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)
4 - Drain (Collector)

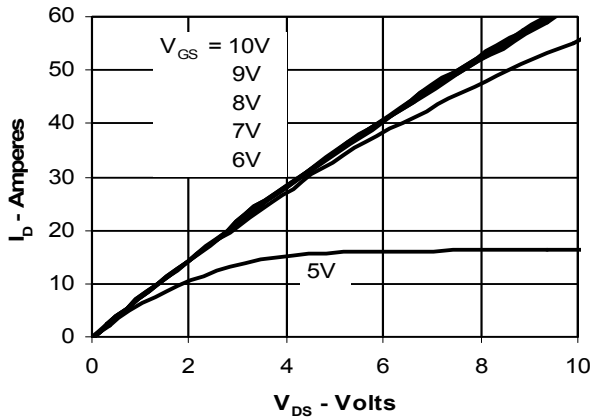
SYM	INCHES	
	MIN	MAX
A	.185	.209
A1	.102	.118
b	.037	.055
b1	.087	.102
b2	.110	.126
c	.017	.029
D	1.007	1.047
E	.760	.799
e	.215	BSC
L	.779	.842
L1	.087	.102
Q	.240	.256
Q1	.330	.346
ØR	.155	.187
ØR1	.085	.093

IXYS reserves the right to change limits, test conditions, and dimensions.

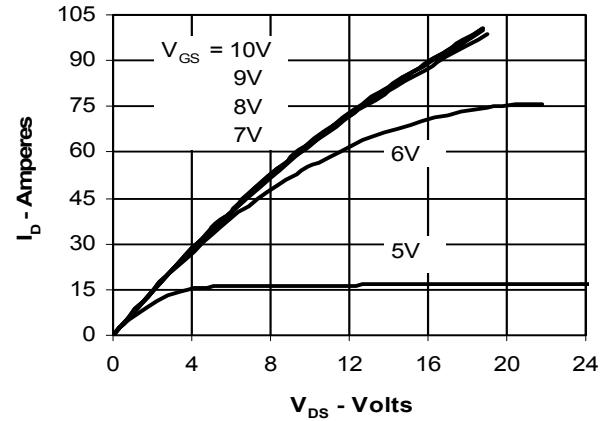
IXYS MOSFETS and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715	6,306,728B1
4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025	

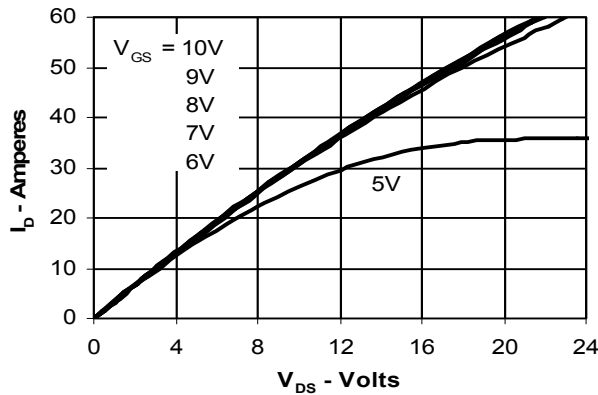
**Fig. 1. Output Characteristics
@ 25 Deg. C**



**Fig. 2. Extended Output Characteristics
@ 25 deg. C**



**Fig. 3. Output Characteristics
@ 125 Deg. C**



**Fig. 4. $R_{DS(on)}$ Normalized to I_{D25} Value
vs. Junction Temperature**

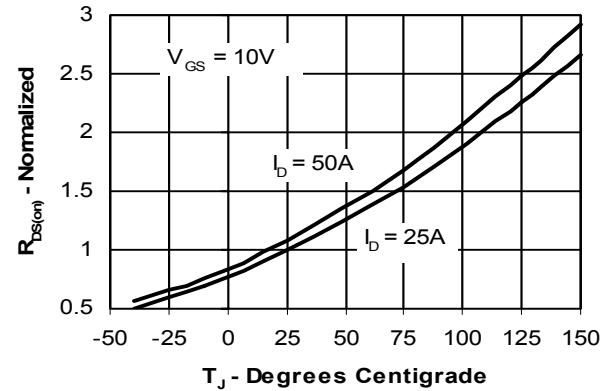
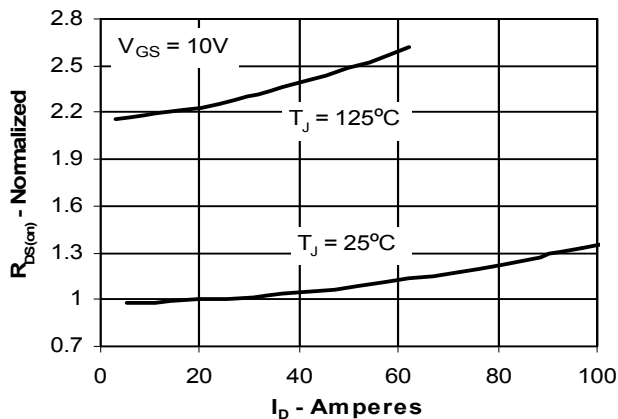


Fig. 5. $R_{DS(on)}$ Normalized to I_{D25} Value vs. I_D



**Fig. 6. Drain Current vs. Case
Temperature**

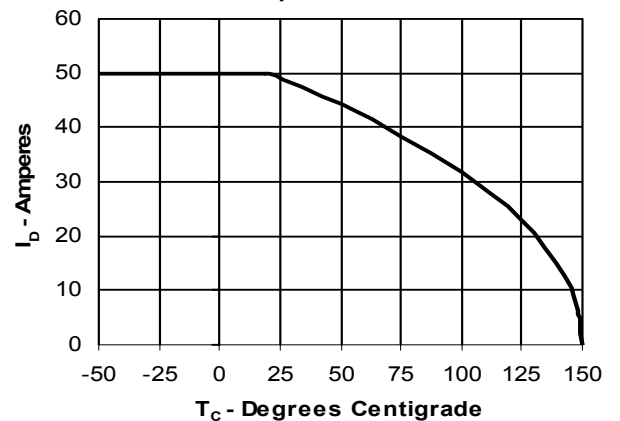


Fig. 7. Input Admittance

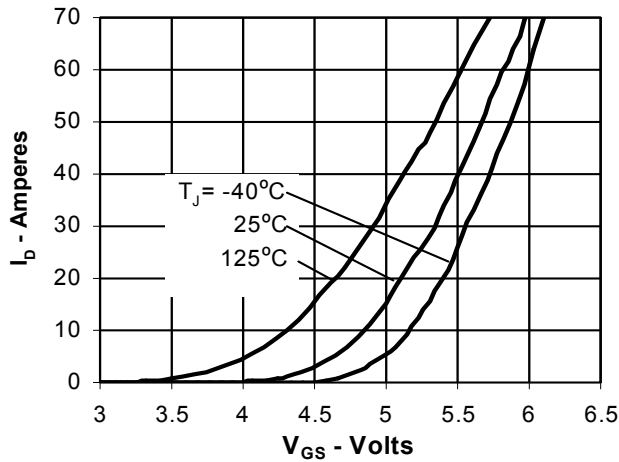


Fig. 8. Transconductance

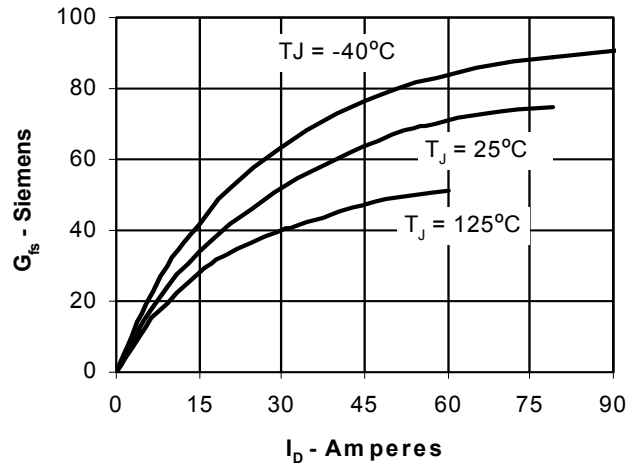


Fig. 9. Source Current vs. Source-To-Drain Voltage

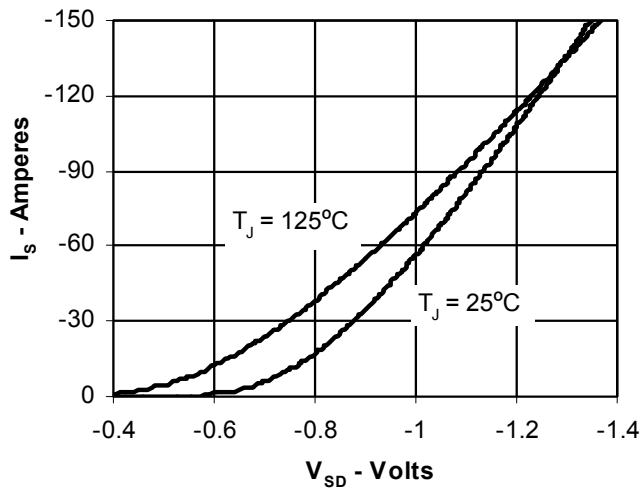


Fig. 10. Gate Charge

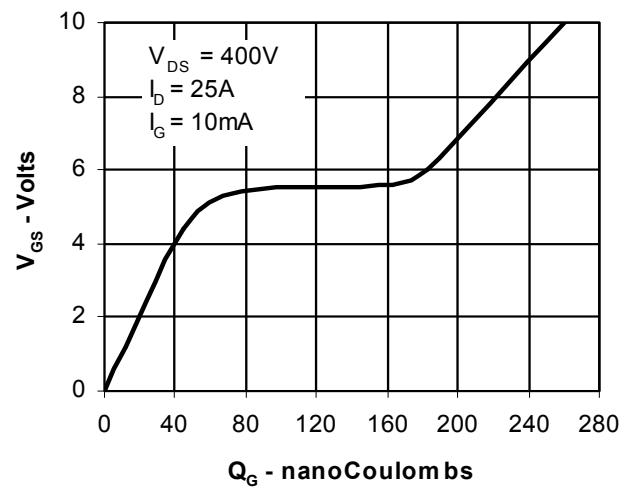


Fig. 11. Capacitance

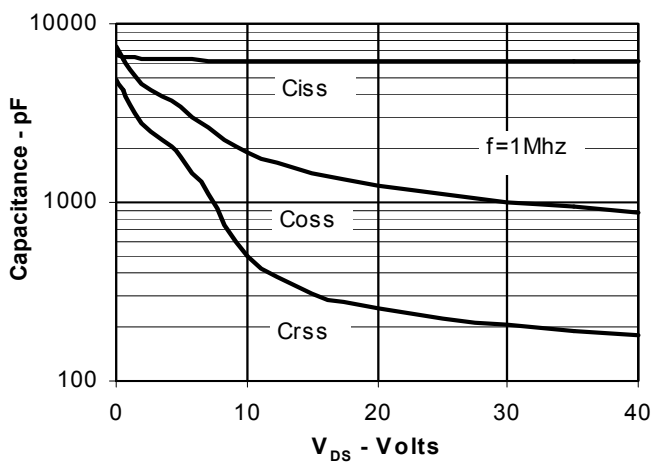
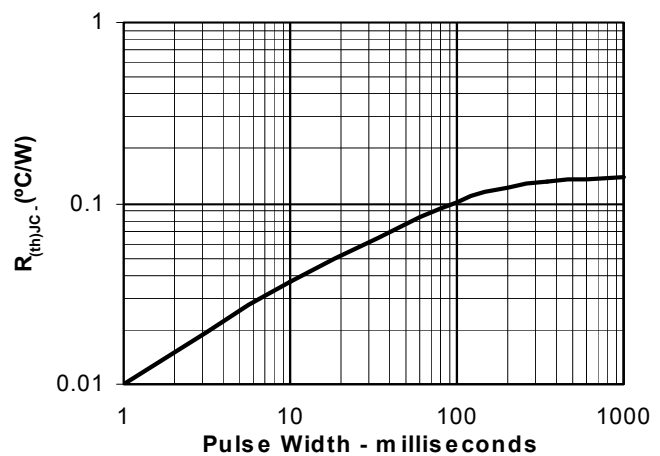


Fig. 12. Maximum Transient Thermal Resistance



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