



## ILC1232

October 1999

### $\mu$ P Supervisory Circuit

Preliminary

#### General Description

The ILC1232 is a multifunction circuit which monitors microprocessor activity, external reset and power supplies in microprocessor based systems. The circuit functions include a watchdog timer, power supply monitor, microprocessor reset, and manual pushbutton reset input.

The power supply line is monitored with a comparator and an internal voltage reference.  $\overline{\text{RST}}$  is forced low when an out-of-tolerance condition exists and remains asserted for at least 250 ms after  $V_{\text{CC}}$  rises above the threshold voltage (4.5 V or 4.75 V). The  $\overline{\text{RST}}$  pin will remain logic low with  $V_{\text{CC}}$  as low as 1.4 V.

The Watchdog input ( $\overline{\text{ST}}$ ) monitors  $\mu$ P activity and will assert  $\overline{\text{RST}}$  if no  $\mu$ P activity has occurred within the watchdog timeout period. The watchdog timeout period is selectable with nominal periods of 150, 600, or 1200 milliseconds.

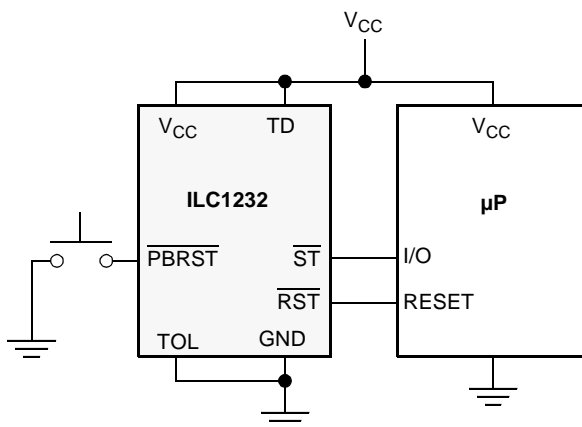
#### Features

- ◆ Power OK/Reset Time Delay, 250 ms min.
- ◆ Watchdog Timer, 150 ms, 600 ms, or 1.2 s Typical
- ◆ Precision Supply Voltage Monitor, Select Between 5% or 10% of Supply Voltage
- ◆ 18  $\mu$ A Supply Current
- ◆ Debounced External Reset Input
- ◆ 8-Pin SOIC or DIP Package

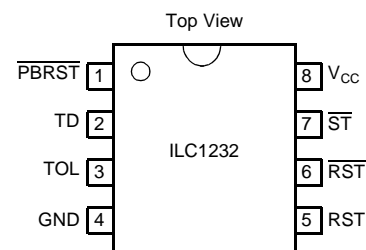
#### Applications

- ◆ Computers
- ◆ Controllers
- ◆ Critical Microprocessor Power Monitoring
- ◆ Intelligent Instruments
- ◆ Portable Equipment

#### Typical Circuit



#### Pin - Package Configurations



ETC1232N - 8 Lead Plastic DIP Package  
ETC1232M - 8 Lead Plastic SOIC Package

#### Ordering Information

Part	Package	Temp. Range
ILC1232N	8-Lead PDIP	-40°C to +85°C
ILC1232M	8-Lead SOIC	-40°C to +85°C



**Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Units
Terminal Voltage	$V_{CC}$	-0.3 to 6.0	V
	All other inputs	-0.3 to ( $V_{CC} + 0.3$ )	V
Input Current	$V_{CC}$	250	mA
	GND, All other inputs	25	mA
Operating Temperature Range	$T_A$	-40 to +85	°C
Storage Temperature Range		-65 to +150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C
Power Dissipation		700	mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Operating ranges define those limits between which the functionality of the device is guaranteed.

**Electrical Characteristics**

$V_{CC} = 4.5$  V to 5.5 V,  $T_A$  = Operating Temperature Range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range, $V_{CC}$		4.5		5.5	V
Supply Current, $I_{CC}$	(See Note 1)		18	40	$\mu$ A
$\overline{ST}$ and $\overline{PBRST}$ Input Levels	$V_{IH}$ (See Note 2) $V_{IL}$	2.0 -0.3		$V_{CC} + 0.3$ 0.8	V
Input Leakage, $I_{IL}$				$\pm 1$	$\mu$ A
Output Source Current, $RST$	$V_{OH} = 2.4$ V	1.0	10		mA
Output Sink Current, $\overline{RST}$ , $RST$	$V_{OL} = 0.4$ V	2.0	10		mA
$V_{CC}$ 5% Trip Point (Reset Threshold Voltage)	TOL = GND	4.50	4.62	4.74	V
$V_{CC}$ 10% Trip Point (Reset Threshold Voltage)	TOL = $V_{CC}$	4.25	4.37	4.49	V
Input Capacitance, $\overline{ST}$ , TOL	$C_{IN}$ (See Note 3)			5	pF
Output Capacitance, $\overline{RST}$ , $RST$	$C_{OUT}$ (See Note 3)			7	pF
$\overline{PBRST}$ Min. Pulse Width, $t_{PB}$	$\overline{PBRST} = V_{IL}$ (See note 4)	20			ms
$\overline{PBRST}$ Delay, $t_{PBD}$		1	4	20	ms
Reset Active Time, $t_{RST}$		250	610	1000	ms
$\overline{ST}$ Pulse Width, $t_{ST}$		20			ns
$\overline{ST}$ Timeout Period, $t_{TD}$	$T_D = 0$ V $T_D = \text{Open}$ $T_D = V_{CC}$	62.5 250 500	150 600 1200	250 1000 2000	ms
$V_{CC}$ Fall Time, $t_F$		10			$\mu$ s
$V_{CC}$ Rise Time, $t_R$		0			ns
$V_{CC}$ Detect to $\overline{RST}$ Low and $RST$ High, $t_{RPD}$	$V_{CC}$ Falling at 1.66 mV/ $\mu$ s		50	150	$\mu$ s
$V_{CC}$ Detect to $\overline{RST}$ Open and $RST$ Low, $t_{RPU}$	$V_{CC}$ Rising (See note 5)	250	610	1000	ms

Note 1:  $I_{CC}$  is measured with outputs open and inputs within 0.5 V of supply rails.

Note 2:  $\overline{PBRST}$  has an internal 40 k $\Omega$  (typical) pull-up resistor to  $V_{CC}$ .

Note 3: Guaranteed by design.

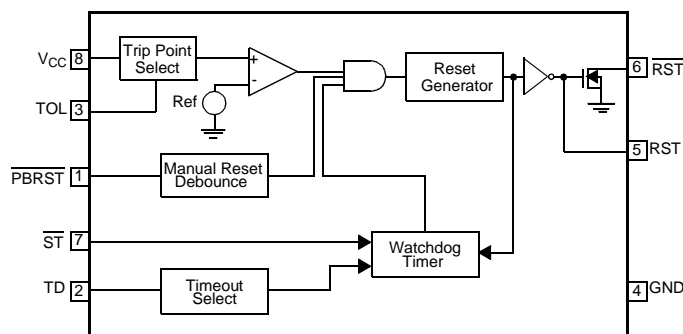
Note 4:  $\overline{PBRST}$  must be held low for a minimum of 20 ms to guarantee a reset.

Note 5:  $\overline{RST}$  has an open drain output.

## Pin Functions

Pin Number	Pin Name	Description
1	$\overline{PBRST}$	Pushbutton reset input. This input is debounced and can be driven with external logic signals or a mechanical pushbutton to actively force a reset. All pulses less than 1 ms in duration on the $\overline{PBRST}$ pin are ignored. Any pulse with a duration of 20 ms or greater is guaranteed to cause a reset.
2	TD	Time delay input. This input selects the timebase used by the watchdog timer. When TD = 0V, the watchdog timeout period is set to a nominal value of 150 ms, when TD = open, the watchdog timeout period is set to a nominal value of 600 ms and when TD = $V_{CC}$ , the watchdog timeout period is 1.2 sec nominally.
3	TOL	Tolerance select input. Selects whether 5% or 10% of $V_{CC}$ is used as the reset threshold voltage. When TOL = 0 V, the 5% tolerance level is selected and when TOL = $V_{CC}$ , a 10% tolerance level is selected.
4	GND	Ground pin, 0 V reference.
5	RST	RST is asserted high if either $V_{CC}$ goes below the reset threshold, the watchdog times out or $\overline{PBRST}$ is pulled low for a minimum of 20 ms. RST remains asserted for one reset timeout period after $V_{CC}$ exceeds the reset threshold or after the watchdog times out or after $\overline{PBRST}$ goes high.
6	$\overline{RST}$	$\overline{RST}$ is asserted low if either $V_{CC}$ goes below the reset threshold, the watchdog times out or $\overline{PBRST}$ is pulled low for a minimum of 20 ms. $\overline{RST}$ remains asserted for one reset timeout period after $V_{CC}$ exceeds the reset threshold or after the watchdog times out or after $\overline{PBRST}$ goes high. Open-drain output.
7	$\overline{ST}$	Input to the watchdog timer. If $\overline{ST}$ does not see a transition from high to low within the watchdog timeout period, RST and $\overline{RST}$ will be asserted.
8	$V_{CC}$	Power supply input, 5 V.

## Block Diagram



## Circuit Description

### Power Monitor

The RST and  $\overline{\text{RST}}$  pins are asserted whenever  $V_{CC}$  falls below the reset threshold voltage set by the TOL pin. A 5% tolerance level (4.62 V reset threshold voltage) can be selected by connecting the TOL pin to ground or a 10% tolerance (4.37V reset threshold voltage) can be selected by connecting the TOL pin to  $V_{CC}$ . The reset pins will remain asserted for a period of 250 ms after  $V_{CC}$  has risen above the reset threshold voltage. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. RST will remain valid with  $V_{CC}$  as low as 1.4 V.

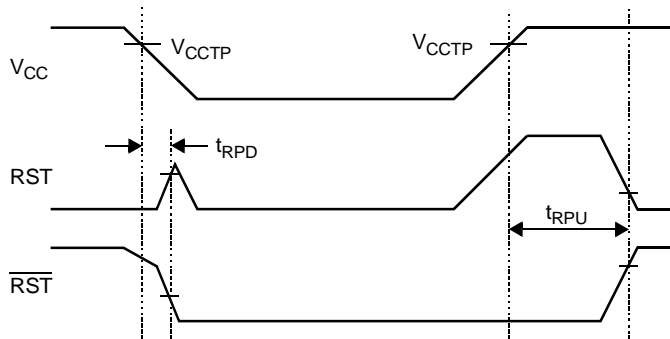


Figure 1: Power-Up/Power-Down Sequence

### Watchdog Timer

The microprocessor can be monitored by connecting the  $\overline{\text{ST}}$  pin (watchdog input) to a bus line or I/O line. If a high-to-low transition does not occur on the  $\overline{\text{ST}}$  pin within the watchdog timeout period set by the TD pin (see Table 1), the RST and  $\overline{\text{RST}}$  pins will be asserted resulting in a microprocessor reset. RST and  $\overline{\text{RST}}$  will remain asserted for 250 ms when this occurs. A minimum pulse of 75 ns or any transition high-to-low on the  $\overline{\text{ST}}$  pin will reset the watchdog timer. The watchdog timer will be reset if  $\overline{\text{ST}}$  sees a valid transition within the watchdog timeout period.

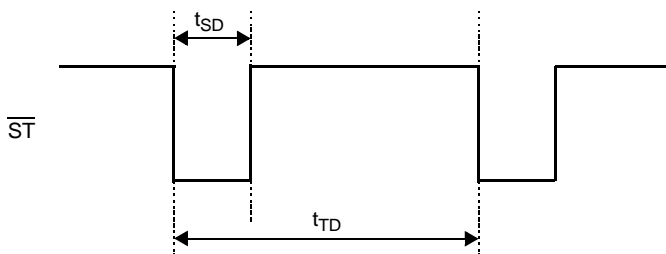


Figure 2: Watchdog Input

### Pushbutton Reset Input

The PBRST input can be driven with a manual pushbutton switch or with external logic signals. The input is internally debounced and requires an active low signal to force the reset outputs into their active states. The PBRST input will recognize any pulse that is 20ms in duration or greater and will ignore all pulses that are less than 1ms in duration.

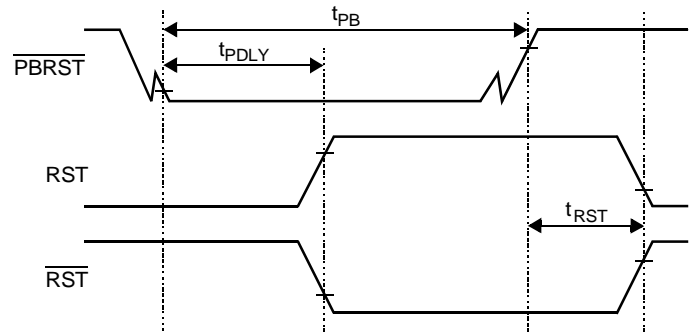


Figure 3: Pushbutton Reset

TD Pin	$t_{TD}$		
	Min.	Typ.	Max.
GND	62.5 ms	150 ms	250 ms
Open	250 ms	600 ms	1000 ms
$V_{CC}$	500 ms	1200 ms	2000 ms

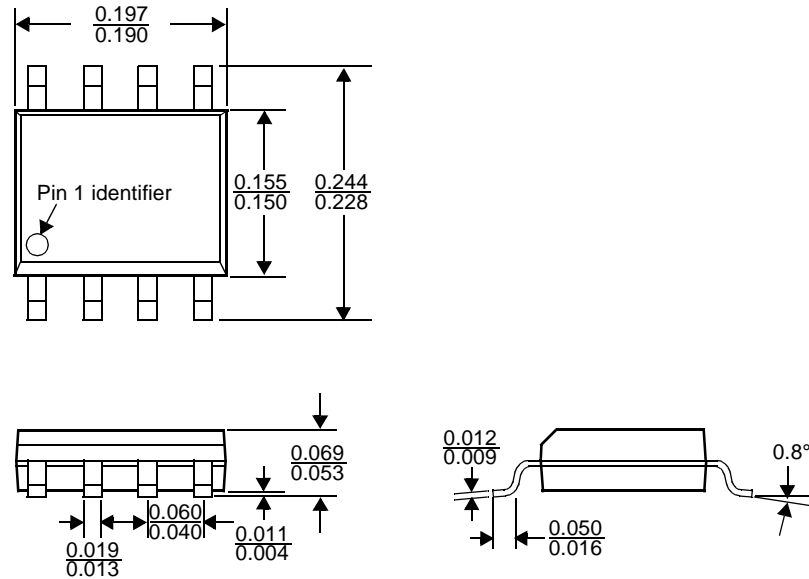
Table 1. Watchdog Timeout Period

### Alternate Source Cross Reference Guide

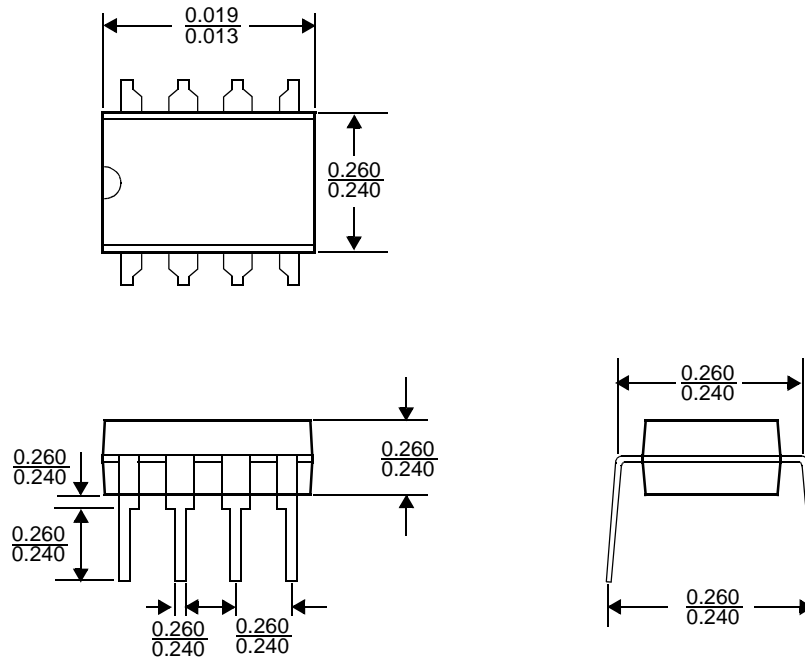
Industry P/N	ILC Direct Replacement
DS1232LP	ILC1232N
DS1232LPS-2	ILC1232M
DS1232	ILC1232N
DS1232LPN	ILC1232N
DS1232LPSN-2	ILC1232M
DS1232N	ILC1232N
MAX1232CPA	ILC1232N
MAX1232CSA	ILC1232M
MAX1232EPA	ILC1232N
MAX1232ESA	ILC1232M
MAX1232C/D	ILC1232D

# Packaging Information

## M Package, 8-Pin Small-Outline



## N Package, 8-Pin Plastic Dual In-Line



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