PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8344
Low Skew 1-to-24 Clock Fanout Buffer

General Description

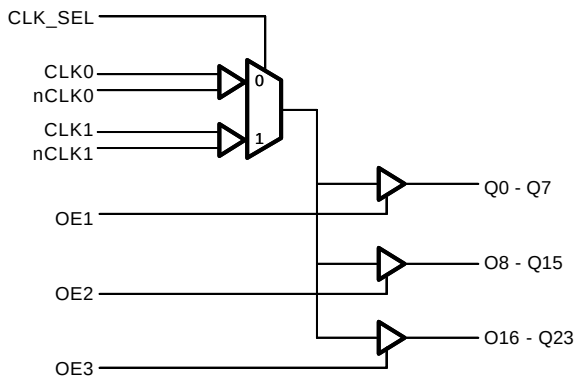
The ICS8344 is a low voltage, low skew fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8344 is designed to translate any differential signal levels to LVCMOS levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock input. The dual clock inputs also facilitate board level testing. ICS8344 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

Guaranteed output and part-to-part skew characteristics make the ICS8344 ideal for those clock distribution applications demanding well defined performance and repeatability.

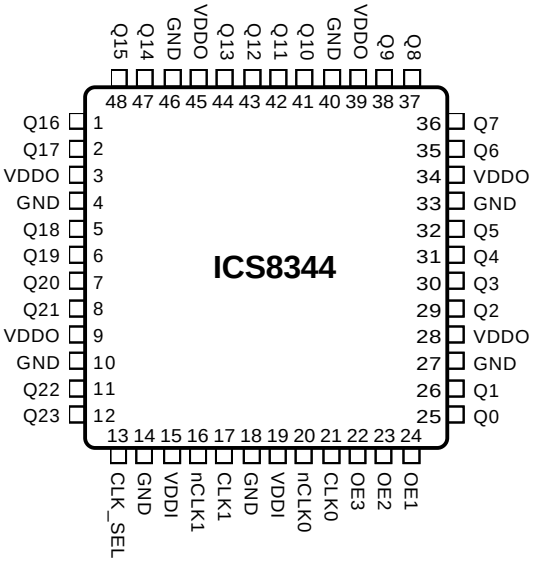
Features

- 24 LVCMOS outputs, 7Ω typical output impedance
- Output frequency up to 166MHz
- 150ps bank skew, 250ps output skew, 600ps part to part skew
- Translates any differential input signal (PECL, HSTL, LVDS) to LVCMOS without external bias networks
- Translates any single-ended input signal to LVCMOS with resistor bias on CLK input
- Translates and inverts any single-ended input signal to LVCMOS with resistor bias on nCLK input
- Multiple differential clock input pairs for redundant clock or multiple frequency applications
- LVCMOS control inputs
- Multiple output enable pins for disabling unused outputs in reduced fanout applications
- 3.3V, 2.5V or mixed 3.3V, 2.5V operating supply modes
- 48 lead low-profile QFP(LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- 0°C to 70°C ambient operating temperature

Block Diagram



Pin Assignment



48-Lead LQFP
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 5, 6 7, 8, 11, 12	Q16, Q17, Q18, Q19 Q20, Q21, Q22, Q23	Output		Q16 thru Q23 outputs. 7W typical output
3, 9, 28 34, 39, 45	VDDO	Power		Output power supply. Connect to ground.
4, 10, 14, 27 18, 33, 40, 46	GND	Power		Power supply ground. Connect to ground.
13	CLK_SEL	Input		Power supply pin. Connect to ground.
15, 19	VDDI	Power		Differential output. 3.3V PECL interface levels.
16	nCLK1	Input		Differential output. 3.3V PECL interface levels.
17	CLK1	Input		Input power supply pin. Connect to 3.3V.
20	nCLK0	Input		Differential output. 3.3V PECL interface levels.
21	CLK0	Input		Differential output. 3.3V PECL interface levels.
22	OE3	Input		Differential output. 3.3V PECL interface levels.
23	OE2	Input		Differential output. 3.3V PECL interface levels.
24	OE1	Input		Differential output. 3.3V PECL interface levels.
25, 26, 29, 30 31, 32, 35, 36	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Output		Differential output. 3.3V PECL interface levels.
37, 38, 41, 42 43, 44, 47, 48	Q8, Q9, Q10, Q11 Q12, Q13, Q14, Q15	Output	Pulldown	Non inverting differential clock input. Any differential input interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance					pF
CPD	Power Dissipation Capacitance (per output)	VDDI, VDDO = 3.465V				pF
		VDDI = 3.465V, VDDO = 2.63V				pF
		VDDI, VDDO = 2.63V				
RPULLUP	Input Pullup Resistor			51		Kohms
RPULLDOWN	Input Pulldown Resistor			51		Kohms
ROUT	Output Impedance			7		ohms

TABLE 3A. OUPUT ENABLE FUNCTION TABLE

Bank 1		Bank 2		Bank 3	
Input	Output	Input	Output	Input	Output
OE1	Q0-Q7	OE2	Q8-Q15	OE3	Q16-Q23
0	Hi-Z	0	Hi-Z	0	Hi-Z
1	Active	1	Active	1	Active

TABLE 3B. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	CLK0, nCLK0	CLK1, nCLK1
0	Selected	De-selected
1	De-selected	Selected

TABLE 3B. CLOCK INPUTS FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
OE1, OE2, OE3	CLK	nCLK	Q0 thru Q23		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Differential	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Differential	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Differential	Inverting

NOTE 1: Single ended input use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS input levels the recommended input bias network is a resistor to VDDI, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is VDDI/2.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. DC ELECTRICAL CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage			3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage			3.135	3.3	3.465	V
VIH	Input High Voltage	All except CLK, nCLK; NOTE 1	VDDI = 3.465V	2		3.8	V
VIL	Input Low Voltage	All except CLK, nCLK; NOTE 1	VDDI = 3.135V	-0.3		1.5	V
IIH	Input High Current	All except CLK	VDDI = VIN = 3.465V			5	µA
		CLK	VDDI = VIN = 3.465V			150	µA
IIL	Input Low Current	All except CLK	VDDI = 3.465, VIN = 0V	-150			µA
		CLK	VDDI = 3.465, VIN = 0	-5			µA
IDD	Quiescent Power Supply Current		VDDI = VIH = 3.465V VIL = 0V			70	mA
VOH	Output High Voltage		VDDI = VDDO = 3.135V IOH = -36mA	2.6			V
VOL	Output Low Voltage		VDDI = VDDO = 3.135V IOL = 36mA			0.5	V

NOTE 1: For CLK, nCLK input levels see VPP and VCMR in AC Electrical Characteristics table.

TABLE 5A. AC ELECTRICAL CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				166	MHz
VPP	Peak-to-Peak Input Voltage	f = 166MHz	0.3		1.3	V
VCMR	Common Mode Input Voltage	f = 166MHz	0.9		2	V
tpLH	Propagation Delay, Low-to-High	0MHz < f < 166MHz	2.6		4.5	ns
tpHL	Propagation Delay, High-to-Low	0MHz < f < 166MHz	2.6		4.5	ns
tsk(b)	Bank Skew; NOTE 2	Measured on the rising edge of VDDO/2			150	ps
tsk(o)	Output Skew; NOTE 3	Measured on the rising edge of VDDO/2			250	ps
tsk(pp)	Part-to-Part Skew; NOTE 4	Measured on the rising edge of VDDO/2			600	ps
tR	Output Rise Time; NOTE 5	30% to 70%	0.3		1.7	ns
tF	Output Fall Time; NOTE 5	30% to 70%	0.3		1.4	ns
tPW	Output Pulse Width		tCYCLE/2 - 650	tCYCLE/2	tCYCLE/2 + 650	ns
		f = 166MHz	2.35	3.01	3.65	ns
tEN	Output Enable Time	f = 10MHz			8	ns
tDIS	Output Disable TIme	f = 10MHz			5	ns

NOTE 1: All parameters measured at 166MHz and VPPmin unless noted otherwise. All outputs terminated with 50 ohms to VDDO/2.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as the skew at different outputs on different devicies operating at the same supply voltages with equal load conditions.
NOTE 5: These parameters are guaranteed by characterization. Not tested inproduction.

TABLE 4B. DC ELECTRICAL CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage			3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage			2.375	2.5	2.625	V
VIH	Input High Voltage	All except CLK, nCLK; NOTE 1	VDDI = 3.465V	2		3.8	V
			VDDI = 3.135V	1.9		3.4	V
VIL	Input Low Voltage	All except CLK, nCLK; NOTE 1	VDDI = 3.465V	-0.3		1.5	V
			VDDI = 3.135V	-0.3		1.2	V
IIH	Input High Current	All except CLK	VDDI = VIN = 3.465V			5	µA
		CLK	VDDI = VIN = 3.465V			150	µA
IIL	Input Low Current	All except CLK	VDDI = 3.465V, VIN = 0V	-150			µA
		CLK	VDDI = 3.465V, VIN = 0V	-5			µA
IDD	Quiescent Power Supply Current		VDDI = VIH = 3.465V VIL = 0V			70	mA
VOH	Output High Voltage		VDDI = 3.135V, VDDO = 2.375V IOH = -27mA	1.9			V
VOL	Output Low Voltage		VDDI = 3.135V, VDDO = 2.365V IOL = 27mA			0.5	V

NOTE 1: For CLK, nCLK input levels see VPP and VCMR in AC Electrical Characteristics table.

TABLE 5B. AC ELECTRICAL CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				166	MHz
VPP	Peak-to-Peak Input Voltage	f = 166MHz	0.3		1.3	V
VCMR	Common Mode Input Voltage	f = 166MHz	0.9		2	V
tpLH	Propagation Delay, Low-to-High	0MHz < f < 166MHz	2.6		4.5	ns
tpHL	Propagation Delay, High-to-Low	0MHz < f < 166MHz	2.6		4.5	ns
tsk(b)	Bank Skew; NOTE 2	Measured on the rising edge of VDDO/2			150	ps
tsk(o)	Output Skew; NOTE 3	Measured on the rising edge of VDDO/2			250	ps
tsk(pp)	Part-to-Part Skew; NOTE 4	Measured on the rising edge of VDDO/2			600	ps
tR	Output Rise Time; NOTE 5	30% to 70%	0.3		1.7	ns
tF	Output Fall Time; NOTE 5	30% to 70%	0.3		1.4	ns
tPW	Output Pulse Width		tCYCLE/2 - 500	tCYCLE/2	tCYCLE/2 + 500	ns
		f = 166MHz	2.35	3.01	3.65	ns
tEN	Output Enable Time	f = 10MHz			8	ns
tDIS	Output Disable TIme	f = 10MHz			5	ns

NOTE 1: All parameters measured at 166MHz and VPPmin unless noted otherwise. All outputs terminated with 50 ohms to VDDO/2.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as the skew at different outputs on different devicies operating at the same supply voltages with equal load conditions.
NOTE 5: These parameters are guaranteed by characterization. Not tested inproduction.

TABLE 4C. DC ELECTRICAL CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage			2.375	2.5	2.625	V
VDDO	Output Power Supply Voltage			2.375	2.5	2.625	V
VIH	Input High Voltage	All except CLK, nCLK; NOTE 1	VDDI = 2.625V	2		2.9	V
VIL	Input Low Voltage	All except CLK, nCLK; NOTE 1	VDDI = 2.375V	-0.3		0.8	V
IIH	Input High Current	All except CLK	VDDI = VIN = 2.625V			5	µA
		CLK	VDDI = VIN = 2.625V			150	µA
IIL	Input Low Current	All except CLK	VDDI = 2.625V, VIN = 0V	-150			µA
		CLK	VDDI = 2.625V, VIN = 0V	-5			µA
IDD	Quiescent Power Supply Current		VDDI = VIH = 2.625V VIL = 0V			70	mA
VOH	Output High Voltage		VDDI =VDDO = 2.375V IOH = -27mA	1.9			V
VOL	Output Low Voltage		VDDI = VDDO = 2.375V IOL = 27mA			0.5	V

NOTE 1: For CLK, nCLK input levels see VPP and VCMR in AC Electrical Characteristics table.

TABLE 5C. AC ELECTRICAL CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				166	MHz
VPP	Peak-to-Peak Input Voltage	f = 166MHz	0.3		1.3	V
VCMR	Common Mode Input Voltage	f = 166MHz	0.9		2	V
tpLH	Propagation Delay, Low-to-High	0MHz < f < 166MHz	2.6		4.5	ns
tpHL	Propagation Delay, High-to-Low	0MHz < f < 166MHz	2.6		4.5	ns
tsk(b)	Bank Skew; NOTE 2	Measured on the rising edge of VDDO/2			150	ps
tsk(o)	Output Skew; NOTE 3	Measured on the rising edge of VDDO/2			250	ps
tsk(pp)	Part-to-Part Skew; NOTE 4	Measured on the rising edge of VDDO/2			675	ps
tR	Output Rise Time; NOTE 5	30% to 70%	0.3		1.7	ns
tF	Output Fall Time; NOTE 5	30% to 70%	0.3		1.4	ns
tPW	Output Pulse Width		tCYCLE/2 - 500	tCYCLE/2	tCYCLE/2 + 500	ns
		f = 166MHz	2.35	3.01	3.65	ns
tEN	Output Enable Time	f = 10MHz			8	ns
tDIS	Output Disable TIme	f = 10MHz			5	ns

NOTE 1: All parameters measured at 166MHz and VPPmin unless noted otherwise. All outputs terminated with 50 ohms to VDDO/2.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as the skew at different outputs on different devicies operating at the same supply voltages with equal load conditions.
NOTE 5: These parameters are guaranteed by characterization. Not tested inproduction.

FIGURE 1A, 1B, 1C - INPUT CLOCK WAVEFORMS

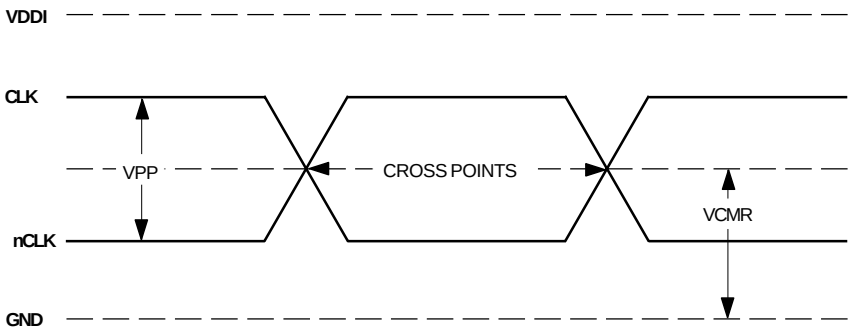


FIGURE 1A - LVDS, HSTL DIFFERENTIAL INPUT LEVELS

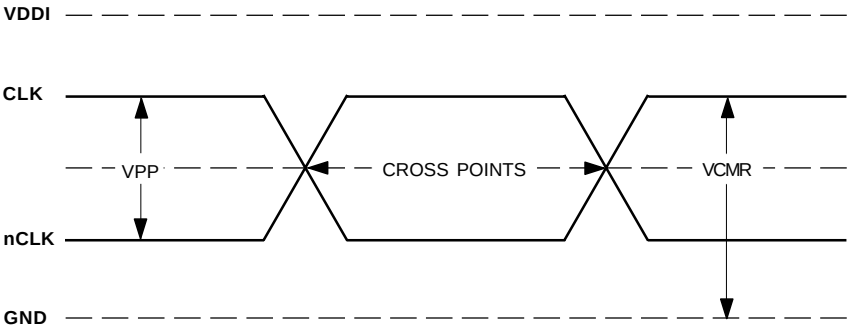


FIGURE 1B - LVPECL DIFFERENTIAL INPUT LEVEL

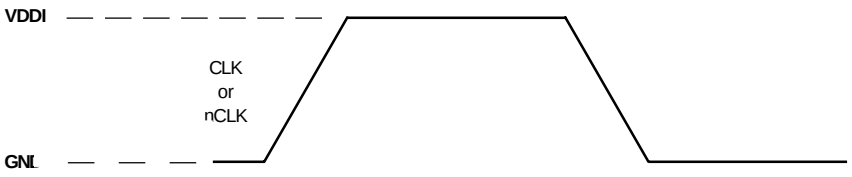


FIGURE 1C- LVCMOS AND LVTTL SINGLE ENDED INPUT LEVEL

FIGURE 2A, 2B - TIMING WAVEFORMS

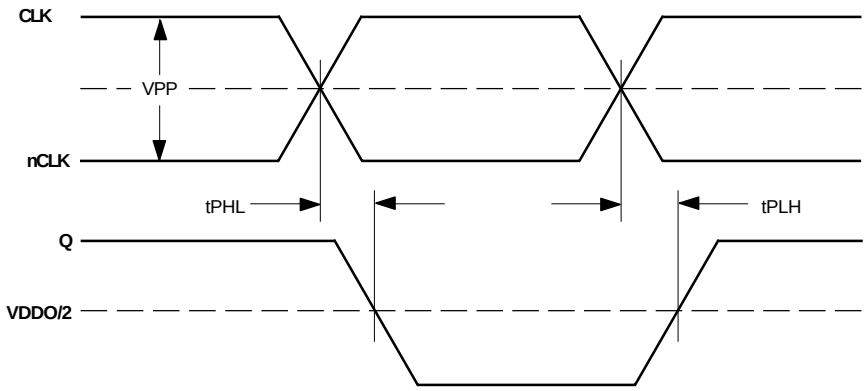


FIGURE 2A - PROPAGATION DELAYS

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

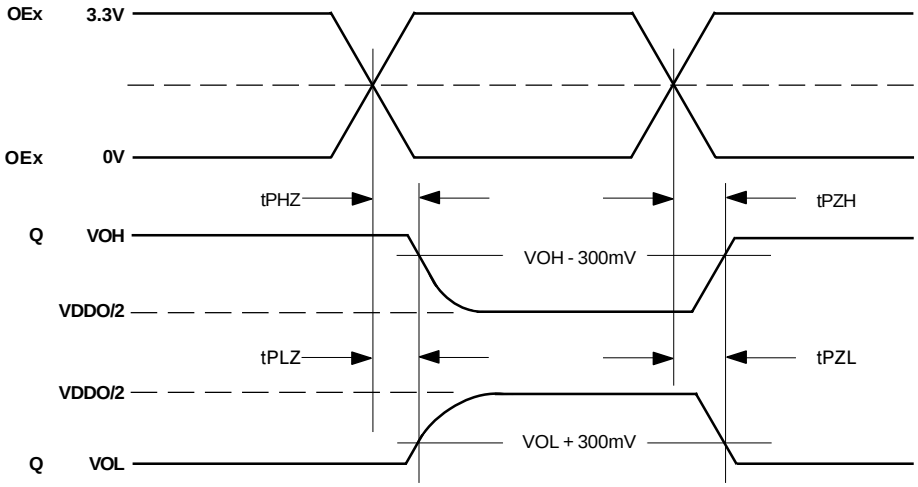


FIGURE 2B - DISABLE AND ENABLE TIMES

fin = 10MHz, Vamp = 3.3V, tr = tf = 600ps

FIGURE 3A, 3B- SKEW DEFINITIONS & WAVEFORMS

Bank Skew - Skew between outputs within a bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

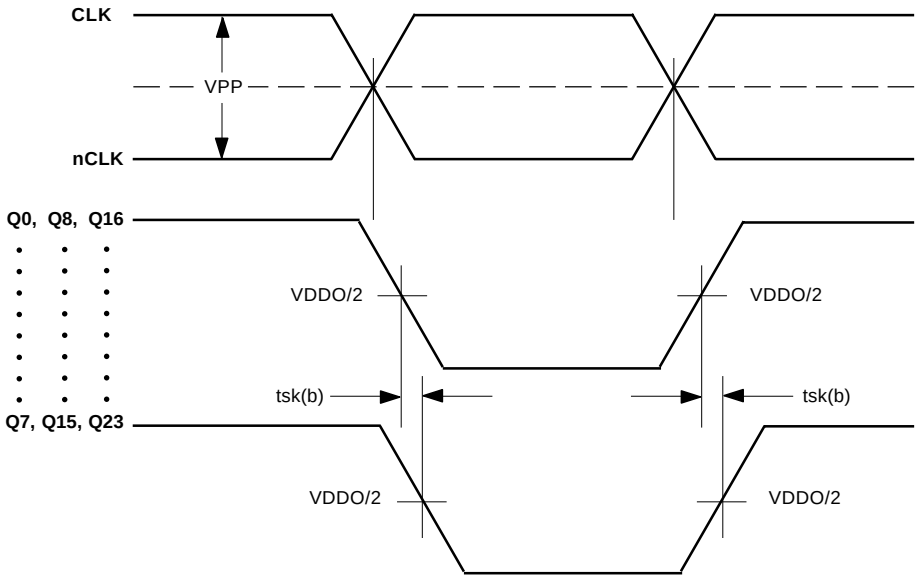


FIGURE 3A - BANK SKEW

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

Output Skew - Skew between outputs of any bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

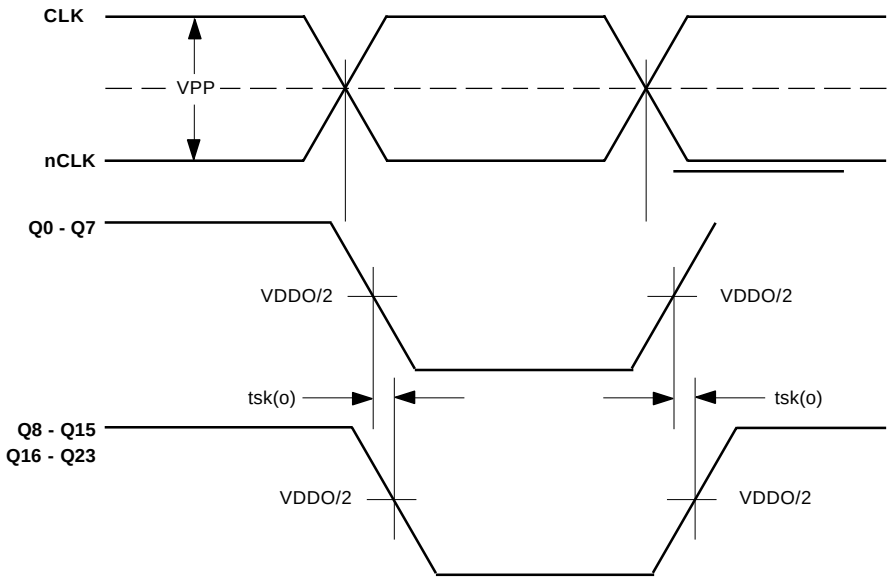


FIGURE 3B - OUTPUT SKEW

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

FIGURE 4A - SKEW DEFINITIONS & WAVEFORMS

Part to Part Skew - Skew between outputs of any bank on different parts. Outputs operating at the same temperature, supply voltages and with equal load conditions.

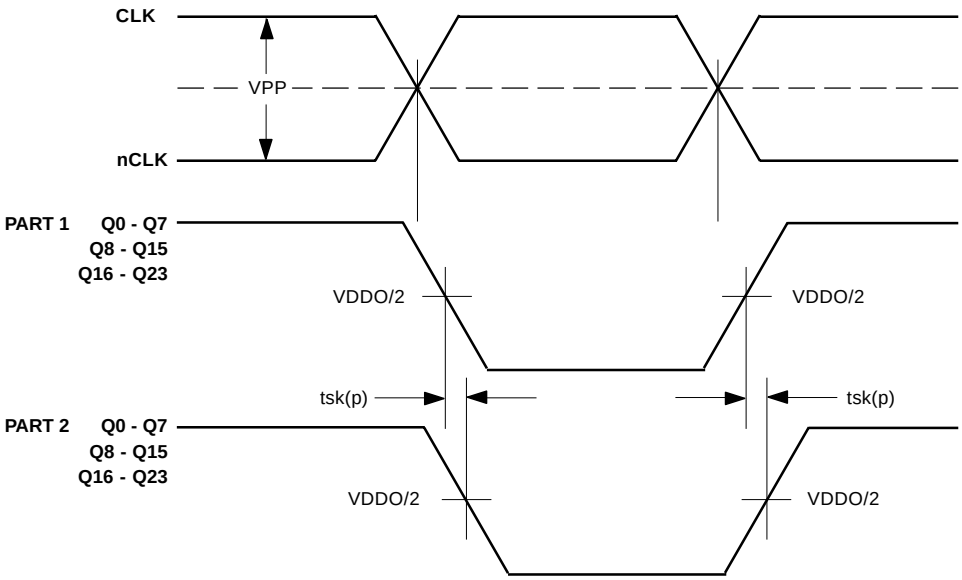
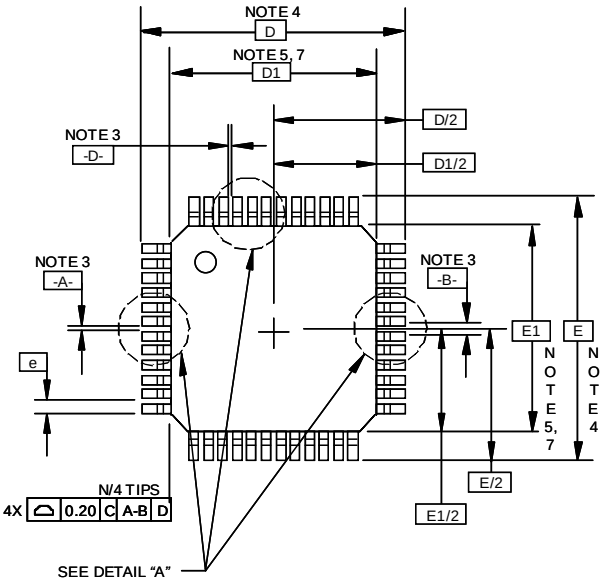
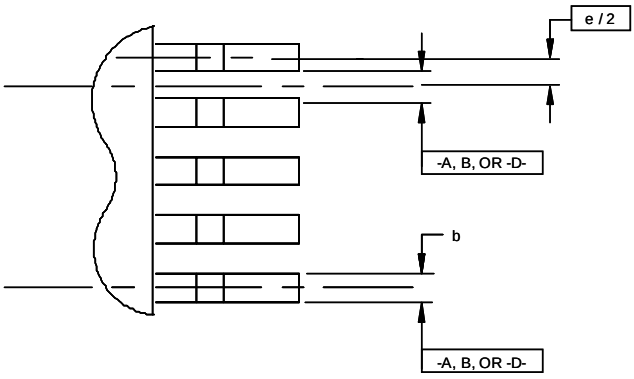


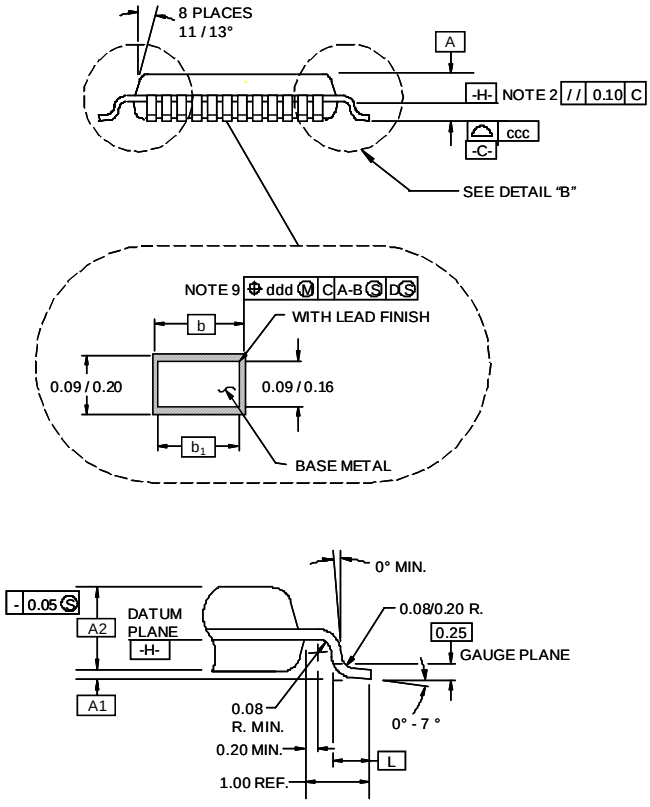
FIGURE 4B - OUTPUT SKEW

fin = 200MHz, Vpp = 300mV, tr = tf = 200ps

PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX







NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLACE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETEREMINED AT DATUM PLANE -H-.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
10. CONTROLLING DIMENSION: MILLIMETER.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLIBCATION 95 REGISTRATION MS-026, VARIATION BBC.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	BBC			
	MIN.	NOM.	MAX.	
A			1.60	
A_1	0.05		0.15	12
A_2	1.35	1.40	1.45	
D		9.00 BSC.		4
D_1		7.00 BSC.		7, 8
E		9.00 BSC.		4
E_1		7.00 BSC.		7, 8
L	0.45	0.60	0.75	
N		48		
e		0.5 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8344BY	ICS8344BY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8344BYT	ICS8344BY	48 Lead LQFP on Tape and Reel	2000	0°C to 70°C