ICS548-05C
T1/E1 Clock Multiplier

Description

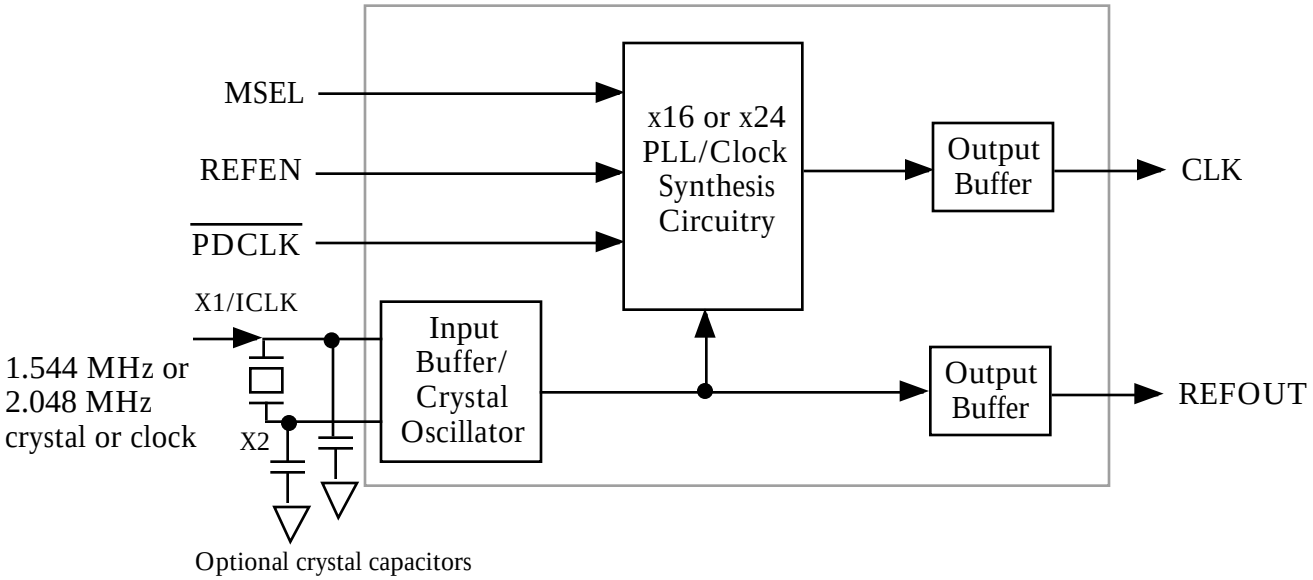
The ICS548-05C is a low cost, low jitter, high performance clock synthesizer designed to produce x16 or x24 clocks from T1 or E1 frequencies. Using ICS' patented analog/digital Phase-Locked Loop (PLL) techniques, the device uses a crystal or clock input to synthesize popular communications frequencies. Power down modes allow the chip to be turned off completely, or the PLL and clock output to be turned off separately.

ICS manufactures the largest variety of communications clock synthesizers for all applications. Consult ICS to eliminate VCXOs, crystals and oscillators from your board.

Features

- Packaged in 16 pin TSSOP
- Ideal for telecom/datacom chips
- Replaces oscillators
- 3.3V or 5V operation
- Uses a crystal or clock input
- Produces 24.704, 37.056, 32.768, or 49.152 MHz
- Includes Power Down features
- Advanced, low power, sub-micron CMOS process
- See also the MK2049-34 for generating

Block Diagram



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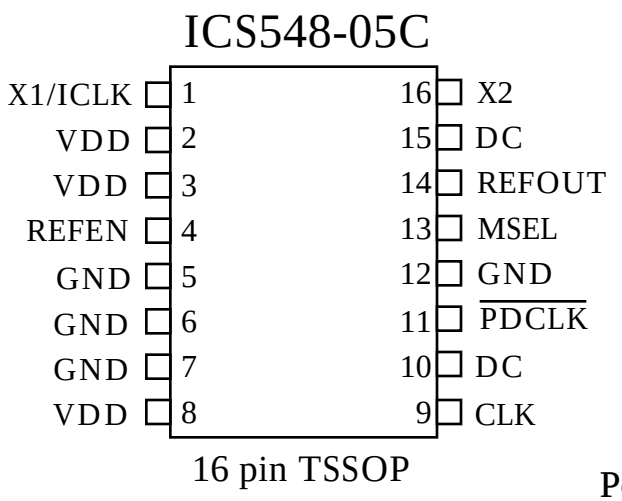
Pin Assignment



16 pin TSSOP

Output Clock Select Table

MSEL	Input (MHz)	CLK (MHz)
Pin 13	Pins 1, (16)	Pin 9
0	1.544	24.704
1	1.544	37.056
0	2.048	32.768
1	2.048	49.152

Power Down Clock Select Table

REFEN	$\overline{\text{PDCLK}}$	Power Down Selection Mode
Pin 4	Pin 11	
0	0	The entire chip is off.
0	1	PLL and CLK output run, REFOUT low.
1	0	REFOUT running, PLL off, CLK low.
1	1	All running.

Key: 0 = connect directly to GND
1 = connect directly to VDD

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	XI	Crystal connection. Connect to a crystal, or input clock.
2, 3, 8	VDD	P	Connect to +3.3V or +5V. All VDDs must be same.
4	REFEN	I	Reference Clock Enable. See above table. Connect to GND for best jitter/phase noise.
5, 6, 7, 12	GND	P	Connect to ground.
9	CLK	O	Clock output set by input and status of MSEL. See table above.
10, 15	DC	-	Don't Connect. Do not connect anything to these pins.
11	$\overline{\text{PDCLK}}$	I	Power Down Clock. See above table.
13	MSEL	I	Multiplier select pin. Selects x16 when low, x24 when high.
14	REFOUT	O	Buffered reference output clock. Controlled by REFEN.
16	X2	XO	Crystal connection. Connect to a crystal, or leave unconnected for clock.

Key: I = Input; O = output; P = power supply connection; XI, XO = crystal connections
The input pin MSEL must be tied directly to VDD or GND.

For a clock input, connect the input to X1, and leave X2 unconnected (floating).

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless noted)					
Core Operating Voltage, VDD		3.15		5.5	V
Input High Voltage, VIH, X1/ICLK pin	Clock input only	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, X1/ICLK pin	Clock input only		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-4mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		10		mA
Power Down Supply Current, IDDPD	No Load		1		µA
Short Circuit Current	CLK output		±50		mA
Input Capacitance	MSEL, $\overline{\text{PDCLK}}$, REFEN		7		pF
Frequency synthesis error	Both selections			0	ppm
AC CHARACTERISTICS (VDD = 3.3V unless noted)					
Input Crystal or Clock Frequency			1.544 or 2.048		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40	50	60	%
Start-up Time	VDD=3.3V to CLK stable			10	ms
Maximum Absolute Jitter, short term			±100		ps
One sigma jitter			25		ps

Note: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components/ Application Information

The ICS548-05 requires a minimum number of external components for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD and GND on pins 3 and 5, as close to the ICS548-05 as possible. Other VDDs can be connected to pin 3. A series termination resistor of 33 Ω may be used for each clock output. If REFOUT is not used, then REFEN should be connected to ground. The input crystal must be connected as close to the chip as possible. The input crystal should be fundamental mode, parallel resonant. For exact accuracy of the output frequencies, the crystal can be tuned with two identical capacitors to ground, as shown on the block diagram. The value of these two crystal caps should be equal to $(C_L-6)*2$, where C_L is the crystal load (or correlation) capacitance. For a clock input, leave X2 unconnected (floating).

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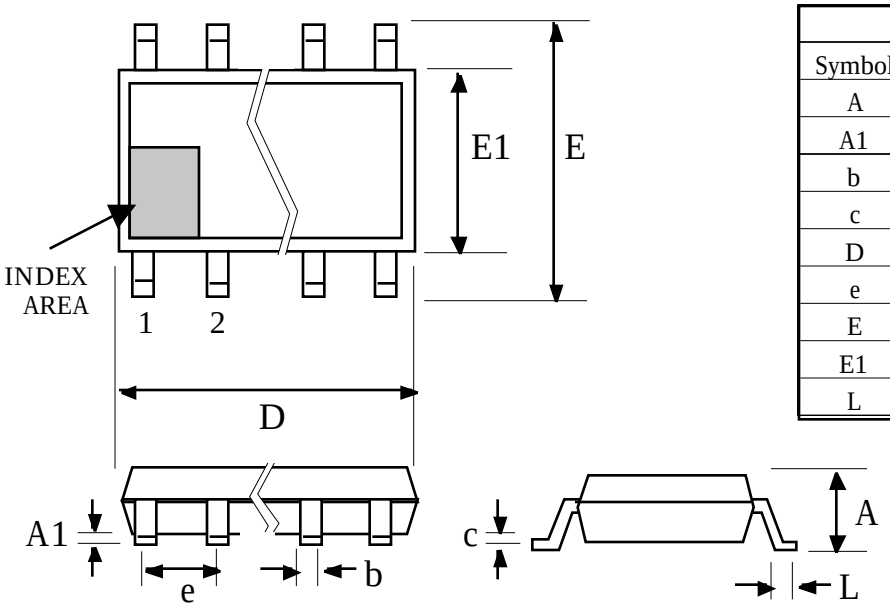
Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC publication no. 95.)



16 pin TSSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	--	0.047	--	1.19
A1	0.002	0.006	0.05	0.15
b	0.007	0.012	0.18	0.30
c	0.0035	0.008	0.09	0.20
D	0.193	0.201	4.90	5.11
e	.025 BSC		0.65 BSC	
E	.252 BSC		6.40 BSC	
E1	0.169	0.177	4.29	4.50
L	0.018	0.030	0.46	0.76

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
ICS548G-05	548G-05	tubes	16 pin TSSOP	0-70 °C
ICS548G-05T	548G-05	tape and reel	16 pin TSSOP	0-70 °C