IS25C02
IS25C04

ISSI®

2,048/4,096-BIT SPI SERIAL ELECTRICALLY ERASABLE PROM

Advanced Information
February 2004

FEATURES

- Serial Peripheral Interface (SPI) Compatible
  — Supports SPI Modes 0 (0,0) and 3 (1,1)
- Low power CMOS
  — Active current less than 3.0 mA (2.5V)
  — Standby current less than 1 µA (2.5V)
- Low-voltage Operation
  — Vcc = 2.5V to 5.5V -3
  — Vcc = 1.8V to 5.5V -2
- Block Write Protection
  — Protect 1/4, 1/2, or Entire Array
- 16 byte page write mode
  — Partial page writes allowed
- 10 MHz Clock Rate (5V)
- Self timed write cycles (5 ms Typical)
- High-reliability
  — Endurance: 1 million cycles per byte
  — Data retention: 100 years
- 8-pin PDIP and 8-pin SOIC packages are available

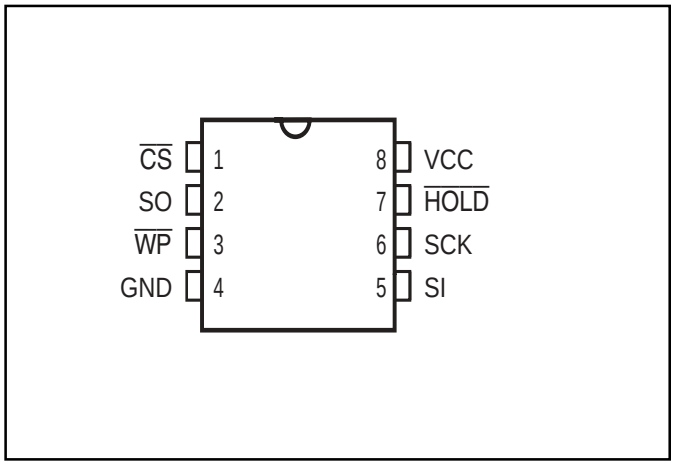
DESCRIPTION

The IS25C02 and IS25C04 are electrically erasable PROM devices that use the Serial Peripheral Interface (SPI) for communications. The IS25C02 is 2Kbit (256x 8) and the IS25C04 is 4Kbit (512x 8). The IS25C02/04 EEPROMs are offered in wide operating voltages of 1.8V to 5.5V and 2.5V to 5.5V compatible with most application voltages. ISSI designed the IS25C02/04 to be an efficient SPI EEPROM solution. The devices are packaged in 8-pin PDIP and 8-pin SOIC.

The functional features of the IS25C02/04 allow them to be among the most advanced serial non-volatile memories available. Each device has a Chip-Select ($\overline{CS}$) pin, and a 3-wire interface of Serial Data In (SI), Serial Data Out (SO), and Serial Clock (SCK). While the 3-wire interface of the IS25C02/04 provides for high-speed access, a $\overline{HOLD}$ pin allows the memories to ignore the interface in a suspended state; later the $\overline{HOLD}$ pin re-activates communication without re-initializing the serial sequence. A Status Register facilitates a flexible write protection mechanism, and a device-ready bit ($\overline{RDY}$).

PIN CONFIGURATION

8-Pin DIP and SOIC



PIN DESCRIPTIONS

CS	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power
WP	Write Protect
HOLD	Suspends Serial Input
NC	No Connect

PIN DESCRIPTIONS

Serial Clock (SCK): This timing signal provides synchronization between the microcontroller and IS25C02/04. Op-Codes, byte addresses, and data are latched on SI with a rising edge of the SCK. Data on SO is refreshed on the falling edge of SCK for SPI modes (0,0) and (1,1).

Serial Data Input (SI): This is the input pin for all data that the IS25C02/04 is required to receive.

Serial Data Output (SO): This is the output pin for all data transmitted from the IS25C02/04.

Chip Select (CS): The CS pin activates the device. Upon power-up, CS should follow Vcc. When the device is to be enabled for instruction input, the signal requires a High-to-Low transition. While CS is stable Low, the master and slave will communicate via SCK, SI, and SO signals. Upon completion of communication, CS must be driven High. At this moment, the slave device may start its internal write cycle. When CS is high, the device enters a power-saving standby mode, unless an internal write operation is underway. During this mode, the SO pin becomes high impedance.

Write Protect (WP): The purpose of this input signal is to initiate Hardware Write Protection mode. This mode prevents the 256/512 byte array or the Status Register from being altered. To cause Hardware Write Protection, WP must be Low. WP may be hardwired to Vcc or GND.

HOLD (HOLD): This input signal is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). Together with Chip Select, the HOLD signal allows multiple slaves to share the bus. The HOLD signal transitions must occur only when SCK is Low, and be held stable during SCK transitions. (See Figure 8 for Hold timing) To disable this feature, HOLD may be hardwired to Vcc.

SERIAL INTERFACE DESCRIPTION

MASTER: The device that provides a clock signal.

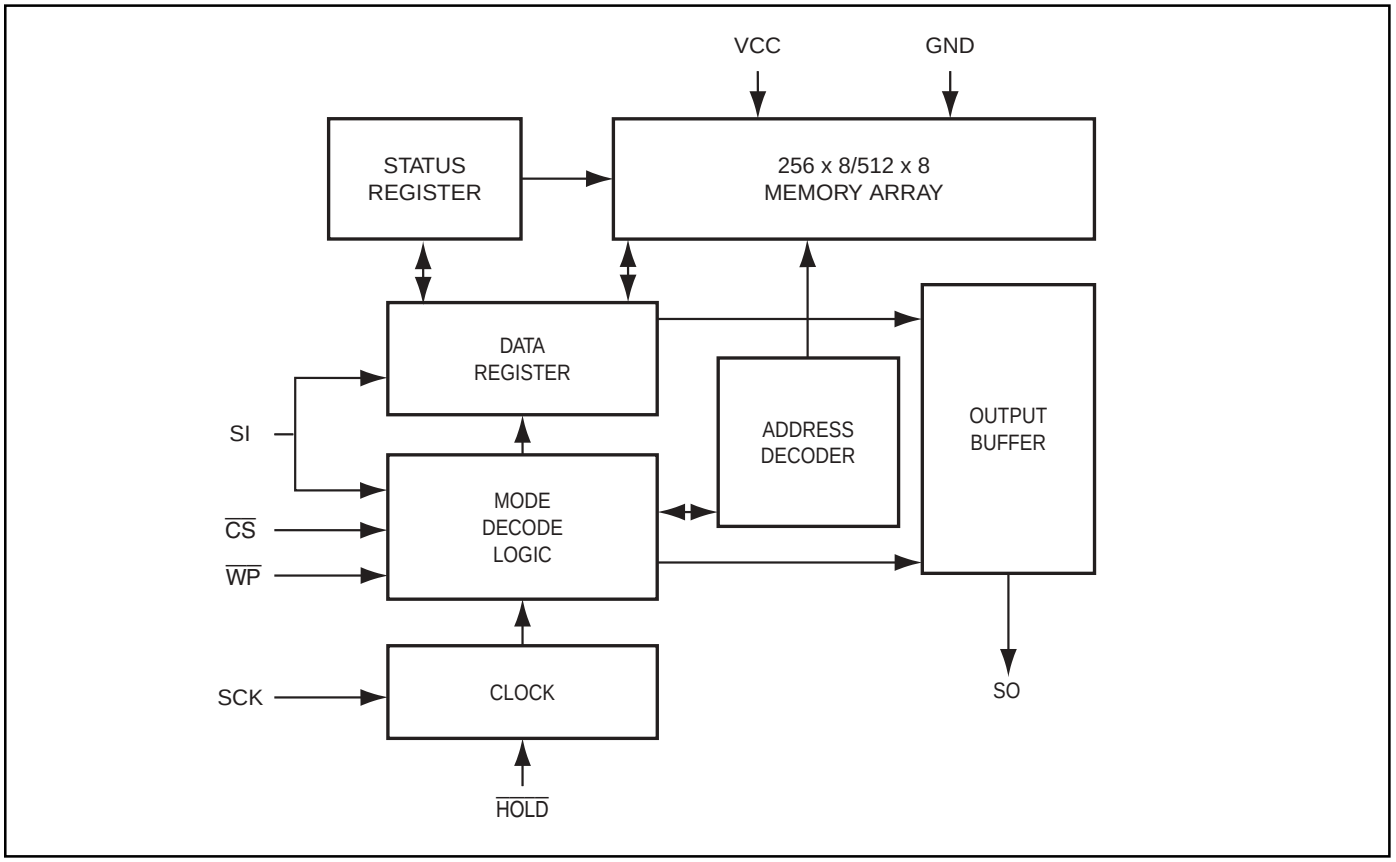
SLAVE: The IS25C02/04 is a slave because the clock signal is an input.

TRANSMITTER/RECEIVER: The IS25C02/04 has both data input (SI) and data output (SO).

MSB: The most significant bit. It is always the first bit transmitted or received.

OP-CODE: The first byte transmitted to the slave following CS transition to LOW. If the OP-CODE is a valid member of the IS25C02/04 instruction set (Table 3), then it is decoded appropriately. If the OP-CODE is not valid, and the SO pin remains in high impedance.

BLOCK DIAGRAM



STATUS REGISTER

The status register contains 8-bits for write protection control and write status. (See Table 1). It is the only region of memory other than the main array that is accessible by the user.

Table 1. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Note: X = Don't care bit.

The Status Register is Read-Only if either: a) Hardware Write Protection is enabled or b) WEN is set to 1. If neither is true, it can be modified by a valid instruction.

Ready ($\overline{RDY}$), Bit 0: When $\overline{RDY}$ = 1, it indicates that the device is busy with a write cycle. $\overline{RDY}$ = 0 indicates that the device is ready for an instruction. If $\overline{RDY}$ = 1, the only command that will be handled by the device is Read Status Register.

Write Enable (WEN), Bit 1: This bit represents the status of device write protection. If WEN = 0, the Status Register and the entire array is protected from modification, regardless of the setting of $\overline{WP}$ pin or block protection. The only way to set WEN to 1 is via the Write Enable command (WREN). WEN is reset to 0 upon power-up, successful completion of Write, WRDI, WRSR, or $\overline{WP}$ being Low.

Block Protect (BP1, BP0), Bits 2-3: Together, these bits represent one of four block protection configurations implemented for the memory array. (See Table 2 for details.)
BP0 and BP1 are non-volatile cells similar to regular array cells, and factory programmed to 0. The block of memory defined by these bits is always protected, regardless of the setting of $\overline{WP}$ or WEN.

Table 2. Block Protection

	Status Register Bits		Array Addresses Protected	
Level	**BP1**	**BP0**	**IS25C02**	**IS25C04**
0	0	0	None	None
1(1/4)	0	1	C0h FFh	180h 1FFh
2(1/2)	1	0	80h FFh	100h 1FFh
3(All)	1	1	00h FFh	000h 1FFh

Don't Care, Bits 4-7: Each of these bits can receive either 0 or 1, but values will not be retained. When these bits are read from the register, they are always 0.

DEVICE OPERATION

The operations of the IS25C02/04 are controlled by a set of instructions that are clocked-in serially SI pin. (See Table 3). To begin an instruction, the chip select ($\overline{CS}$) should be dropped Low. Subsequently, each Low-to-High transition of the clock (SK) will latch a stable value on the SI pin. After the 8-bit op-code, it may be appropriate to continue to input an address or data to SI, or to output data from SO. During data output, values appear on the falling edge of SK. All bits are transferred with MSB first. Upon the last bit of communication, but prior to any following Low-to-High transition of SK, $\overline{CS}$ should be raised High to end the transaction. The device then would enter Standby Mode if no internal programming were underway.

Table 3. Instruction Set

Name	Op-code	Operation	Address	Data(SI)	Data (SO)
WREN	0000 X110	Set Write Enable Latch	-	-	-
WRDI	0000 X100	Reset Write Enable Latch	-	-	-
RDSR	0000 X101	Read Status Register	-	-	D_7-D_0,...
WRSR	0000 X001	Write Status Register	-	D_7-D_0	-
READ	0000 $A_8$011	Read Data from Array	A_7-A_0	-	D_7-D_0,...
WRITE	0000 $A_8$010	Write Data to Array	A_7-A_0	D_7-D_0,...	-

1. X = Don't care bit. For consistency, it is best to use "0".
2. Some address bits are don't care. See Table 5.
3. If the bits clocked-in for an op-code are invalid, SO remains high impedance, and upon CS going High there is no affect. A valid op-code with an invalid number of bits clocked-in for address or data will cause an attempt to modify the array or Status Register to be ignored.

WRITE ENABLE (WREN)

When Vcc is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR), or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a WREN instruction is necessary to set WEN to 1. (See Figure 2 for timing).

WRITE DISABLE (WRDI)

The device can be completely protected from modification by resetting WEN to 0 through the WRDI instruction. (See Figure 3 for timing).

READ STATUS REGISTER (RDSR)

The Read Status instruction indicates the status of the Block Protection setting (see Table 2), the Write Enable state, and the $\overline{RDY}$ status. RDSR is the only instruction accepted when a write cycle is underway. It is recommended that the status of $\overline{RDY}$ be checked, especially prior to an attempted modification of data. The 8 bits of the Status Register can be repeatedly output on SO after the initial Op-code. (See Figure 4 for timing).

WRITE STATUS REGISTER (WRSR)

This instruction lets the user choose a Block Protection setting. The values of the other data bits incorporated into WRSR can be 0 or 1, and are not stored in the Status Register. WRSR will be ignored unless both the following are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled. (See Table 4 for details). Except for the $\overline{RDY}$ status, the values in the Status Register remain unchanged until the moment when the write cycle is complete and the register is updated. Once successfully completed, WEN is reset for complete chip write protection. (See Figure 5 for timing).

READ DATA (READ)

This instruction begins with the op-code and the 8-bit address, and causes the selected data byte to be shifted out on SO. Following this first data byte, additional sequential bytes are output. If the data byte in the highest address is output, the address rolls-over to the lowest address in the array, and the output could loop indefinitely. At any time, a rising $\overline{CS}$ signal completes the operation. (See Figure 6 for timing).

WRITE DATA (WRITE)

The WRITE instruction begins with the op-code, the 8-bit address of the first byte to be modified, and the first data byte. Additional data bytes may be written sequentially to the array after the first byte. Each WRITE instruction can affect the contents of a 16 byte page, but no more. The page begins at address XXXX 0000, and ends with XXXX 1111. If the last byte of the page is input, the address rolls over to the beginning of the same page. More than 16 data bytes can be input during the same instruction, but upon a completed write cycle, a page would only contain the last 16 bytes.

The region of the array defined within Block Protection cannot be modified as long as that block configuration is selected. The region of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction occur prior to WRITE. In addition, if Hardware Write Protection is enabled, the memory array cannot be modified. Once Write is successfully completed, WEN is reset for complete chip write protection. (See Figure 7 for timing).

Table 5. Address Key

Name	IS25C02	IS25C04
A_N	$A_{7-}A_0$	$A_{8-}A_0$
Don't Care Bits	A_8	-

Table 4. Write Protection

$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register
0	Enabled	X	Read-only	Read-only	Read-only
1	Not Enabled	0	Read-only	Read-only	Read-only
1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	–0.5 to + 6.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (IS25C04-2 and IS25C02-2)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	1.8V to 5.5V
Industrial	–40°C to +85°C	1.8V to 5.5V

OPERATING RANGE (IS25C04-3 and IS25C02-3)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.5V to 5.5V
Industrial	–40°C to +85°C	2.5V to 5.5V
Automotive	–40°C to +125°C	2.5V to 5.5V

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for Commercial, T_A = –40°C to +85°C for Industrial, T_A = –40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OL1}	Output LOW Voltage	V_{CC} = 5V, I_{OL} = 2 mA	—	0.4	V
V_{OL2}	Output LOW Voltage	V_{CC} = 2.5V, I_{OL} = 1.5 mA	—	0.4	V
V_{OL3}	Output LOW Voltage	V_{CC} = 1.8V, I_{OL} = 0.15 mA	—	0.2	V
V_{OH1}	Output HIGH Voltage	V_{CC} = 5V, I_{OH} = -2 mA	0.8 x V_{CC}	—	V
V_{OH2}	Output HIGH Voltage	V_{CC} = 2.5V, I_{OH} = -0.4mA	0.8 x V_{CC}	—	V
V_{OH3}	Output HIGH Voltage	V_{CC} = 1.8V, I_{OH} = -0.1mA	0.8 x V_{CC}	—	V
V_{IH}	Input HIGH Voltage		0.7xV_{CC}	V_{CC} + 1	V
V_{IL}	Input LOW Voltage		-0.3	0.3 x V_{CC}	V
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-2	2	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, $\overline{CS}$ = V_{CC}	-2	2	µA

POWER SUPPLY CHARACTERISTICS

T_A = 0°C to +70°C for Commercial, T_A = –40°C to +85°C for Industrial.

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Operating Current	Read/Write at 10 MHz (Vcc = 5V)	—	5.0	mA
I_{CC2}	Vcc Operating Current	Read/Write at 5 MHz (Vcc = 2.5V)	—	3.0	mA
I_{CC3}	Vcc Operating Current	Read/Write at 2 MHz (Vcc = 1.8V)	—	1.0	mA
I_{SB1}	Standby Current	Vcc = 5.0V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	2	µA
I_{SB2}	Standby Current	Vcc = 2.5V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	1	µA
I_{SB3}	Standby Current	Vcc = 1.8V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	0.5	µA

POWER SUPPLY CHARACTERISTICS

T_A = –40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Operating Current	Read/Write at 5 MHz (Vcc = 5V)	—	4.0	mA
I_{CC2}	Vcc Operating Current	Read/Write at 5 MHz (Vcc = 2.5V)	—	3.0	mA
I_{SB1}	Standby Current	Vcc = 5.0V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	5.0	µA
I_{SB2}	Standby Current	Vcc =2.5V, V_{IN} = V_{CC} or GND $\overline{CS}$ = Vcc	—	2.0	µA

AC Characteristics

T_A = 0°C to +70°C for Commercial, T_A = –40°C to +85°C for Industrial.

Symbol	Parameter	1.8V to 5.5V Min	1.8V to 5.5V Max	2.5V to 5.5V Min	2.5V to 5.5V Max	4.5V to 5.5V Min	4.5V to 5.5V Max	Units
f_{SCK}	SCK Clock Frequency	0	2	0	5	0	10	MHz
t_{RI}	Input Rise Time	—	2	—	2	—	2	µs
t_{FI}	Input Fall Time	—	2	—	2	—	2	µs
t_{WH}	SCK High Time	200	—	90	—	40	—	ns
t_{WL}	SCK Low Time	200	—	90	—	40	—	ns
t_{CS}	$\overline{CS}$ High Time	200	—	100	—	40	—	ns
t_{CSS}	$\overline{CS}$ Setup Time	200	—	90	—	15	—	ns
t_{CSH}	$\overline{CS}$ Hold Time	200	—	90	—	25	—	ns
t_{SU}	Data In Setup Time	40	—	20	—	15	—	ns
t_H	Data In Hold Time	50	—	30	—	15	—	ns
t_{HD}	$\overline{Hold}$ Setup Time	100	—	50	—	25	—	ns
t_{CD}	$\overline{Hold}$ Hold Time	100	—	50	—	25	—	ns
t_V	Output Valid	0	150	0	60	0	25	ns
t_{HO}	Output Hold Time	0	—	0	—	0	—	ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	0	100	0	50	0	25	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	—	250	—	100	—	25	ns
t_{DIS}	Output Disable Time	—	250	—	100	—	25	ns
t_{WC}	Write Cycle Time	—	10	—	5	—	5	ms

C_L = 100pF

AC Characteristics

T_A = –40°C to +125°C for Automotive.

Symbol	Parameter	2.5V to 5.5V Min	2.5V to 5.5V Max	4.5V to 5.5V Min	4.5V to 5.5V Max	Units
f_{SCK}	SCK Clock Frequency	0	5	0	10	MHz
t_{RI}	Input Rise Time	—	2	—	2	µs
t_{FI}	Input Fall Time	—	2	—	2	µs
t_{WH}	SCK High Time	90	—	40	—	ns
t_{WL}	SCK Low Time	90	—	40	—	ns
t_{CS}	$\overline{CS}$ High Time	100	—	40	—	ns
t_{CSS}	$\overline{CS}$ Setup Time	90	—	15	—	ns
t_{CSH}	$\overline{CS}$ Hold Time	90	—	25	—	ns
t_{SU}	Data In Setup Time	20	—	15	—	ns
t_H	Data In Hold Time	30	—	15	—	ns
t_{HD}	$\overline{Hold}$ Setup Time	50	—	25	—	ns
t_{CD}	$\overline{Hold}$ Hold Time	50	—	25	—	ns
t_V	Output Valid	0	60	0	25	ns
t_{HO}	Output Hold Time	0	—	0	—	ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	0	50	0	25	ns
t_{HZ}	$\overline{Hold}$ to Output High Z	—	100	—	25	ns
t_{DIS}	Output Disable Time	—	100	—	25	ns
t_{WC}	Write Cycle Time	—	5	—	5	ms

C_L = 100pF

TIMING DIAGRAMS

Figure 1. Synchronous Data Timing

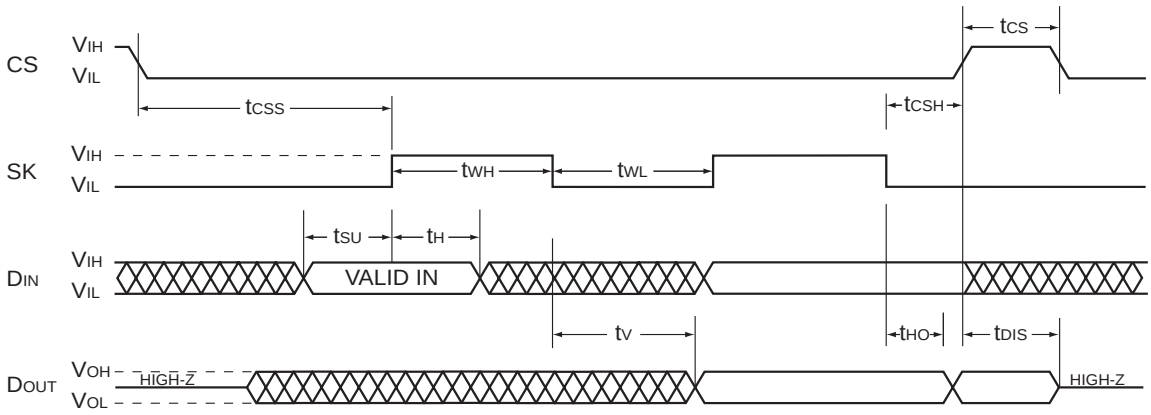


Figure 2. WREN Timing

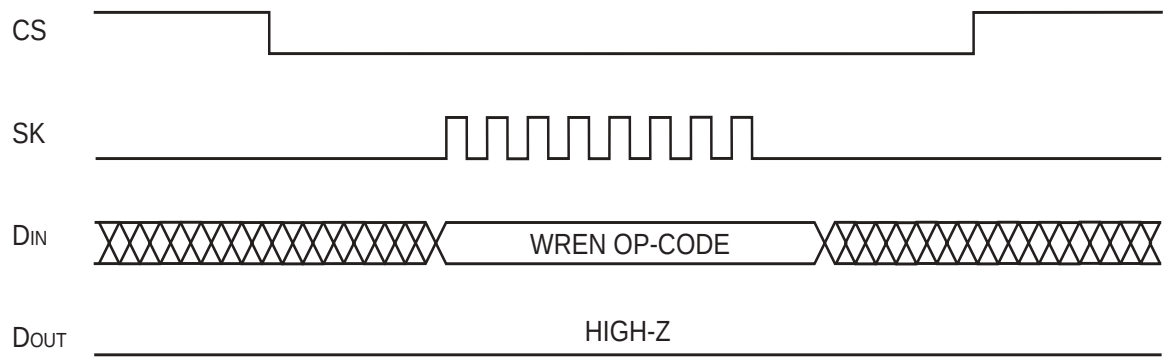


Figure 3. WRDI Timing

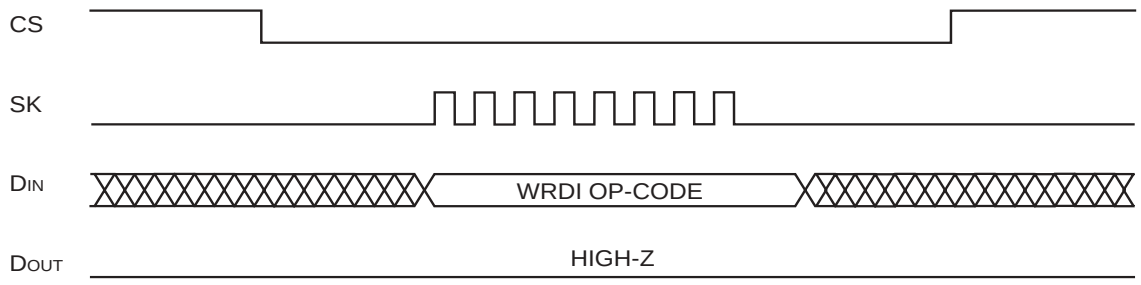


Figure 4. RDSR Timing

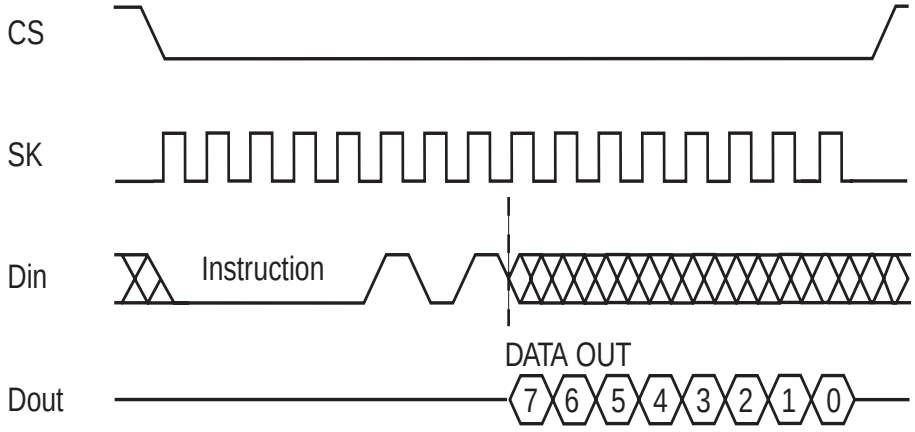


Figure 5. WRSR Timing

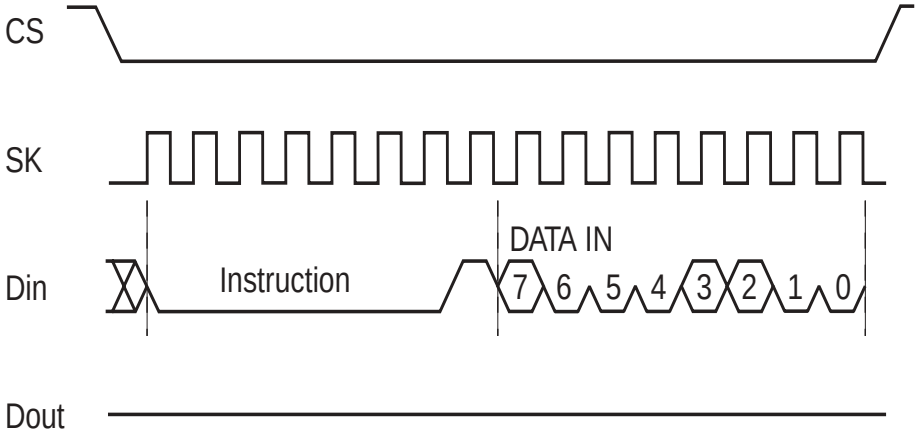


Figure 6. READ Timing

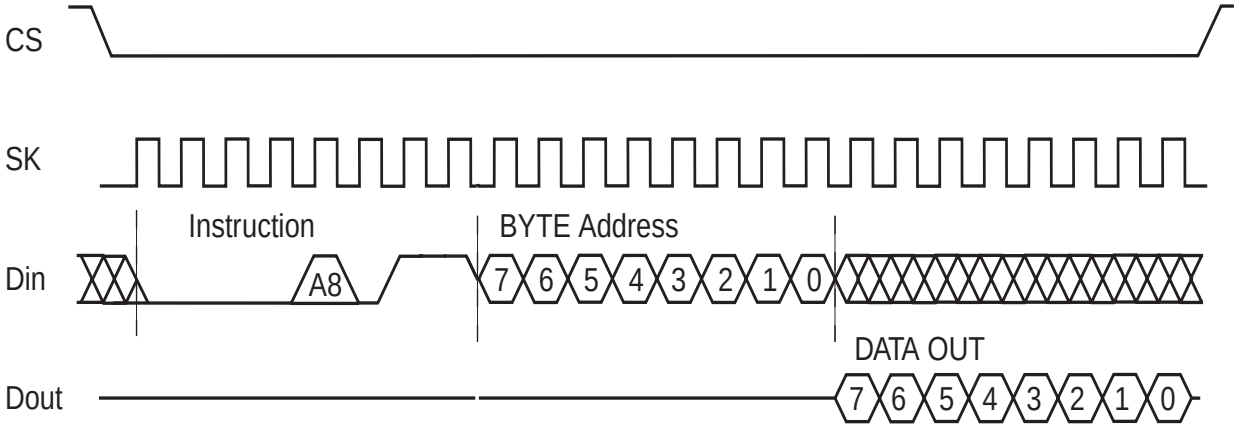


Figure 7. WRITE Timing

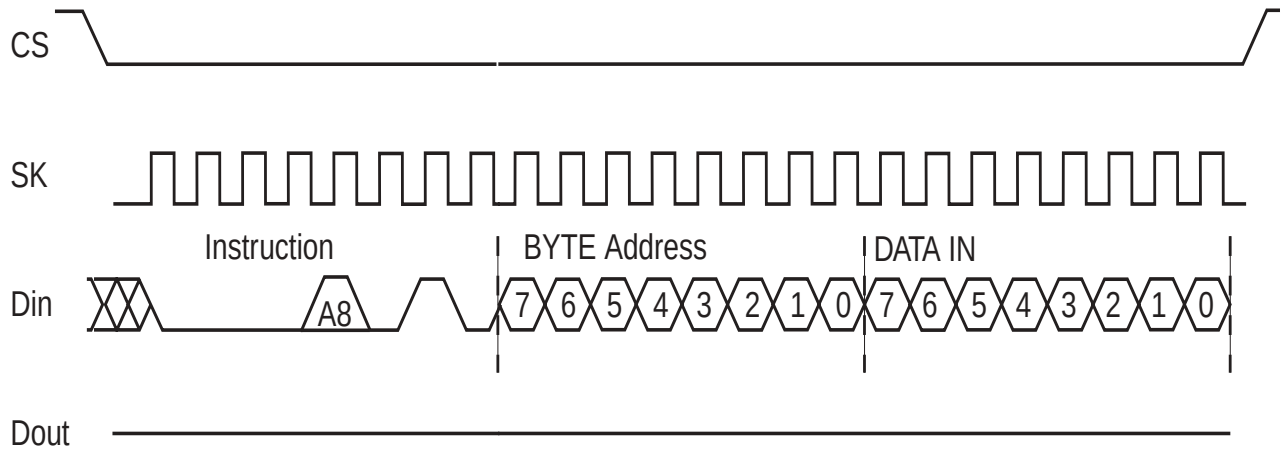
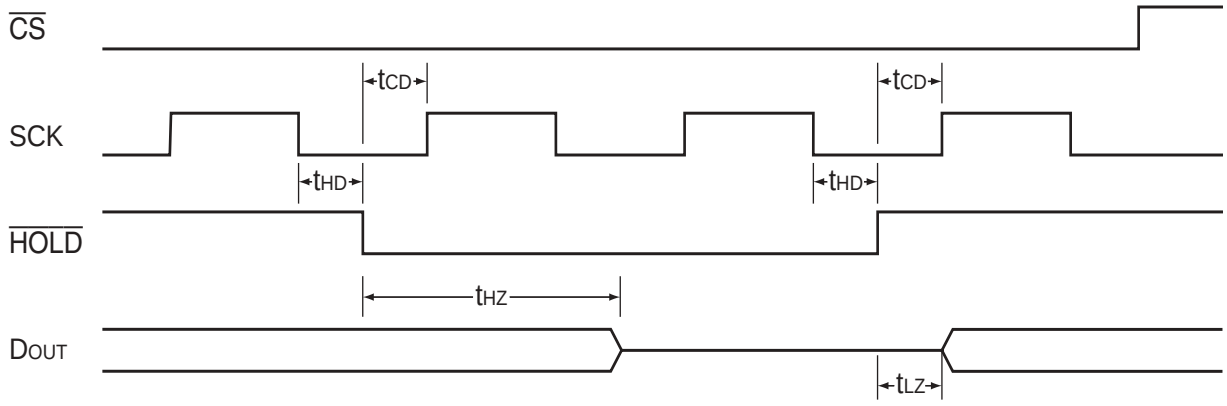


Figure 8. $\overline{\text{HOLD}}$ Timing



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Voltage Range	Part Number	Package
2 MHz	1.8V to 5.5V	IS25C02-2P IS25C02-2G	300-mil Plastic DIP Small Outline (JEDEC STD)
2 MHz	1.8V to 5.5V	IS25C04-2P IS25C04-2G	300-mil Plastic DIP Small Outline (JEDEC STD)
5 MHz	2.5V to 5.5V	IS25C02-3P IS25C02-3G	300-mil Plastic DIP Small Outline (JEDEC STD)
5 MHz	2.5V to 5.5V	IS25C04-3P IS25C04-3G	300-mil Plastic DIP Small Outline (JEDEC STD)

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Frequency	Voltage Range	Part Number	Package
2 MHz	1.8V to 5.5V	IS25C02-2PI IS25C02-2GI	300-mil Plastic DIP Small Outline (JEDEC STD)
2 MHz	1.8V to 5.5V	IS25C04-2PI IS25C04-2GI	300-mil Plastic DIP Small Outline (JEDEC STD)
5 MHz	2.5V to 5.5V	IS25C02-3PI IS25C02-3GI	300-mil Plastic DIP Small Outline (JEDEC STD)
5 MHz	2.5V to 5.5V	IS25C04-3PI IS25C04-3GI	300-mil Plastic DIP Small Outline (JEDEC STD)

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