IS93C76A   IS93C86A

ISSI®

8,192/16,384-BIT SERIAL ELECTRICALLY ERASABLE PROM
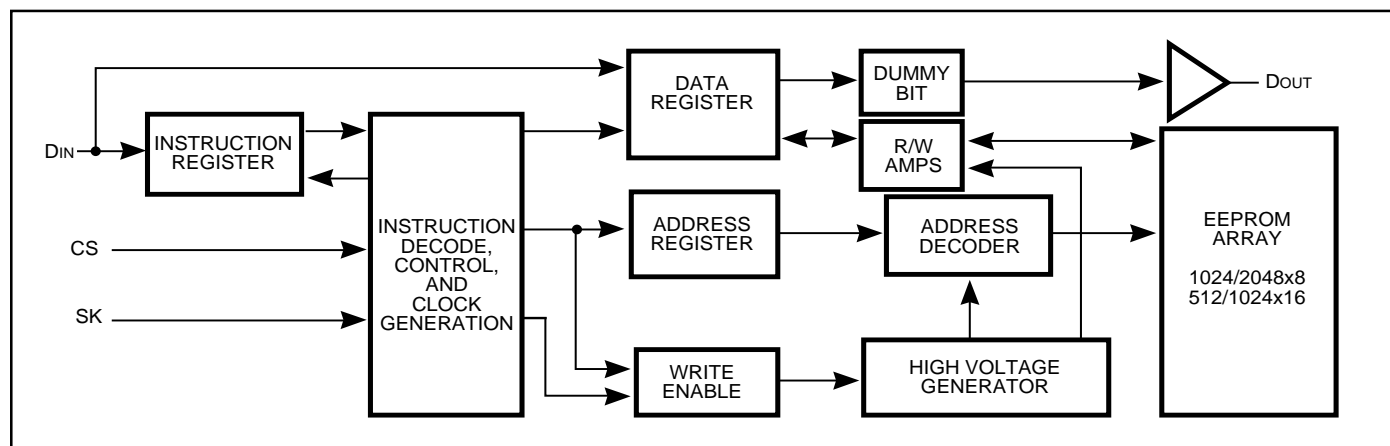
Advanced
November 2003

FEATURES

- Industry-standard Microwire Interface
  — Non-volatile data storage
  — Low voltage operation:
    Vcc = 1.8V to 5.5V -2
    Vcc = 2.5V to 5.5V -3
  — Full TTL compatible inputs and outputs
  — Auto increment for efficient data dump
- User Configured Memory Organization
  — By 16-bit or by 8-bit
- Hardware and software write protection
  — Defaults to write-disabled state at power-up
  — Software instructions for write-enable/disable
- Enhanced low voltage CMOS E^{2}PROM technology
- Versatile, easy-to-use Interface
  — Self-timed programming cycle
  — Automatic erase-before-write
  — Programming status indicator
  — Word and chip erasable
  — Chip select enables power savings
- Durable and reliable
  — 40-year data retention after 1M write cycles
  — 1 million write cycles
  — Unlimited read cycles
  — Schmitt-trigger and filtered inputs
- Industrial and Automotive Temperature Grade

DESCRIPTION

IS93C76A/86A are 8kb/16kb non-volatile, ISSI ® serial EEPROMs. They are fabricated using an enhanced CMOS design and process. IS93C76A/86A contains power-efficient read/write memory, and organization of either 1,024/2,048 bytes of 8 bits or 512/1,024 words of 16 bits. When the ORG pin is connected to Vcc or left unconnected, x16 is selected; when it is connected to ground, x8 is selected.

An instruction set defines the operation of the devices, including read, write, and mode-enable functions. To protect against inadvertent data modification, all erase and write instructions are accepted only while the device are write-enabled. A selected x8 byte or x16 word can be modified with a single WRITE or ERASE instruction. Additionally, the two instructions WRITE ALL or ERASE ALL can program an entire array. Once a device begins its self-timed program procedure, the data out pin (Dout) can indicate the READY/$\overline{BUSY}$ status by raising chip select (CS). The self-timed write cycle includes an automatic erase-before-write capability. The devices can output any number of consecutive bytes/words using a single READ instruction.
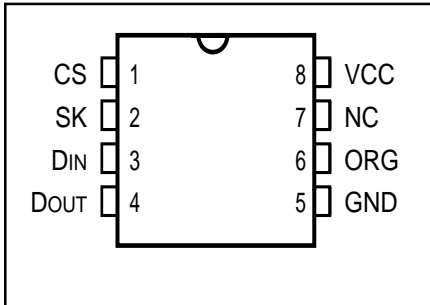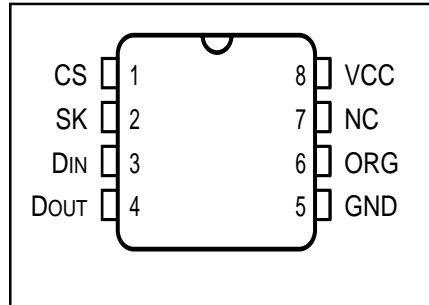
FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATIONS

8-Pin DIP, 8-Pin TSSOP

CS	1	8	VCC
SK	2	7	NC
DIN	3	6	ORG
DOUT	4	5	GND

8-Pin JEDEC SOIC "GR"

CS	1	8	VCC
SK	2	7	NC
DIN	3	6	ORG
DOUT	4	5	GND

PIN DESCRIPTIONS

CS	Chip Select
SK	Serial Data Clock
DIN	Serial Data Input
DOUT	Serial Data Output
ORG	Organization Select
NC	Not Connected
Vcc	Power
GND	Ground

Applications

The IS93C76A/86A are very popular in many applications which require low-power, low-density storage. Applications using these devices include industrial controls, networking, and numerous other consumer electronics.

Endurance and Data Retention

The IS93C76A/86A are designed for applications requiring up to 1M programming cycles (WRITE, WRALL, ERASE and ERAL). They provide 40 years of secure data retention without power after the execution of 1M programming cycles.

Device Operations

The IS93C76A/86A are controlled by a set of instructions which are clocked-in serially on the Din pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the Din value must be stable at either LOW or HIGH. Each instruction begins with a start bit of the logical "1" or HIGH. Following this are the opcode (2 bits), address field (10 or 11 bits), and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock-speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

Read (READ)

The READ instruction is the only instruction that outputs serial data on the Dout pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a serial shift register. (Please note that one logical "0" bit precedes the actual 8 or 16-bit output data string.) The output on Dout changes during the low-to-high transitions of SK (see Figure 3).

Low Voltage Read

The IS93C76A/86A are designed to ensure that data read operations are reliable in low voltage environments. They provide accurate operation with Vcc as low as 1.8V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the IS93C76A/86A are designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8 or16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When Vcc is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until Vcc is removed. (See Figure 4.) (Note: Chip select must remain LOW until Vcc reaches its operational value.)

Write (WRITE)

The WRITE instruction includes 8 or 16 bits of data to be written into the specified register. After the last data bit has been applied to D$_{IN}$, and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN).

If CS is brought HIGH, after a minimum wait of 200 ns (5V operation) after the falling edge of CS (t$_{CS}$) D$_{OUT}$ will indicate the READY/$\overline{BUSY}$ status of the chip. Logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction (see Figure 5). The READY/$\overline{BUSY}$ status will not be available if: a) The CS input goes HIGH after the end of the self-timed programming cycle, t$_{WP}$; or b) Simultaneously CS is HIGH, Din is HIGH, and SK goes HIGH, which clears the status flag.

Write All (WRALL)

The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 200 ns (t$_{CS}$), the D$_{OUT}$ pin indicates the READY/$\overline{BUSY}$ status of the chip (see Figure 6). Vcc is required to be above 4.5V for WRALL to function properly.

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

Erase Register (ERASE)

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t$_{CS}$, will cause D$_{OUT}$ to indicate the READ/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction (see Figure 8).

Erase All (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1" (see Figure 9). Vcc is required to be above 4.5V for ERALL to function properly.

INSTRUCTION SET - IS93C76A (8kb)

Instruction[2]	Start Bit	OP Code	8-bit Organization (ORG = GND)		16-bit Organization (ORG = Vcc)	
			Address [1]	Input Data	Address [1]	Input Data
READ	1	10	x(A_9-A_0)	—	x(A_8-A_0)	—
WEN (Write Enable)	1	00	11x xxxx xxxx	—	11 xxxx xxxx	—
WRITE	1	01	x(A_9-A_0)	(D_7-D_0)	x(A_8-A_0)	(D_{15}-D_0)
WRALL (Write All Registers)	1	00	01x xxxx xxxx	(D_7-D_0)	01 xxxx xxxx	(D_{15}-D_0)
WDS (Write Disable)	1	00	00x xxxx xxxx	—	00 xxxx xxxx	—
ERASE	1	11	x(A_9-A_0)	—	x(A_8-A_0)	—
ERAL (Erase All Registers)	1	00	10x xxxx xxxx	—	10 xxxx xxxx	—

Notes:
1. x = Don't care bit.
2. If the number of bits clocked-in does not match the number corresponding to a selected command, all extra trailing bits are ignored, and WRITE, WRALL, ERASE, ERAL, WEN, and WDS instructions are rejected, but READ is accepted.

INSTRUCTION SET - IS93C86A (16kb)

Instruction[2]	Start Bit	OP Code	8-bit Organization (ORG = GND)		16-bit Organization (ORG = Vcc)	
			Address [1]	Input Data	Address [1]	Input Data
READ	1	10	(A_{10}-A_0)	—	(A_9-A_0)	—
WEN (Write Enable)	1	00	11x xxxx xxxx	—	11 xxxx xxxx	—
WRITE	1	01	(A_{10}-A_0)	(D_7-D_0)	(A_9-A_0)	(D_{15}-D_0)
WRALL (Write All Registers)	1	00	01x xxxx xxxx	(D_7-D_0)	01 xxxx xxxx	(D_{15}-D_0)
WDS (Write Disable)	1	00	00x xxxx xxxx	—	00 xxxx xxxx	—
ERASE	1	11	(A_{10}-A_0)	—	(A_9-A_0)	—
ERAL (Erase All Registers)	1	00	10x xxxx xxxx	—	10 xxxx xxxx	—

Notes:
1. x = Don't care bit.
2. If the number of bits clocked-in does not match the number corresponding to a selected command, all extra trailing bits are ignored, and WRITE, WRALL, ERASE, ERAL, WEN, and WDS instructions are rejected, but READ is accepted.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{GND}	Voltage with Respect to GND	−0.3 to +6.5	V
T_{BIAS}	Temperature Under Bias (Industrial)	−40 to +85	°C
T_{BIAS}	Temperature Under Bias (Automotive)	−40 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Industrial	−40°C to+85°C	1.8V to 5.5V or 2.5V to 5.5V
Automotive	−40°C to+125°C	2.5V to 5.5V

CAPACITANCE

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	5	pF

DC ELECTRICAL CHARACTERISTICS

T_A = −40°C to +85°C for Industrial and −40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
V_{OL2}	Output LOW Voltage	$I_{OL}=100\,\mu A$	1.8V to 5.5V	—	0.2	V
V_{OL}	Output LOW Voltage	$I_{OL}=100\,\mu A$	2.5V to 5.5V	—	0.2	V
V_{OL1}	Output LOW Voltage	$I_{OL}=2.1mA$	4.5V to 5.5V	—	0.4	V
V_{OH}	Output HIGH Voltage	$I_{OH}=-100\,\mu A$	1.8V to 5.5V	$V_{CC}-0.2$	—	V
V_{OH2}	Output HIGH Voltage	$I_{OH}=-100\,\mu A$	2.5V to 5.5V	$V_{CC}-0.2$	—	V
V_{OH1}	Output HIGH Voltage	$I_{OH}=-400\,\mu A$	4.5V to 5.5V	2.4	—	V
V_{IH}	Input HIGH Voltage		1.8V to 5.5V 2.5V to 5.5V 4.5V to 5.5V	$0.7\times V_{CC}$ $0.7\times V_{CC}$ 2.0	$V_{CC}+1$ $V_{CC}+1$ $V_{CC}+1$	V
V_{IL}	Input LOW Voltage		1.8V to 5.5V 2.5V to 5.5V 4.5V to 5.5V	−0.3 −0.3 −0.3	$0.2\times V_{CC}$ $0.2\times V_{CC}$ 0.8	V
I_{LI}	Input Leakage	$V_{IN}=0V$ to V_{CC} (CS, SK, D_{IN}, ORG)		0	2.5	μA
I_{LO}	Output Leakage	$V_{OUT}=0V$ to V_{CC}, CS = 0V		0	2.5	μA

Notes:

Automotive grade devices in this table are tested with Vcc = 2.5V to 5.5V and 4.5V to 5.5V. Operations with Vcc <2.5V is not specified.

POWER SUPPLY CHARACTERISTICS

T_A = −40°C to +85°C for Industrial, and −40°C to +125°C for Automotive.

Symbol	Parameter	Test Conditions	Vcc	Min.	Typ.	Max.	Unit
I_{CC1}	Vcc Read Supply Current	CS = V_{IH}, SK = 1 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels	1.8V 2.5V 5.0V	— — —	TBD TBD TBD	100 100 500	μA μA μA
I_{CC2}	Vcc Write Supply Current	CS = V_{IH}, SK = 1 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels CS = V_{IH}, SK = 2 MHz, CMOS input levels	1.8V 2.5V 5.0V	— — —	TBD TBD TBD	1 1 2	mA mA mA
I_{SB}	Standby Current	CS = V_{IH}, SK = 0V	1.8V 2.5V 5.0V	— — —	TBD TBD TBD	1 2 4	μA μA μA

AC ELECTRICAL CHARACTERISTICS

T_A = −40°C to +85°C for Industrial

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
f_{SK}	SK Clock Frequency		1.8V to 5.5V	0	1	Mhz
			2.5V to 5.5V	0	2	Mhz
			4.5V to 5.5V	0	3	Mhz
t_{SKH}	SK HIGH Time		1.8V to 5.5V	250	—	ns
			2.5V to 5.5V	200	—	ns
			4.5V to 5.5V	200	—	ns
t_{SKL}	SK LOW Time		1.8V to 5.5V	250	—	ns
			2.5V to 5.5V	200	—	ns
			4.5V to 5.5V	100	—	ns
t_{CS}	Minimum CS LOW Time		1.8V to 5.5V	250	—	ns
			2.5V to 5.5V	200	—	ns
			4.5V to 5.5V	200	—	ns
t_{CSS}	CS Setup Time	**Relative to SK**	1.8V to 5.5V	50	—	ns
			2.5V to 5.5V	50	—	ns
			4.5V to 5.5V	50	—	ns
t_{DIS}	Din Setup Time	Relative to SK	1.8V to 5.5V	100	—	ns
			2.7V to 5.5V	50	—	ns
			4.5V to 5.5V	50	—	ns
t_{CSH}	CS Hold Time	Relative to SK	1.8V to 5.5V	0	—	ns
			2.5V to 5.5V	0	—	ns
			4.5V to 5.5V	0	—	ns
t_{DIH}	Din Hold Time	Relative to SK	1.8V to 5.5V	50	—	ns
			2.5V to 5.5V	50	—	ns
			4.5V to 5.5V	50	—	ns
t_{PD1}	Output Delay to "1"	AC Test	1.8V to 5.5V	—	400	ns
			2.5V to 5.5V	—	200	ns
			4.5V to 5.5V	—	100	ns
t_{PD0}	Output Delay to "0"	AC Test	1.8V to 5.5V	—	400	ns
			2.5V to 5.5V	—	200	ns
			4.5V to 5.5V	—	100	ns
t_{SV}	CS to Status Valid	AC Test	1.8V to 5.5V	—	400	ns
			2.5V to 5.5V	—	200	ns
			4.5V to 5.5V	—	200	ns
t_{DF}	CS to Dout in 3-state	AC Test, CS=VIL	1.8V to 5.5V	—	100	ns
			2.5V to 5.5V	—	100	ns
			4.5V to 5.5V	—	100	ns
t_{WP}	Write Cycle Time		1.8V to 5.5V	—	10	ms
			2.5V to 5.5V	—	5	ms
			4.5V to 5.5V	—	5	ms

Notes:

1. C_L = 100pF

AC ELECTRICAL CHARACTERISTICS

T_A = −40°C to +125°C for Automotive

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
f_{SK}	SK Clock Frequency		2.5V to 5.5V	0	2	Mhz
			4.5V to 5.5V	0	3	Mhz
t_{SKH}	SK HIGH Time		2.5V to 5.5V	200	—	ns
			4.5V to 5.5V	200	—	ns
t_{SKL}	SK LOW Time		2.5V to 5.5V	200	—	ns
			4.5V to 5.5V	100	—	ns
t_{CS}	Minimum CS LOW Time		2.5V to 5.5V	200	—	ns
			4.5V to 5.5V	200	—	ns
t_{CSS}	CS Setup Time	Relative to SK	2.5V to 5.5V	50	—	ns
			4.5V to 5.5V	50	—	ns
t_{DIS}	Din Setup Time	Relative to SK	2.5V to 5.5V	50	—	ns
			4.5V to 5.5V	50	—	ns
t_{CSH}	CS Hold Time	Relative to SK	2.5V to 5.5V	0	—	ns
			4.5V to 5.5V	0	—	ns
t_{DIH}	Din Hold Time	Relative to SK	2.5V to 5.5V	50	—	ns
			4.5V to 5.5V	50	—	ns
t_{PD1}	Output Delay to "1"	AC Test	2.5V to 5.5V	—	200	ns
			4.5V to 5.5V	—	100	ns
t_{PD0}	Output Delay to "0"	AC Test	2.5V to 5.5V	—	200	ns
			4.5V to 5.5V	—	100	ns
t_{SV}	CS to Status Valid	AC Test	2.5V to 5.5V	—	200	ns
			4.5V to 5.5V	—	200	ns
t_{DF}	CS to Dout in 3-state	AC Test, CS=VIL	2.5V to 5.5V	—	100	ns
			4.5V to 5.5V	—	100	ns
t_{WP}	Write Cycle Time		2.5V to 5.5V	—	5	ms
			4.5V to 5.5V	—	5	ms

N o t e s :

1. C_L = 100pF

AC WAVEFORMS

FIGURE 2. SYNCHRONOUS DATA TIMING
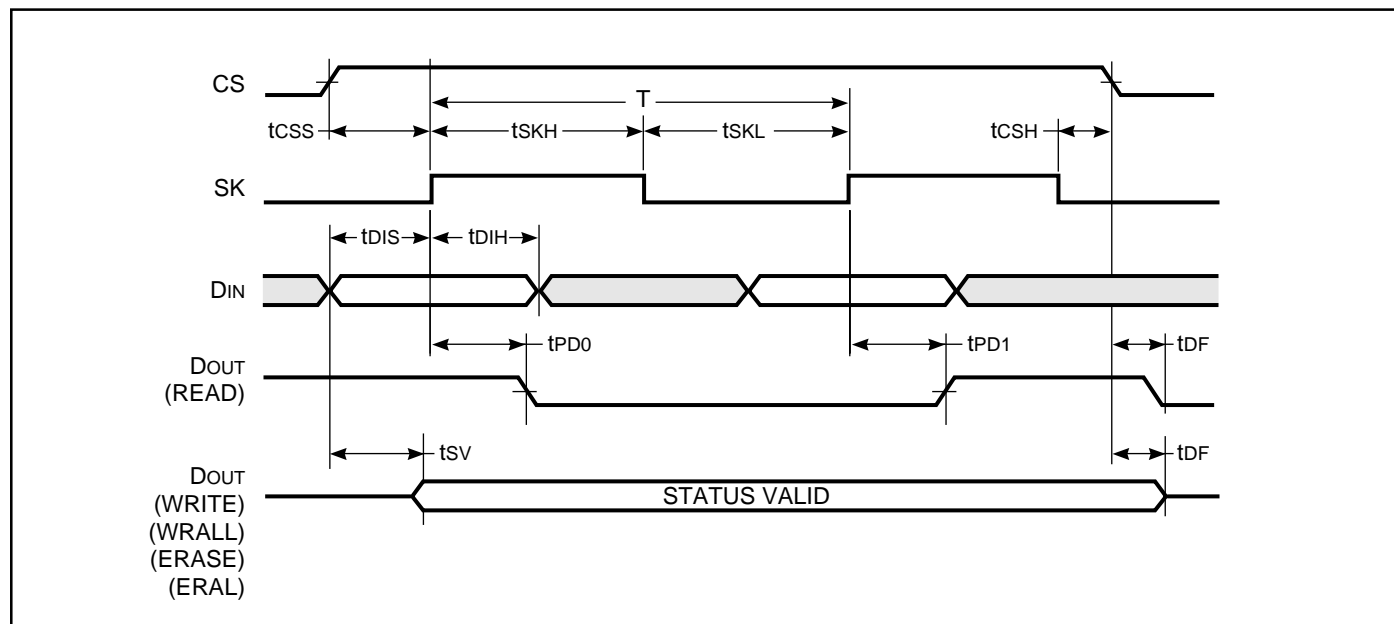
FIGURE 3. READ CYCLE TIMING

*Address Pointer Cycles to the Next Register
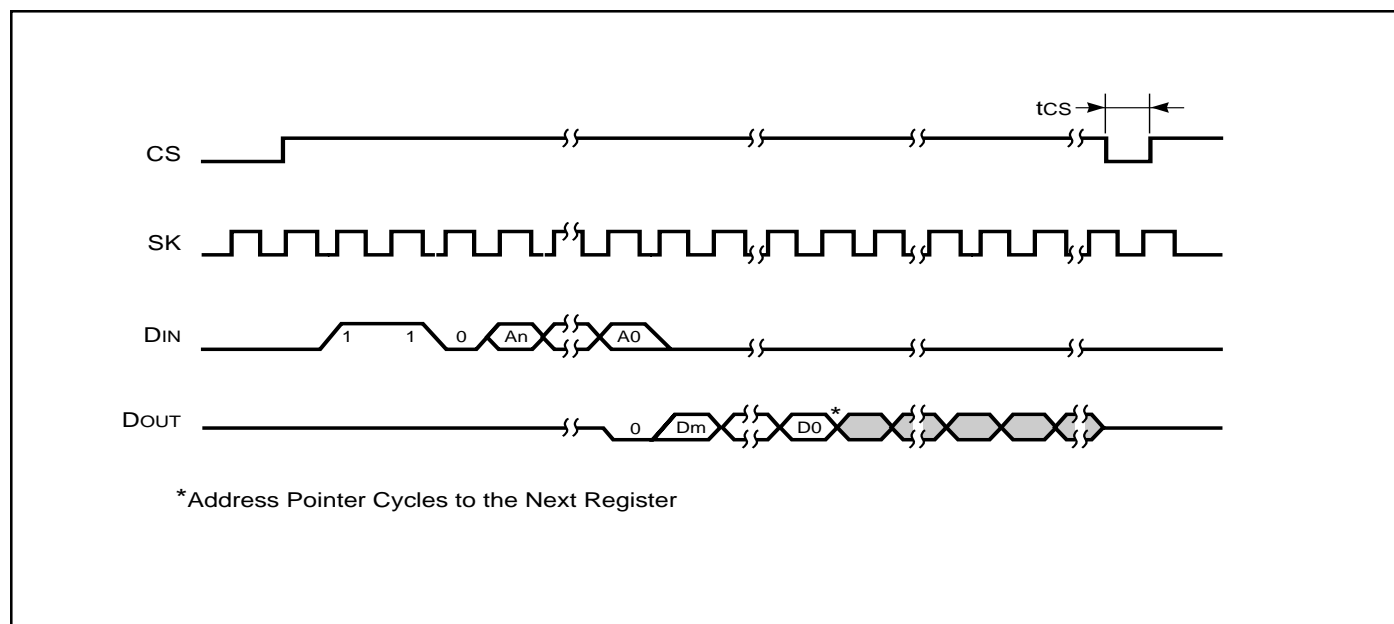
Notes:
To determine address bits An-A0 and data bits Dm-Do, see Instruction Set for the specific device.

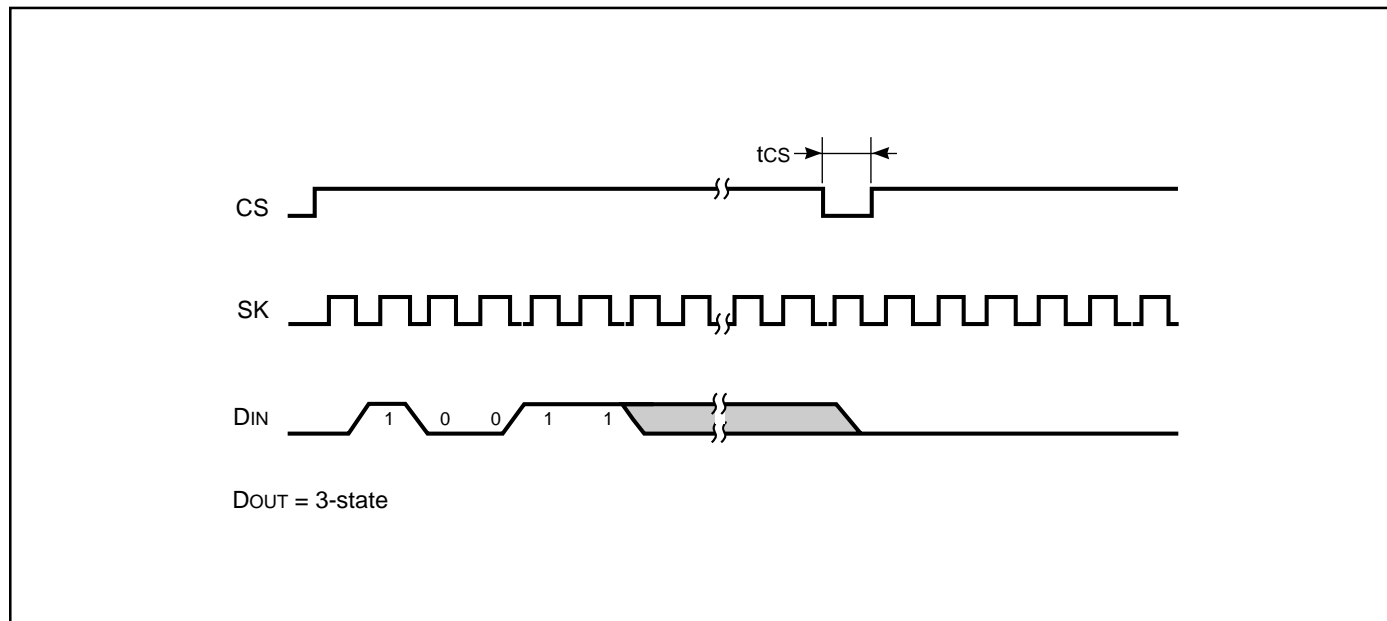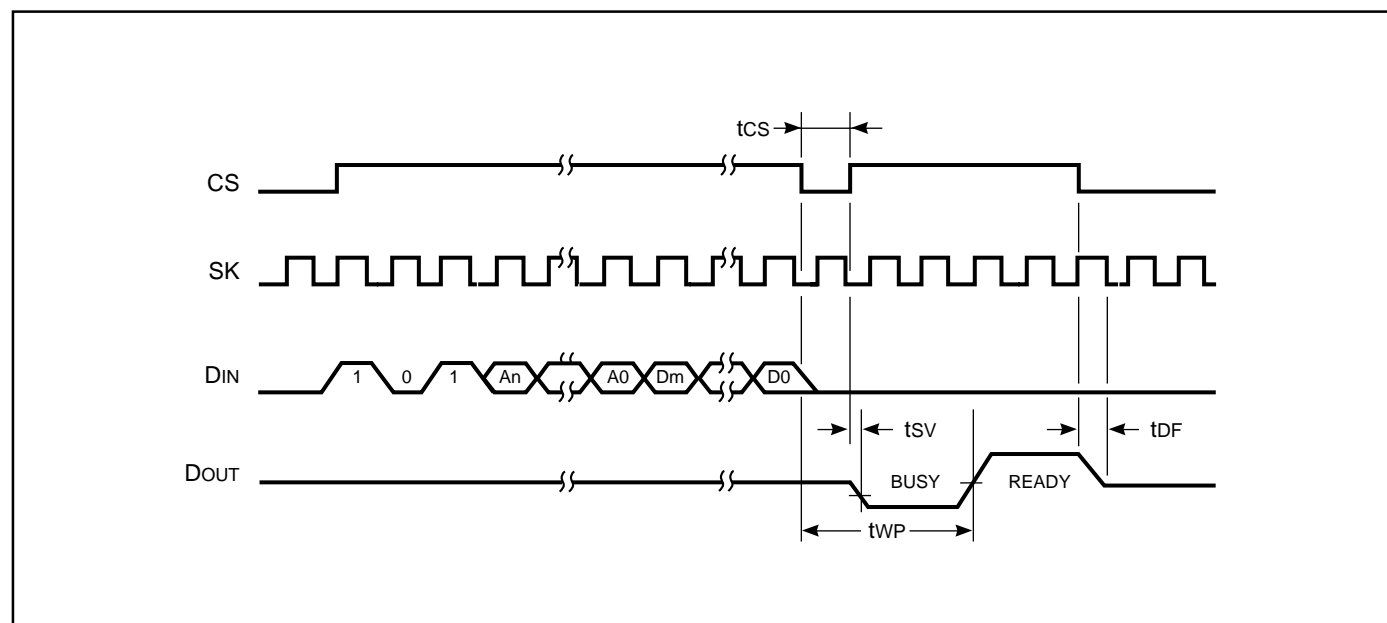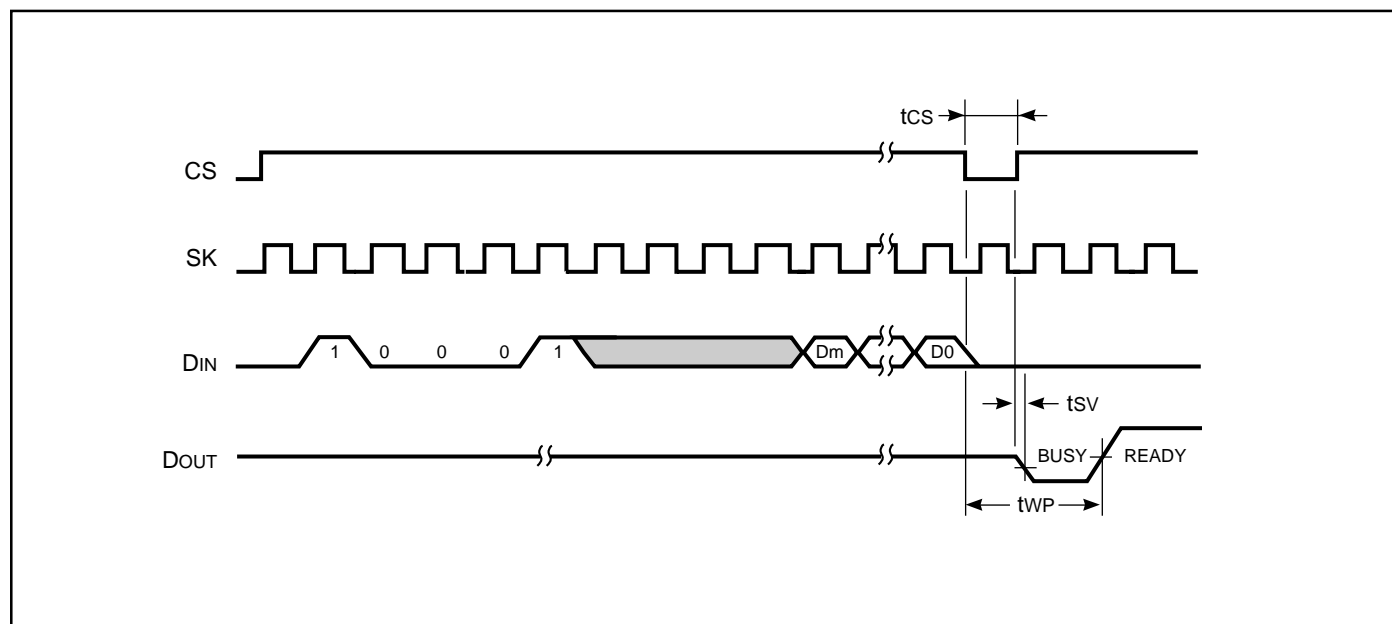## AC WAVEFORMS

FIGURE 4.   WRITE ENABLE (WEN) CYCLE TIMING

FIGURE 5.   WRITE (WRITE) CYCLE TIMING

Notes:

1. After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in $\overline{BUSY}$ status (D_{OUT} indicates $\overline{BUSY}$ status) then attempting to perform another instruction could cause device malfunction.

2. To determine address bits A_n-A_0 and data bits D_m-D_0, see Instruction Set for the specific device.

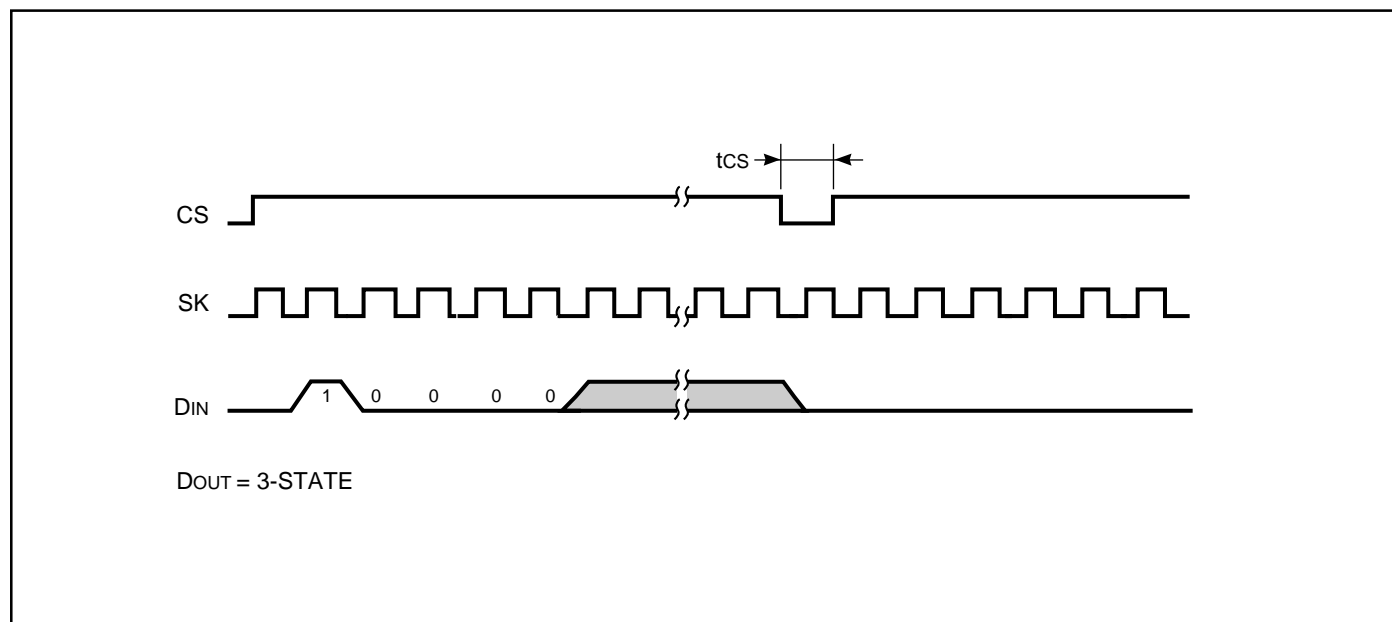## AC WAVEFORMS

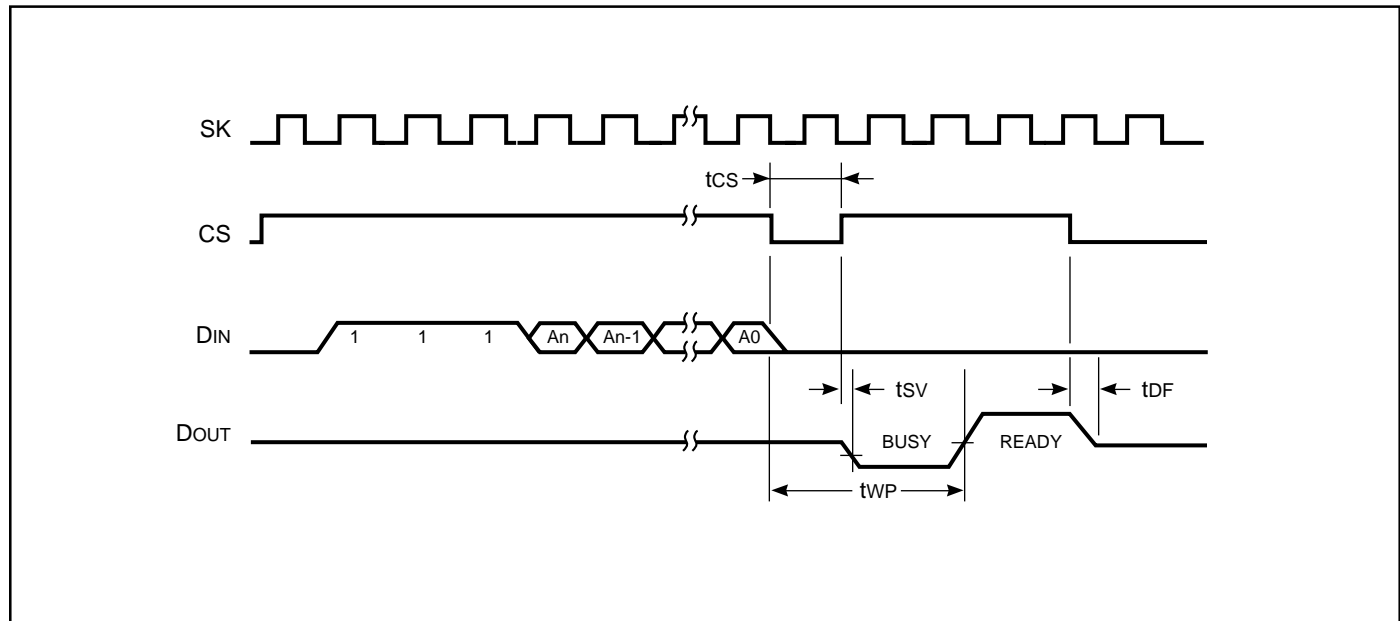## FIGURE 6.   WRITE ALL (WRALL) CYCLE TIMING

Notes:
1. After the completion of the instruction (D_{OUT} is in READY status) then it may perform another instruction. If device is in $\overline{BUSY}$ status (D_{OUT} indicates $\overline{BUSY}$ status) then attempting to perform another instruction could cause device malfunction.
2. To determine data bits D_m-D₀, see Instruction Set for the appropriate device.
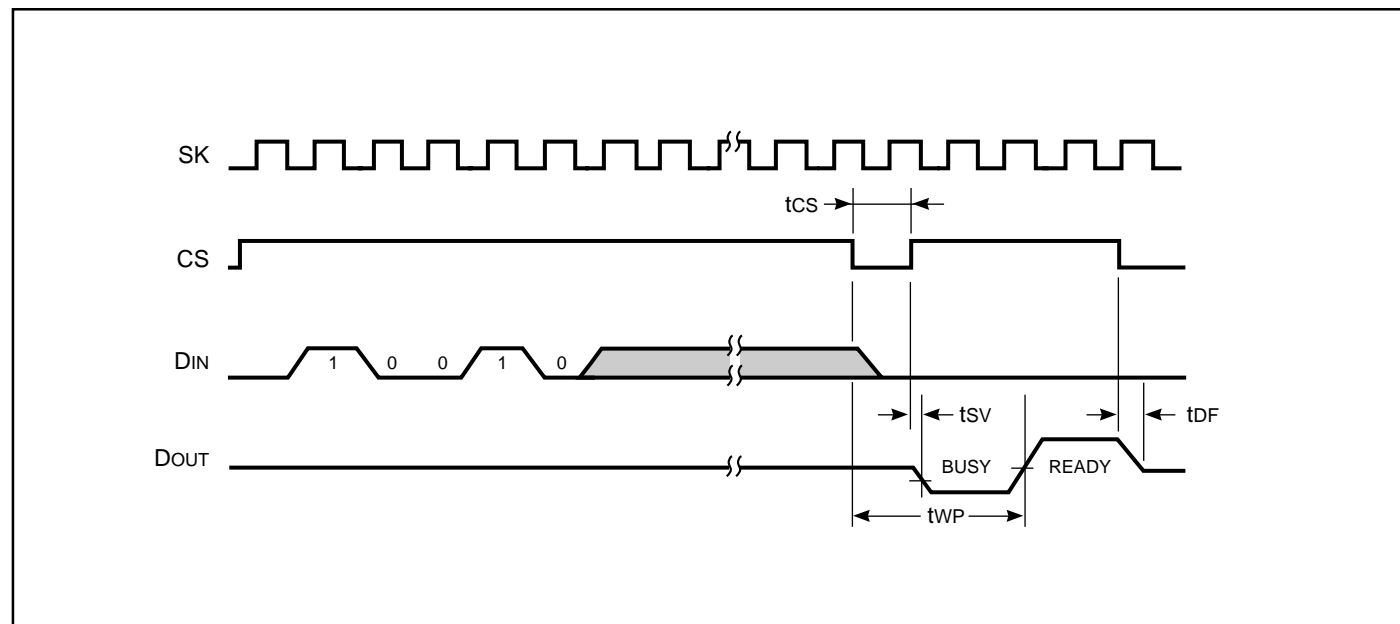
FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

AC WAVEFORMS

FIGURE 8. ERASE (REGISTER ERASE) CYCLE TIMING

Notes:

To determine data bits An - A0, see Instruction Set for the appropriate device.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

Note for Figures 8 and 9:

After the completion of the instruction (D$_{OUT}$ is in READY status) then it may perform another instruction. If device is in $\overline{\text{BUSY}}$ status (D$_{OUT}$ indicates $\overline{\text{BUSY}}$ status) then attempting to perform another instruction could cause device malfunction.

ORDERING INFORMATION

Industrial Range: -40ºC to +85ºC

Speed	Voltage Range	Order Part No.	Package
2Mhz *	2.5V to 5.5V	IS93C76A-3PI	300-mil Plastic DIP
		IS93C76A-3GRI	SOIC JEDEC
		IS93C76A-3ZI	169-mil TSSOP
2Mhz *	2.5V to 5.5V	IS93C86A-3PI	300-mil Plastic DIP
		IS93C86A-3GRI	SOIC JEDEC
		IS93C86A-3ZI	169-mil TSSOP
1Mhz *	1.8V to 5.5V	IS93C76A-2PI	300-mil Plastic DIP
		IS93C76A-2GRI	SOIC JEDEC
		IS93C76A-2ZI	169-mil TSSOP
1Mhz *	1.8V to 5.5V	IS93C86A-2PI	300-mil Plastic DIP
		IS93C86A-2GRI	SOIC JEDEC
		IS93C86A-2ZI	169-mil TSSOP

* The specification allows higher speed. Please see AC Characteristics for more information.

ORDERING INFORMATION

Automotive Range: -40ºC to +125ºC

Speed	Voltage Range	Order Part No.	Package
2Mhz *	2.5V to 5.5V	IS93C76A-3PA	300-mil Plastic DIP
		IS93C76A-3GRA	SOIC JEDEC
2 Mhz *	2.5V to 5.5V	IS93C86A-3PA	300-mil Plastic DIP
		IS93C86A-3GRA	SOIC JEDEC
3Mhz	4.5V to 5.5V	IS93C76A-PA	300-mil Plastic DIP
		IS93C76A-GRA	SOIC JEDEC
3Mhz	4.5V to 5.5V	IS93C86A-PA	300-mil Plastic DIP
		IS93C86A-GRA	SOIC JEDEC

* The specification allows higher speed. Please see AC Characteristics for more information.