

3.0 Volt-Only Flash & SRAM COMBO with Stacked Multi-Chip Package (MCP) — 64 Mbit Simultaneous Operation Flash Memory and 8 Mbit Static RAM

PRELIMINARY INFORMATION
AUGUST 2002

MCP FEATURES

- Power supply voltage 2.7V to 3.1V
- High performance:
 - Flash: 70 ns maximum access time
 - SRAM: 70 ns maximum access time
- Package: 65-ball BGA
- Industrial Temperature: -40C to +85C

FLASH FEATURES

- Power Dissipation:
 - Read Current at 1 Mhz: 7 mA maximum
 - Read Current at 5 Mhz: 18 mA maximum
 - Sleep Mode: 5 μ A maximum
- Simultaneous R/W Operations (dual virtual bank):
 - Zero latency between read and write operations; Data can be programmed or erased in one bank while data is simultaneously being read from the other bank
- Low-Power Mode:
 - A period of no activity causes flash to enter a low-power state
- Erase Suspend/Resume:
 - Suspends of erase activity to allow a read in the same bank
- Sector Erase Architecture:
 - 16 words of 4k size and 126 words of 32K size (32 Mbit)
 - Any combination of sectors, or the entire flash can be simultaneously erased
- Erase Algorithms:
 - Automatically preprograms/erases the flash memory entirely, or by sector
- Program Algorithms:
 - Automatically writes and verifies data at specified address
- Hidden ROM Region:
 - 256 byte with a Factory-serialized secure electronic serial number (ESN), which is accessible through a command sequence
- Data Polling and Toggle Bit:
 - Allow for detection of program or erase cycle completion
- Ready-Busy output (RY/ $\overline{\text{BY}}$)
 - Detection of program or erase cycle completion

- Over 100,000 write/erase cycles
- Low supply voltage ($V_{\text{ccf}} \leq 2.5\text{V}$) inhibits writes
- $\overline{\text{WP}}/\text{ACC}$ input pin:
 - If V_{IL} , allows partial protection of boot sectors
 - If V_{IH} , allows removal of boot sector protection
 - If V_{acc} , program time is improved

SRAM FEATURES (8 Mb density)

- Power Dissipation:
 - Operating: 50 mA maximum
 - Standby: 15 μ A maximum
- Chip Selects: $\overline{\text{CE}}1\text{s}$, $\text{CE}2\text{s}$
- Power down feature using $\overline{\text{CE}}1\text{s}$, or $\text{CE}2\text{s}$
- Data retention supply voltage: 1.0 to 3.1 volt
- Byte data control: $\overline{\text{LB}}\text{s}$ (DQ0–DQ7), $\overline{\text{UB}}\text{s}$ (DQ8–DQ15) — on x16 mode

GENERAL DESCRIPTION

The flash and SRAM MCP is available in 64 Mbit Flash/8 Mbit SRAM, with a data bus of either x8 or x16. The 64 Mbit flash is composed of 4,194,304 words of 16 bits or 8,388,608 bytes of 8 bits. The 8Mbit SRAM has 524,288 words of 16 bits or 1,048,576 bytes of 8 bits. Data lines DQ0-DQ7 handle the x8 mode, while lines DQ0-DQ15 handle the x16 mode.

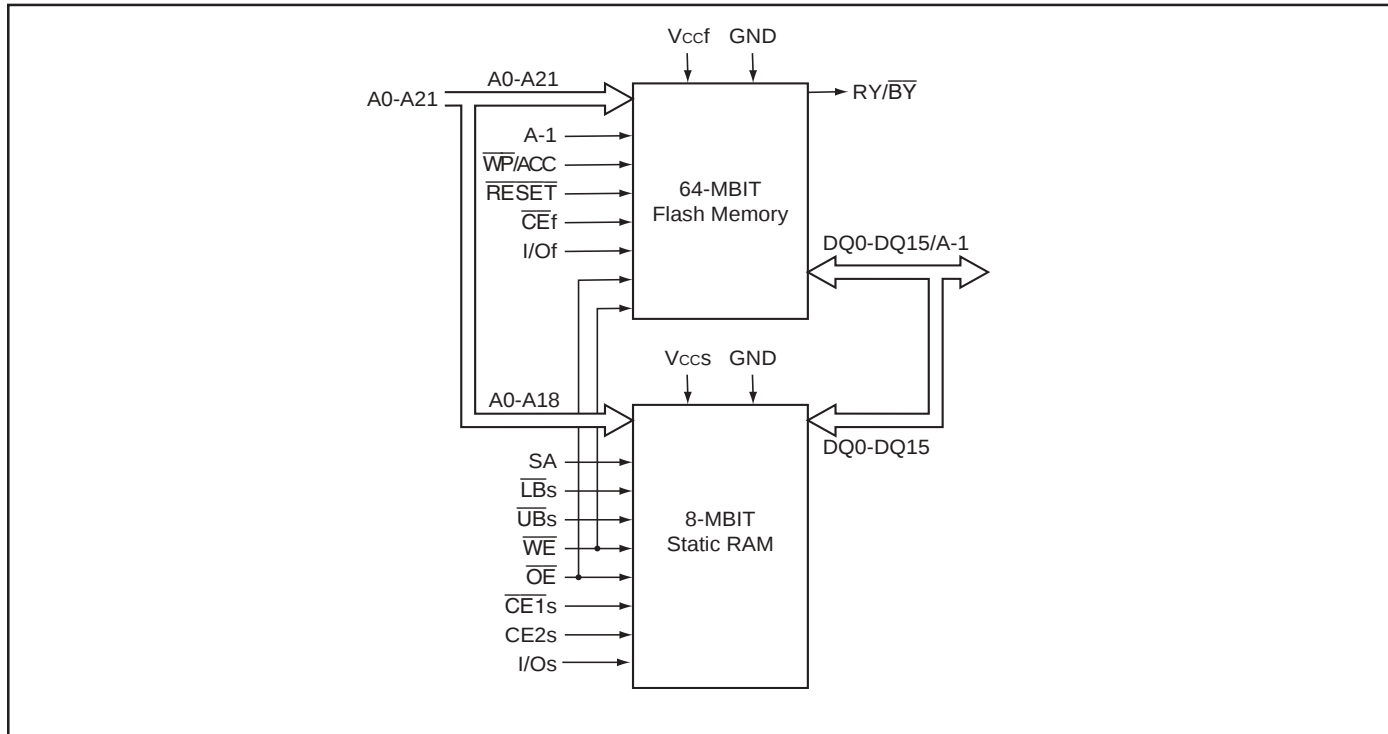
The package uses a 3.0V power supply for all operations. No other source is required for program and erase operations. The flash can be programmed in system using this 3.0V supply, or can be programmed in a standard EPROM programmer.

The 64 Mbit flash/8 Mbit SRAM is offered in a 65-ball BGA or 101-ball BGA package. The flash is compatible with the JEDEC Flash command set standard. The flash access time is 70ns and the SRAM access time is 70 ns.

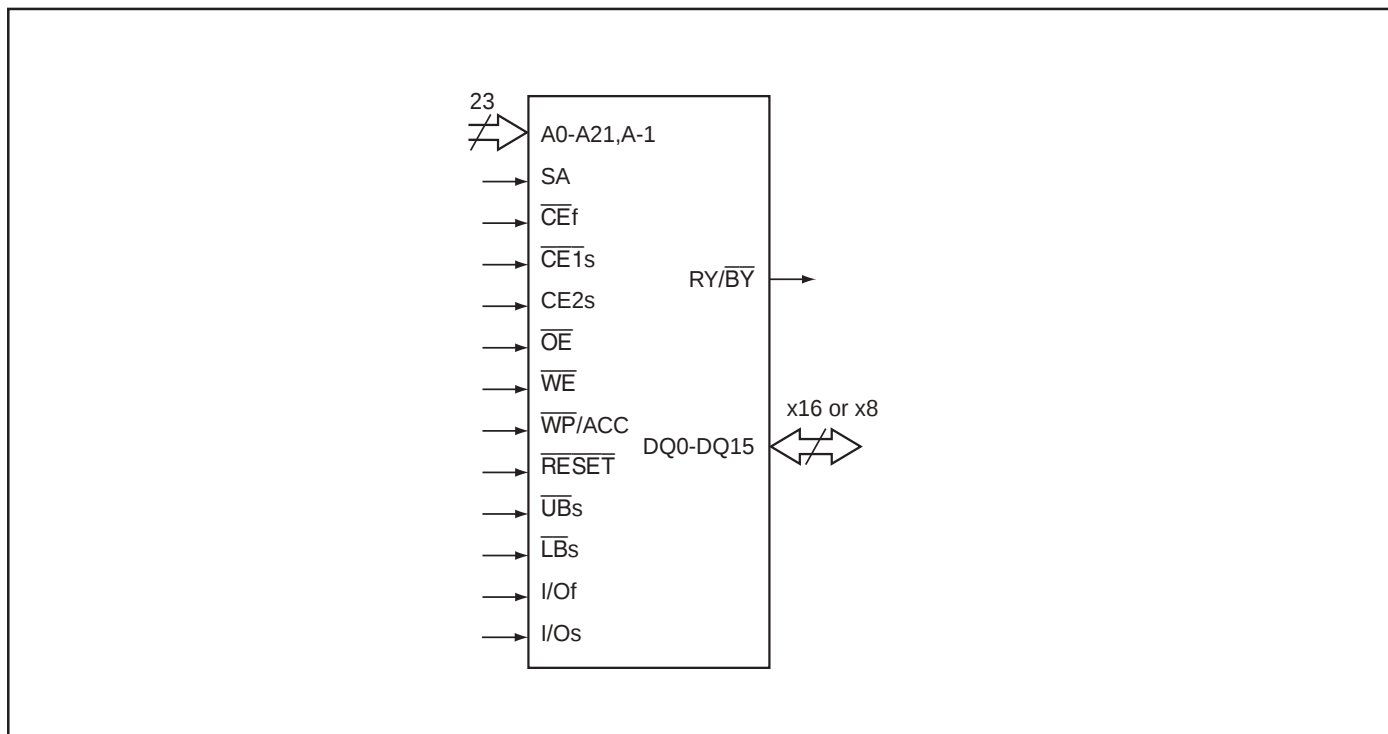
The Flash architecture is composed of two virtual banks made of a combination of four physical banks, which allows simultaneous operation on each. Optimized performance can be achieved by first initializing a program or erase function in one bank, then immediately starting a read from the other bank. Both operations would then be operating simultaneously, with zero latency.

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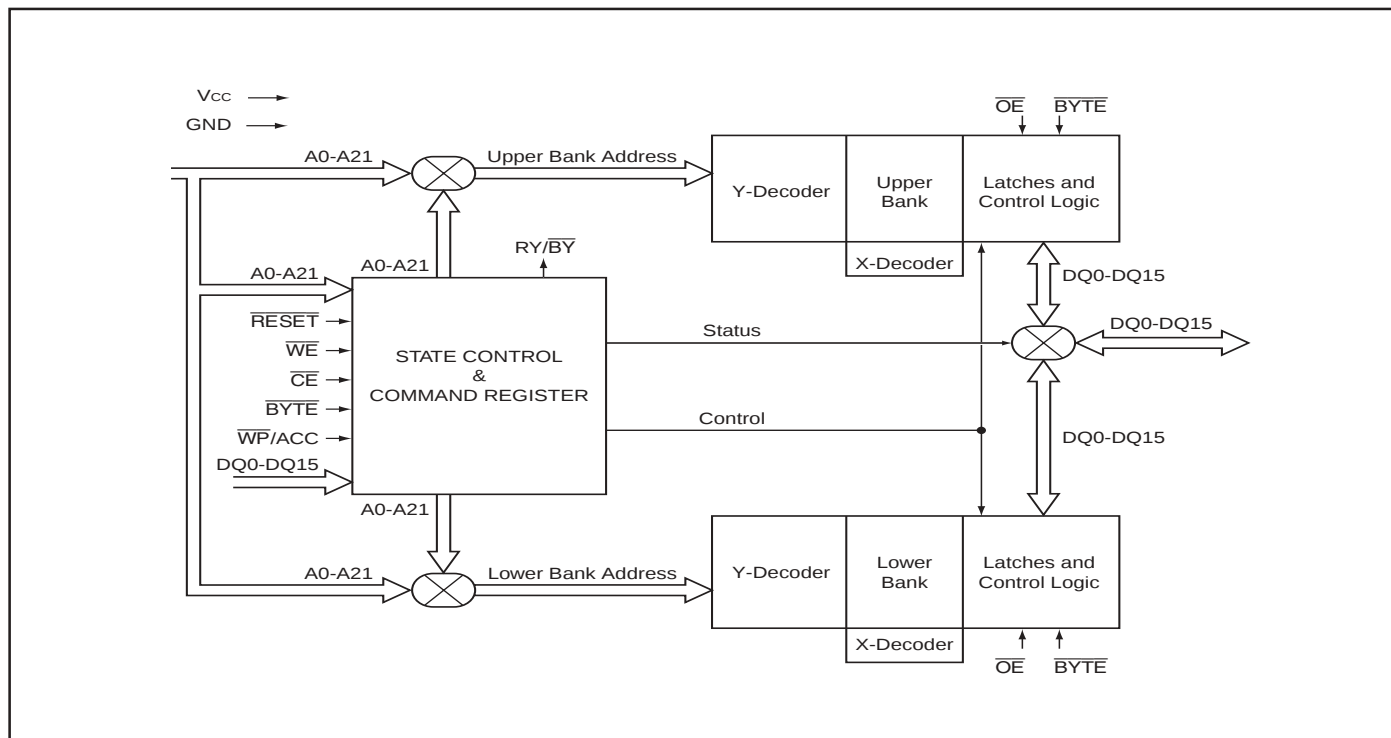
MCP BLOCK DIAGRAM



LOGIC SYMBOL



FLASH MEMORY BLOCK DIAGRAM



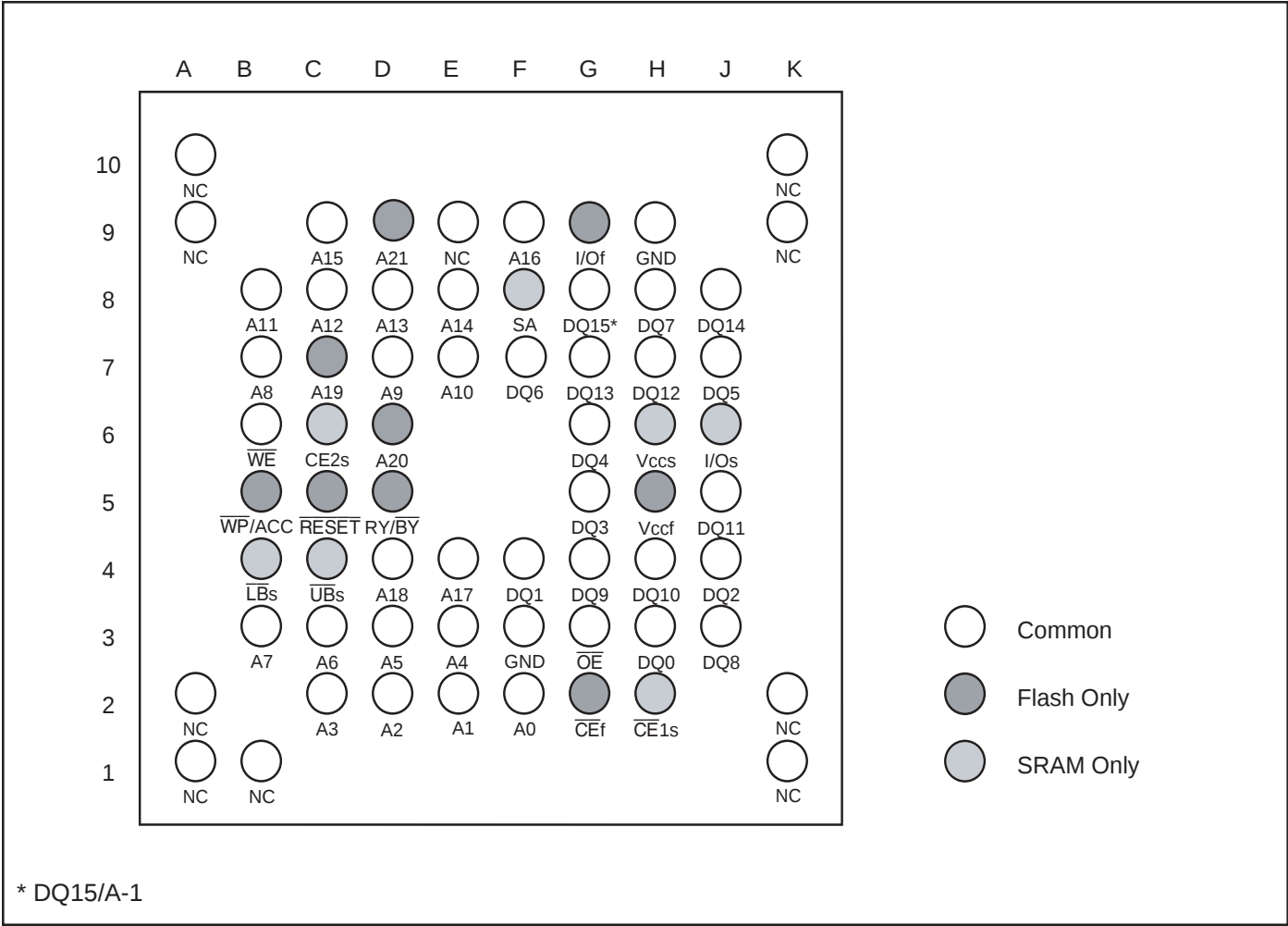
FLASH BANK ORGANIZATION

Physical Bank	Bank Size	Number of Sectors	Sector Size
1	8Mb	8	8KB / 4KW
		15	64KB / 32KW
2	24Mb	48	64KB / 32KW
3	24Mb	48	64KB / 32KW
4	8Mb	15	64KB / 32KW
		8	8KB / 4KW

Note:

Groups of banks can be configured into two virtual banks.

PIN CONFIGURATION (64Mb Flash and 8 Mb SRAM)
65 BALL FBGA (Top View) (9.00mm x 9.00mm Body, 0.8 mm Ball Pitch)



PIN DESCRIPTIONS

A0-A18	Address Inputs, Common
A19-A21, A-1	Address Inputs, Flash
DQ0-DQ15/A-1	Data Inputs/Outputs
RESET	Reset
CE1s, CE2s	Chip Selects, SRAM
I/Os	I/O Configuration, SRAM
I/Of	I/O Configuration, Flash
CEf	Chip Enable Input, Flash
OE	Output Enable Input
WE	Write Enable Input

LBs	Lower-byte Control (DQ0-DQ7), SRAM
UBs	Upper-byte Control (DQ8-DQ15), SRAM
WP/ACC	Write Protect/Acceleration Pin, Flash
RY/BY	Ready/Busy Output
SA	High Order Address Pin, SRAM (x8)
NC	No Connection
Vccf	Power, Flash
Vccs	Power, SRAM
GND	Ground

DEVICE BUS OPERATIONS

User Bus Operations (Flash = WORD mode: I/Of = Vccf, SRAM = WORD mode)

OPERATION ^(1,3)	$\overline{CE}f$	$\overline{CE}1s$	CE2s	$\overline{OE}$	$\overline{WE}$	SA ⁽⁶⁾	$\overline{LB}s$	$\overline{UB}s$	DQ ₀ -DQ ₇	DQ ₈ -DQ ₁₅	$\overline{RESET}$	$\overline{WP}/ACC^{(5)}$
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash ⁽²⁾	L	H	X	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	L	H	X	L	L	DOUT	DOUT	H	X
	H	L	H	L	H	X	H	L	High-Z	DOUT	H	X
	H	L	H	L	H	X	L	H	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	L	X	L	L	DIN	DIN	H	X
	H	L	H	X	L	X	H	L	High-Z	DIN	H	X
	H	L	H	X	L	X	L	H	DIN	High-Z	H	X
Temporary Sector Group Unprotection ⁽⁴⁾	X	X	X	X	X	X	X	X	X	X	V _{ID(8)}	X
Flash Hardware	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
Reset	X	X	L	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector	X	X	X	X	X	X	X	X	X	X	X	L
Write Protection												

Notes:

- Any operations not indicated this column are inhibited.
- $\overline{WE}$ can be VIL if $\overline{OE}$ is VIL, $\overline{OE}$ at VIH initiates the write operations.
- Do not apply $\overline{CE}f = VIL$, $\overline{CE}1s = VIL$ and CE2s = VIH all at once.
- It is also used for the extended sector group protections.
- $\overline{WP}/ACC = VIL$: protection of boot sectors.
 $\overline{WP}/ACC = VIH$: removal of boot sectors protection.
 $\overline{WP}/ACC = VACC$ (9V): Program time will reduce by 40%.
- SA: Don't care or open.
- L = VIL, H = VIH, X = VIL or VIH.
- See DC CHARACTERISTICS.

DEVICE BUS OPERATIONS

User Bus Operations (Flash = BYTE mode: I/Of = GND, SRAM = WORD mode)

OPERATION ^(1,3)	$\overline{CE}_f$	$\overline{CE}_{1s}$	CE2s	DQ ₁₅ /A-1	$\overline{OE}$	$\overline{WE}$	SA ⁽⁶⁾	$\overline{LB}_s$	$\overline{UB}_s$	DQ ₀ -DQ ₇	DQ ₈ -DQ ₁₅	$\overline{RESET}$	WPI/ACC ⁽⁵⁾
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	A-1	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	A-1	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash ⁽²⁾	L	H	X	A-1	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	A-1	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	A-1	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	A-1	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	X	L	H	X	L	L	DOUT	DOUT	H	X
	H	L	H	X	L	H	X	H	L	High-Z	DOUT	H	X
	H	L	H	X	L	H	X	L	H	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	X	L	L	DIN	DIN	H	X
	H	L	H	X	X	L	X	H	L	High-Z	DIN	H	X
	H	L	H	X	X	L	X	L	H	DIN	High-Z	H	X
Temporary Sector Group Unprotection ⁽⁴⁾	X	X	X	X	X	X	X	X	X	X	X	V _{ID(8)}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
	X	X	L	X	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Notes:

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 $\overline{WP}/ACC$ = VACC (9V): Program time will reduce by 40%.
- SA: Don't care or open.
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DEVICE BUS OPERATIONS

User Bus Operations (Flash = WORD mode: I/Of = Vccf, SRAM = BYTE mode)

OPERATION ^(1,3)	$\overline{CE}f$	$\overline{CE}1s$	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}s^{(6)}$	$\overline{UB}s^{(6)}$	DQ ₀ -DQ ₇	DQ ₈ -DQ ₁₅	$\overline{RESET}$	$\overline{WP}/ACC^{(5)}$
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash ⁽²⁾	L	H	X	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	L	H	SA	X	X	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	DIN	High-Z	H	X
Temporary Sector Group Unprotection ⁽⁴⁾	X	X	X	X	X	X	X	X	X	X	V _{ID(8)}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
	X	X	L	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

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User Bus Operations (Flash = BYTE mode: I/Of = GND, SRAM = BYTE mode)

OPERATION ^(1,3)	$\overline{CE}_f$	$\overline{CE}_{1s}$	CE2s	DQ ₁₅ /A-1	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}_s^{(6)}$	$\overline{UB}_s^{(6)}$	DQ ₀ -DQ ₇	DQ ₈ -DQ ₁₅	$\overline{RESET}$	WP/ACC ⁽⁵⁾
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	A-1	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	A-1	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash ⁽²⁾	L	H	X	A-1	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	A-1	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	A-1	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	A-1	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	X	L	H	SA	X	X	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	SA	X	X	DIN	High-Z	H	X
Temporary Sector Group Unprotection ⁽⁴⁾	X	X	X	X	X	X	X	X	X	X	X	V _{ID(8)}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	L	X	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector	X	X	X	X	X	X	X	X	X	X	X	X	L

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- See DC CHARACTERISTICS.

FLASH - SECTOR ADDRESS

Bank	Sector	Sector Address A21-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank 1	SA0	0000000000	8/4	000000h–001FFFh	000000h–000FFFh
Bank 1	SA1	0000000001	8/4	002000h–003FFFh	001000h–001FFFh
Bank 1	SA2	0000000010	8/4	004000h–005FFFh	002000h–002FFFh
Bank 1	SA3	0000000011	8/4	006000h–007FFFh	003000h–003FFFh
Bank 1	SA4	0000000100	8/4	008000h–009FFFh	004000h–004FFFh
Bank 1	SA5	0000000101	8/4	00A000h–00BFFFh	005000h–005FFFh
Bank 1	SA6	0000000110	8/4	00C000h–00DFFFh	006000h–006FFFh
Bank 1	SA7	0000000111	8/4	00E000h–00FFFFFFh	007000h–007FFFh
Bank 1	SA8	0000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh
Bank 1	SA9	0000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh
Bank 1	SA10	0000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
Bank 1	SA11	0000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
Bank 1	SA12	0000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
Bank 1	SA13	0000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
Bank 1	SA14	0000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
Bank 1	SA15	0001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
Bank 1	SA16	0001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
Bank 1	SA17	0001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
Bank 1	SA18	0001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
Bank 1	SA19	0001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
Bank 1	SA20	0001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
Bank 1	SA21	0001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
Bank 1	SA22	0001111xxx	64/32	0F0000h–0FFFFFFh	078000h–07FFFFh
Bank 2	SA23	0010000xxx	64/32	100000h–00FFFFh	080000h–087FFFh
Bank 2	SA24	0010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
Bank 2	SA25	0010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
Bank 2	SA26	0010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
Bank 2	SA27	0010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
Bank 2	SA28	0010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
Bank 2	SA29	0010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh
Bank 2	SA30	0010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
Bank 2	SA31	0011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
Bank 2	SA32	0011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
Bank 2	SA33	0011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
Bank 2	SA34	0011011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh
Bank 2	SA35	0011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh

FLASH - SECTOR ADDRESS Continued:

Bank	Sector	Sector Address A21-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank 2	SA36	0011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
Bank 2	SA37	0011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh
Bank 2	SA38	0011111xxx	64/32	1F0000h–1FFFFFFh	0F8000h–0FFFFFFh
Bank 2	SA39	0100000xxx	64/32	200000h–20FFFFh	0F9000h–107FFFh
Bank 2	SA40	0100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
Bank 2	SA41	0100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
Bank 2	SA42	0100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
Bank 2	SA43	0100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
Bank 2	SA44	0100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
Bank 2	SA45	0100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
Bank 2	SA46	0100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
Bank 2	SA47	0101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
Bank 2	SA48	0101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
Bank 2	SA49	0101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
Bank 2	SA50	0101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
Bank 2	SA51	0101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
Bank 2	SA52	0101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
Bank 2	SA53	0101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
Bank 2	SA54	0101111xxx	64/32	2F0000h–2FFFFFFh	178000h–17FFFFh
Bank 2	SA55	0110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
Bank 2	SA56	0110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
Bank 2	SA57	0110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
Bank 2	SA58	0110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
Bank 2	SA59	0110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
Bank 2	SA60	0110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
Bank 2	SA61	0110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
Bank 2	SA62	0110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
Bank 2	SA63	0111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
Bank 2	SA64	0111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
Bank 2	SA65	0111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
Bank 2	SA66	0111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
Bank 2	SA67	0111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
Bank 2	SA68	0111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
Bank 2	SA69	0111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
Bank 2	SA70	0111111xxx	64/32	3F0000h–3FFFFFFh	1F8000h–1FFFFFFh

FLASH - SECTOR ADDRESS Continued:

Bank	Sector	Sector Address A21-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank 3	SA71	1000000xxx	64/32	400000h–40FFFFh	200000h–207FFFh
Bank 3	SA72	1000001xxx	64/32	410000h–41FFFFh	208000h–20FFFFh
Bank 3	SA73	1000010xxx	64/32	420000h–42FFFFh	210000h–217FFFh
Bank 3	SA74	1000011xxx	64/32	430000h–43FFFFh	218000h–21FFFFh
Bank 3	SA75	1000100xxx	64/32	440000h–44FFFFh	220000h–227FFFh
Bank 3	SA76	1000101xxx	64/32	450000h–45FFFFh	228000h–22FFFFh
Bank 3	SA77	1000110xxx	64/32	460000h–46FFFFh	230000h–237FFFh
Bank 3	SA78	1000111xxx	64/32	470000h–47FFFFh	238000h–23FFFFh
Bank 3	SA79	1001000xxx	64/32	480000h–48FFFFh	240000h–247FFFh
Bank 3	SA80	1001001xxx	64/32	490000h–49FFFFh	248000h–24FFFFh
Bank 3	SA81	1001010xxx	64/32	4A0000h–4AFFFFh	250000h–257FFFh
Bank 3	SA82	1001011xxx	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
Bank 3	SA83	1001100xxx	64/32	4C0000h–4CFFFFh	260000h–267FFFh
Bank 3	SA84	1001101xxx	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
Bank 3	SA85	1001110xxx	64/32	4E0000h–4EFFFFh	270000h–277FFFh
Bank 3	SA86	1001111xxx	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
Bank 3	SA87	1010000xxx	64/32	500000h–50FFFFh	280000h–28FFFFh
Bank 3	SA88	1010001xxx	64/32	510000h–51FFFFh	288000h–28FFFFh
Bank 3	SA89	1010010xxx	64/32	520000h–52FFFFh	290000h–297FFFh
Bank 3	SA90	1010011xxx	64/32	530000h–53FFFFh	298000h–29FFFFh
Bank 3	SA91	1010100xxx	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
Bank 3	SA92	1010101xxx	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
Bank 3	SA93	1010110xxx	64/32	560000h–56FFFFh	2B0000h–2B7FFFh
Bank 3	SA94	1010111xxx	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
Bank 3	SA95	1011000xxx	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
Bank 3	SA96	1011001xxx	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
Bank 3	SA97	1011010xxx	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
Bank 3	SA98	1011011xxx	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
Bank 3	SA99	1011100xxx	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
Bank 3	SA100	1011101xxx	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
Bank 3	SA101	1011110xxx	64/32	5E0000h–5EFFFFh	2F0000h–2FFFFFh
Bank 3	SA102	1011111xxx	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
Bank 3	SA103	1100000xxx	64/32	600000h–60FFFFh	300000h–307FFFh
Bank 3	SA104	1100001xxx	64/32	610000h–61FFFFh	308000h–30FFFFh
Bank 3	SA105	1100010xxx	64/32	620000h–62FFFFh	310000h–317FFFh

FLASH - SECTOR ADDRESS Continued:

Bank	Sector	Sector Address A21-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank 3	SA106	1100011xxx	64/32	630000h–63FFFFh	318000h–31FFFFh
Bank 3	SA107	1100100xxx	64/32	640000h–64FFFFh	320000h–327FFFh
Bank 3	SA108	1100101xxx	64/32	650000h–65FFFFh	328000h–32FFFFh
Bank 3	SA109	1100110xxx	64/32	660000h–66FFFFh	330000h–337FFFh
Bank 3	SA110	1100111xxx	64/32	670000h–67FFFFh	338000h–33FFFFh
Bank 3	SA111	1101000xxx	64/32	680000h–68FFFFh	340000h–347FFFh
Bank 3	SA112	1101001xxx	64/32	690000h–69FFFFh	348000h–34FFFFh
Bank 3	SA113	1101010xxx	64/32	6A0000h–6AFFFFh	350000h–357FFFh
Bank 3	SA114	1101011xxx	64/32	6B0000h–6BFFFFh	358000h–35FFFFh
Bank 3	SA115	1101100xxx	64/32	6C0000h–6CFFFFh	360000h–367FFFh
Bank 3	SA116	1101101xxx	64/32	6D0000h–6DFFFFh	368000h–36FFFFh
Bank 3	SA117	1101110xxx	64/32	6E0000h–6EFFFFh	370000h–377FFFh
Bank 3	SA118	1101111xxx	64/32	6F0000h–6FFFFFh	378000h–37FFFFh
Bank 4	SA119	1110000xxx	64/32	700000h–70FFFFh	380000h–387FFFh
Bank 4	SA120	1110001xxx	64/32	710000h–71FFFFh	388000h–38FFFFh
Bank 4	SA121	1110010xxx	64/32	720000h–72FFFFh	390000h–397FFFh
Bank 4	SA122	1110011xxx	64/32	730000h–73FFFFh	398000h–39FFFFh
Bank 4	SA123	1110100xxx	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
Bank 4	SA124	1110101xxx	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
Bank 4	SA125	1110110xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
Bank 4	SA126	1110111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
Bank 4	SA127	1111000xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
Bank 4	SA128	1111001xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
Bank 4	SA129	1111010xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
Bank 4	SA130	1111011xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
Bank 4	SA131	1111100xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
Bank 4	SA132	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
Bank 4	SA133	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
Bank 4	SA134	1111111000	8/4	7F0000h–7F1FFFh	3F8000h–3F8FFFh
Bank 4	SA135	1111111001	8/4	7F2000h–7F3FFFh	3F9000h–3F9FFFh
Bank 4	SA136	1111111010	8/4	7F4000h–7F5FFFh	3FA000h–3FAFFFh
Bank 4	SA137	1111111011	8/4	7F6000h–7F7FFFh	3FB000h–3FBFFFh
Bank 4	SA138	1111111100	8/4	7F8000h–7F9FFFh	3FC000h–3FCFFFh
Bank 4	SA139	1111111101	8/4	7FA000h–7FBFFFh	3FD000h–3FDFFFh
Bank 4	SA140	1111111110	8/4	7FC000h–7FDFFFh	3FE000h–3FEFFFh
Bank 4	SA141	1111111111	8/4	7FE000h–7FFFFFFh	3FF000h–3FFFFFFh

Note: The address range is A21:A-1 in byte mode (I/Of=VIL) or A21:A0 in word mode (I/Of=VIH). The bank address bits are A21 - A19.

FLASH - SECURITY SECTOR ADDRESSES

(Hidden-ROM)

Sector Address A21-A12	Size Byte / Word	(x8) Address Range	(x16) Address Range
0000000xxx	256/128	00000h-0000FFh	00000h-0007Fh

SECTOR GROUP ADDRESS

Sector Group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0 1 1	1 0 1	X	X	X	SA8 to SA10
SGA9	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	1	0	0	0	1	X	X	X	X	X	SA75 to SA78

SECTOR GROUP ADDRESS Continued:

Sector Group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA26	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA33	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	1	1	1	1	1	0	0	X	X	X	SA131 to SA133
						0	1				
						1	0				
SGA40	1	1	1	1	1	1	1	0	0	0	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	SA141

FLASH MEMORY AUTOSELECT CODES

Type		A ₂₁ to A ₁₂	A ₆	A ₃	A ₂	A ₁	A ₀	A ₋₁ ⁽¹⁾	Code (HEX)
Manufacturer's Code		BA	VIL	VIL	VIL	VIL	VIL	VIL	04h
Device Code	Byte	BA	VIL	VIL	VIL	VIL	VIH	VIL	7Eh
	Word	BA	VIL	VIL	VIL	VIL	VIH	X	227Eh
Extended Device Code ⁽³⁾	Byte	BA	VIL	VIH	VIH	VIH	VIL	VIL	02h
	Word	BA	VIL	VIH	VIH	VIH	VIL	X	2202h
Extended Device Code ⁽³⁾	Byte	BA	VIL	VIH	VIH	VIH	VIH	VIL	01h
	Word	BA	VIL	VIH	VIH	VIH	VIH	X	2201h
Sector Group Protection	Sector Group Addresses		VIL	VIL	VIL	VIH	VIL	VIL	01h ⁽²⁾

Note:

1. A₋₁ is used for Byte mode.
2. Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.
3. At WORD mode, a read cycle at address (BA) 01h (at BYTE mode, (BA) 02h) outputs device code. When 227Eh (at BYTE mode, 7Eh) was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh (at BYTE mode, (BA) 1Ch) , as well as at (BA) 0Fh (at BYTE mode, (BA) 1Eh) .

FLASH MEMORY COMMAND DEFINITIONS

Command Sequence Bus		Bus Write Cycle Req'd	First Bus Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write		Fifth Bus Cycle		Sixth Bus Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read / Reset		1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read / Reset * 1	Word Byte	3	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	F0H	RA	RD	—	—	—	—
Autoselect	Word Byte	3	555H AAAH	AAH	2AAH 555H	55H	(BA) 555H (BA) AAAH	90H	—	—	—	—	—	—
Program	Word Byte	4	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	A0H	PA	PD	—	—	—	—
Chip Erase	Word Byte	6	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	80H	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	10H
Sector Erase	Word Byte	6	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	80H	555H AAAH	AAH	2AAH 555H	55H	SA	30H
Sector Erase Suspend	Word Byte	1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Sector Erase Resume	Word Byte	1	BA	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word Byte	3	555H AAH	AAH	2AAH 555H	55H	555H AAAH	20H	—	—	—	—	—	—
Fast Program * 2	Word Byte	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode * 2	Word Byte	2	BA	90H	XXXH	F0H*6	—	—	—	—	—	—	—	—
Extended Sector Group Protection * 3	Word Byte	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
Query * 4	Word Byte	1	55H AAH	98h	—	—	—	—	—	—	—	—	—	—
Hidden-ROM Entry	Word Byte	3	555H AAAH	AAh	2AAH 555H	55H	555H AAAH	88H	—	—	—	—	—	—
Hidden-ROM Program * 5	Word Byte	4	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	A0H	PA	PD	—	—	—	—
Hidden-ROM Erase * 5	Word Byte	6	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	80H	555H AAAH	AAH	2AAH 555H	55H	HRA	30H
Hidden-Rom Exit * 5	Word Byte	4	555H AAAH	AAH	2AAH 555H	55H	(HRBA) 555H (HRBA) AAAH	90H	XXXH	00H	—	—	—	—

Note:

*1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

*2: This command is valid during Fast Mode.

*3: This command is valid while RESET=VID.

*4: The valid Address is A0 to A6.

*5: This command is valid during Hi-ROM mode.

*6: The data "00h" is also acceptable.

FLASH MEMORY COMMAND DEFINITIONS Continued:

Address bits A21 to A11 = X = "H" or "L" for all address commands except for Program Address (PA), Sector Address (SA), and Bank Address (BA).

Bus operations are defined in "Device Bus Operations".
RA = Address of the memory location to be read
PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased.

The combination of A21, A20, A19, A18, A17, A16, A15, A14, A13, and A12 will uniquely select any sector.
BA = Bank address (A21 to A19)
SPA = Sector group address to be protected.

Set sector group address (SGA) and (A6, A3, A2, A1, A0) = (0, 0, 0, 1, 0) for protect; or SGA and (A6, A3, A2, A1, A0) = (1, 0, 0, 1, 0) for unprotect.

HRA= Address of the Hidden-ROM area
Word mode: 000000h to 00007Fh
Byte mode: 000000h to 0000FFh

HRBA = Bank address of the Hidden-ROM area
A21 = A20 = A19 = 0

RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA.
SD = Sector protection verify data.

Output 01h at protected sector addresses and output 00h at unprotected sector addresses.

The system should generate the following address patterns;
Word mode : 555h or 2AAh to addresses A0 to A10
Byte mode : AAh or 555h to addresses A–1 and A0 to A10

MCP ABSOLUTE MAXIMUM RATINGS^(1,2,3)

Symbol	Parameter	Value	Unit
T _{BIAS}	Temperature Under Bias	–40 to +85	°C
T _{STG}	Storage Temperature	–55 to +125	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for Data, Address and Control Pins	–0.3 to V _{CCF} + 0.3 –0.3 to V _{CCS} + 0.3	V V
V _{IN}	RESET ⁽⁵⁾	–0.5 to +13.0	V
V _{IN}	WP/ACC ⁽⁶⁾	–0.5 to +10.5	V
V _{CCF} /V _{CCS}	Voltage on Vcc Supply Relative to GND ⁽⁴⁾	–0.3 to 3.3	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.
4. Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot VSS to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CCF}+0.3 V or V_{CCS}+0.3 V. During voltage transitions, input or I/O pins may overshoot to V_{CCF}+2.0 V or V_{CCS}+2.0 V for periods of up to 20 ns.
5. Minimum DC input voltage on RESET pin is –0.5 V. During voltage transitions, RESET pin may undershoot VSS to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-V_{CCF} or V_{CCS}) does not exceed 9.0 V. Maximum DC input voltage on RESET pin is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
6. Minimum DC input voltage on WP/ACC pin is –0.5 V. During voltage transitions, WP/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on WP/ACC pin is +10.5 V which may overshoot to +12.0V for periods of up to 20 ns, when V_{CCF} is applied.

MCP OPERATING RANGE

Range	Ambient Temperature	V _{CCF} , V _{CCS}
Industrial	−40°C to +85°C	2.7–3.1V

STANDARD VOLTAGE RANGE V_{CC} = 2.7-3.3 V

	FLASH MEMORY	SRAM	UNITS
Max Access Time	70	70	ns
$\overline{\text{CE}}$ Access	70	70	ns
$\overline{\text{OE}}$ Access	30	35	ns

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	11	14	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	12	16	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0V	14	16	pF
C _{IN3}	$\overline{\text{WP}}$ /ACC Pin Capacitance	V _{IN} = 0V	21.5	26	pF

Notes:

1. Test conditions: T_A = 25°C, f = 1 MHz

MCP DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _{LI}	Input Leakage	V _{IN} =V _{SS} to V _{CCf} , V _{CCS}	-1.0	1.0	μA
I _{LO}	Output Leakage	V _{OUT} =V _{SS} to V _{CCf} , V _{CCS}	-1.0	1.0	μA
V _{IL}	Input Low Level		-0.3	0.5	V
V _{IH}	Input High Level		2.4	V _{CC} ± 0.3 ⁽²⁾	V
V _{ID}	Voltage for Sector Protection, and Temporary Sector Unprotection (RESET) ⁽¹⁾		11.5	12.5	V
V _{ACC}	Voltage for Program Acceleration (WP/ACC) ⁽¹⁾		8.5	9.5	V
V _{OL}	Output Low Level Flash	V _{CCf} = V _{CCf} min, I _{OL} = 4.0mA	—	0.45	V
V _{OH}	Output High Level Flash	V _{CCf} = V _{CCf} min, I _{OH} = -0.1mA	0.85 V _{CCf}	—	V
V _{OL}	Output Low Level SRAM	V _{CCS} = V _{CCS} min I _{OL} = 1.0mA	—	0.4	V
V _{OH}	Output High Level SRAM	V _{CCS} = V _{CCS} min I _{OH} = -0.5mA	2.2	—	V
V _{LKO}	Flash Low V _{CCf}		2.3	2.5	V

Notes:

1. Applicable for only V_{CCf} applying.
2. V_{CC} indicates lower of V_{CCf} or V_{CCS}.

FLASH DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _{LIT}	RESET Inputs Leakage Current	V _{ccf} =V _{ccf} max., V _{ccs} =V _{ccs} max. RESET = 12.5V	—	35	μA
I _{LIA}	ACC Inputs Leakage Current	V _{ccf} =V _{ccf} max., V _{ccs} =V _{ccs} max. WP/ACC = V _{acc} max.	—	20	μA
I _{cc1f}	FLASH V _{cc} ⁽¹⁾ Active Current (Read)	CEf=V _{IL} tCycle = 5Mhz Byte OE=V _{IH} tCycle = 5Mhz Word tCycle = 1Mhz Byte tCycle = 1Mhz Word	— — — —	16 18 4 4	mA
I _{cc2f}	FLASH V _{cc} Active ⁽²⁾ Current(Program/Erase)	CEf=V _{IL} OE=V _{IH}	—	35	mA
I _{cc3f}	FLASH V _{cc} Active ⁽⁴⁾ Current (Read-While-Program)	CEf=V _{IL} Byte OE=V _{IH} Word	—	51 53	mA
I _{cc4f}	FLASH V _{cc} Active ⁽⁴⁾ Current (Read-While-Erase)	CEf=V _{IL} Byte OE=V _{IH} Word	—	51 53	mA
I _{cc5f}	FLASH V _{cc} Active Current (Erase-Suspend-Program)	CEf=V _{IL} OE=V _{IH}	—	40	mA
I _{sb1f}	FLASH V _{cc} Standby Current	V _{ccf} = V _{cc} max, CEf= V _{ccf} = ± 0.3V RESET, CEf, WP/ACC = V _{ccf} = ± 0.3V	—	5	μA
I _{sb2f}	FLASH V _{cc} Standby Current (RESET)	V _{ccf} = V _{cc} max, RESET= V _{ss} = ± 0.3V WP/ACC = V _{ccf} = ± 0.3V	—	5	μA
I _{sb3f}	FLASH V _{cc} ⁽³⁾ Standby Current (Auto Sleep Mode)	V _{ccf} = V _{cc} max. CEf, = V _{ss} = ± 0.3V RESET, WP/ACC = V _{ccf} = ± 0.3V V _{IN} = V _{ccf} ± 0.3V OR V _{ss} ± 0.3V	—	5	μA

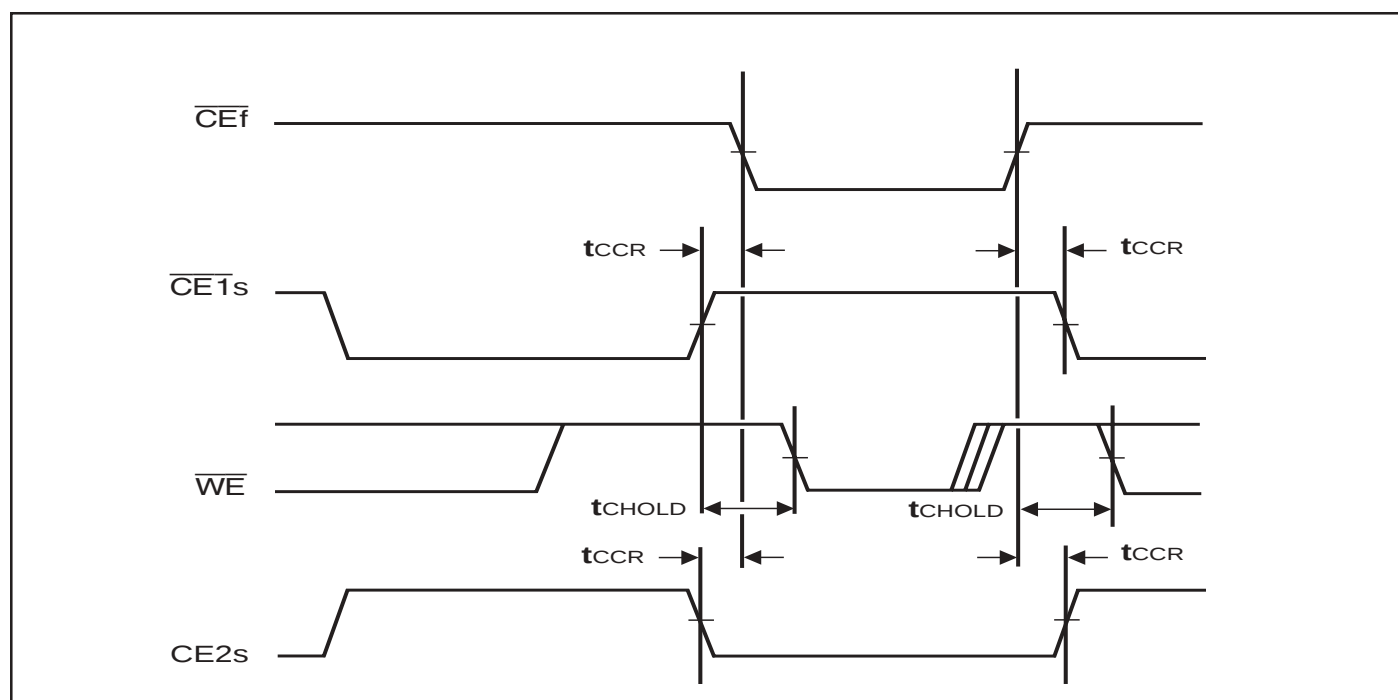
Notes:

1. The ICC current listed includes both the DC operating current and the frequency dependent component.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns..
4. Embedded Algorithm (program or erase) is in progress. (@5 MHz)

AC CHARACTERISTICS - $\overline{CE}$ TIMING

Parameter	JEDEC Symbol	Standard Symbol	Condition	Min	Unit
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	ns
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	ns

TIMING DIAGRAM FOR ALTERNATING SRAM TO FLASH



FLASH READ ONLY SWITCHING CHARACTERISTICS

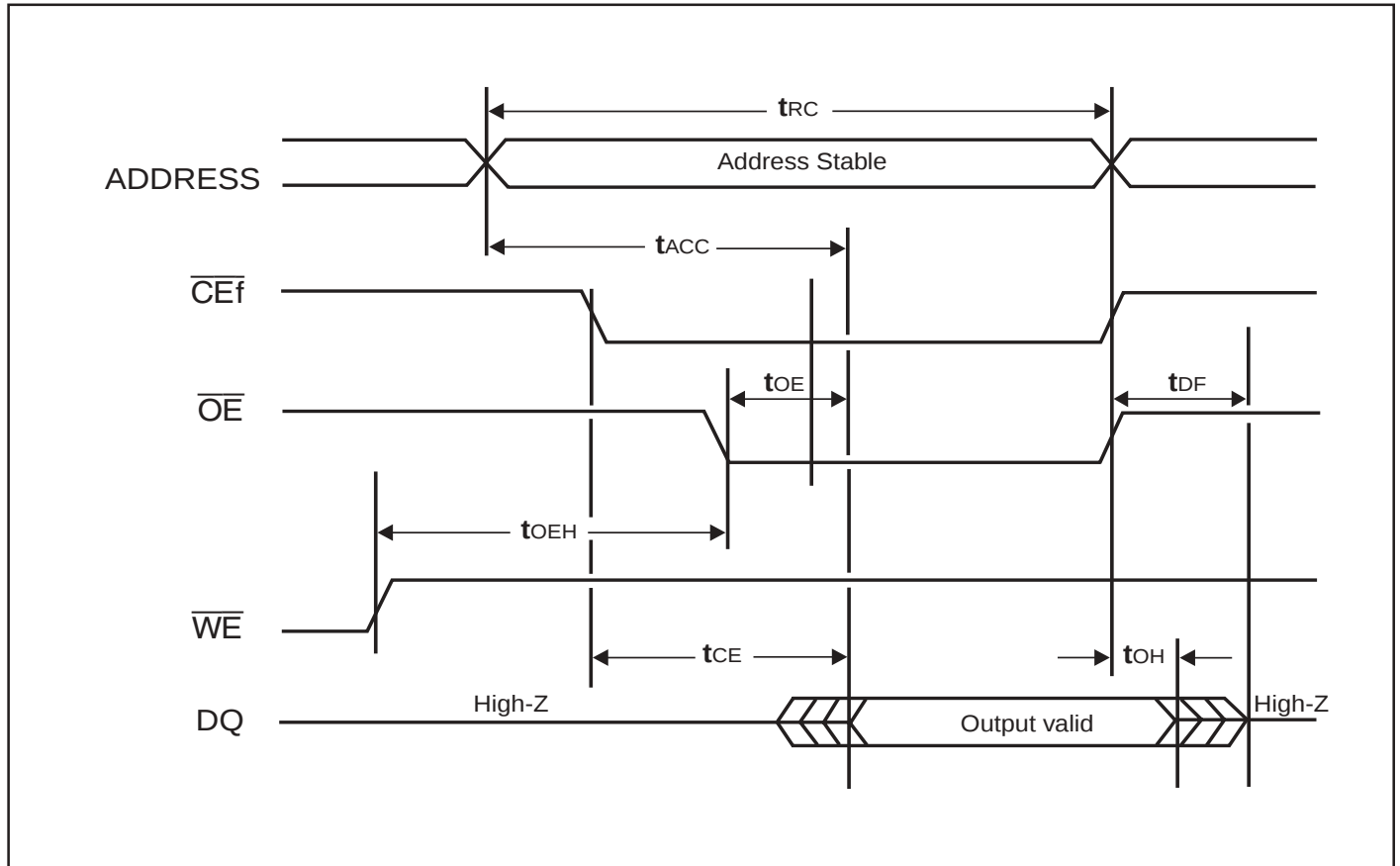
(Over Operating Range)

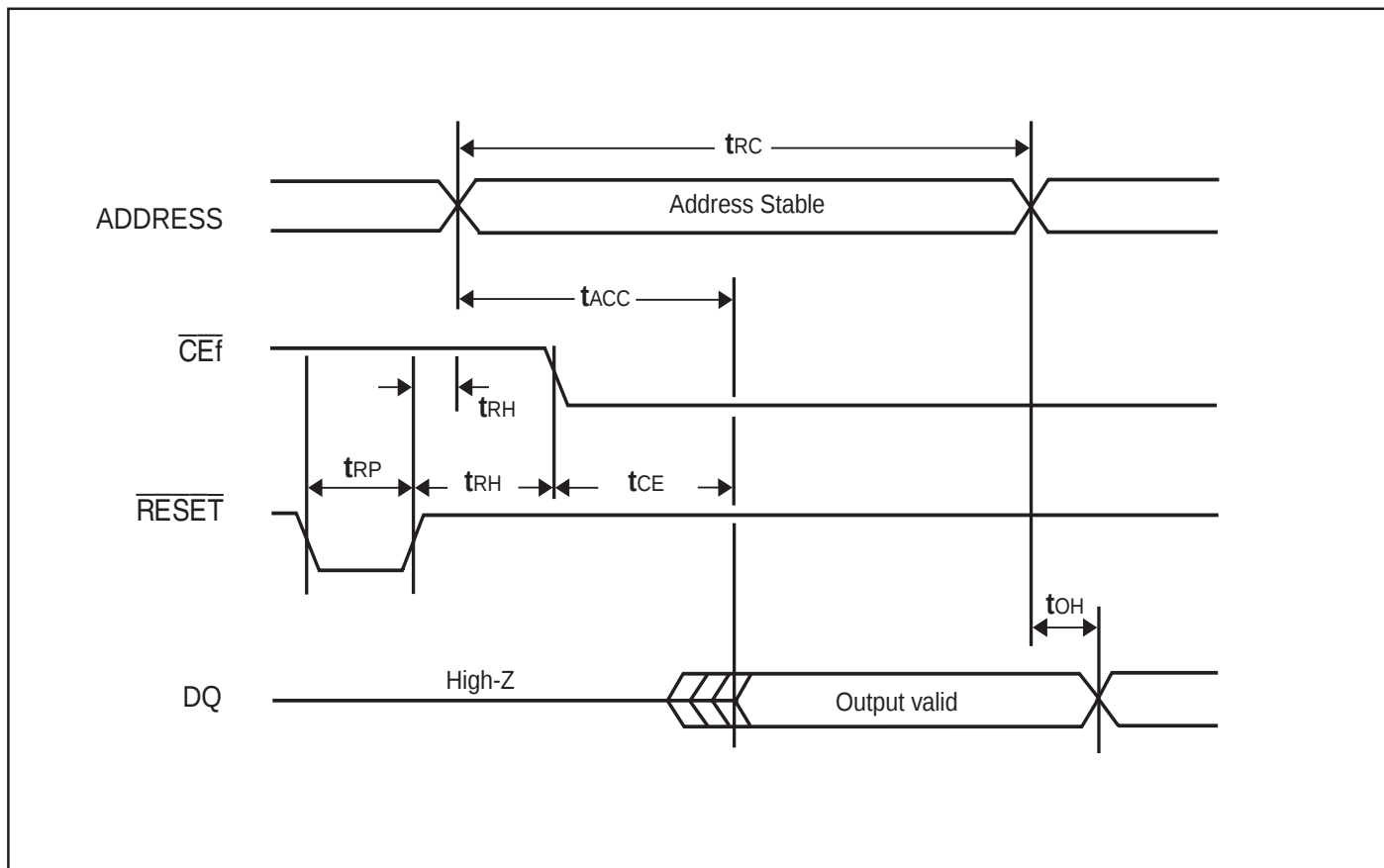
Symbol	Parameter	Min.	Max.	Unit
t _{RC}	Cycle Time	70		ns
t _{ACC}	Address to Output Delay	—	70	ns
t _{CE}	Chip Enable to Output Delay	—	70	ns
t _{OE}	Output Enable to Output Delay	—	30	ns
t _{DF}	Chip Enable to Output High-Z	—	25	ns
t _{DF}	Output Enable to Output High-Z	—	25	ns
t _{OH}	Output Hold Time from Addresses, $\overline{\text{CE}}$ or $\overline{\text{OE}}$, Whichever Occurs First	0	—	ns
t _{READY}	$\overline{\text{RESET}}$ Pin Low to Read Mode	—	20	μs

FLASH AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.1V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	V _{ccf} /2
Output Load	1 TTL gate and 30pF

FLASH READ CYCLE



FLASH HARDWARE $\overline{\text{RESET}}$ / READ OPERATION TIMING DIAGRAM

FLASH Erase/Program Operation Characteristics (Over Operating Range)

Symbol	Parameter	-70 ns		Unit
		Min.	Max.	
t _{WC}	Write Cycle Time	70	-	ns
t _{AS}	Address Setup Time ($\overline{WE}$ to Addr.)	0	-	ns
t _{ASO}	Address Setup Time to $\overline{CEf}$ Low During Toggle Bit Polling	12	-	ns
t _{AH}	Address Hold Time ($\overline{WE}$ to Addr.)	45	-	ns
t _{AHT}	Address Hold Time from $\overline{CEf}$ or $\overline{OE}$ High During Toggle Bit Polling	0	-	ns
t _{DS}	Data Setup Time	30	-	ns
t _{DH}	Data Hold Time	0	-	ns
t _{oES}	Output Enable Setup Time	0	-	ns
t _{oEH}	Output Enable Hold Time Read	0	-	ns
t _{oEH}	Output Enable Hold Time Toggle and Data Polling	10	-	ns
t _{CEPH}	$\overline{CEf}$ High During Toggle Bit Polling	20	-	ns
t _{OEPH}	$\overline{OE}$ High During Toggle Bit Polling	20	-	ns
t _{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CEf}$)	0	-	ns
t _{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)	0	-	ns
t _{WS}	WE Setup Time ($\overline{CEf}$ to $\overline{WE}$)	0	-	ns
t _{CS}	$\overline{CEf}$ Setup Time ($\overline{WE}$ to $\overline{CEf}$)	0	-	ns
t _{WH}	$\overline{WE}$ Hold Time ($\overline{CEf}$ to $\overline{WE}$)	0	-	ns
t _{CH}	$\overline{CEf}$ Hold Time ($\overline{WE}$ to $\overline{CEf}$)	0	-	ns
t _{WP}	Write Pulse Width	35	-	ns
t _{CP}	$\overline{CEf}$ Pulse Width	35	-	ns
t _{WPH}	Write Pulse Width High	25	-	ns
t _{CPH}	$\overline{CEf}$ Pulse Width High	25	-	ns
t _{WHWH1}	Byte Programming Operation	-	12	μs
t _{WHWH1}	Word Programming Operation	-	15	μs
t _{WHWH2}	Sector Erase Operation ⁽¹⁾	-	0.7	s
t _{VCS}	V _{ccf} Setup Time	50	-	μs

Note:

1. This reflects typical value not maximum value and does not include the preprogramming time.

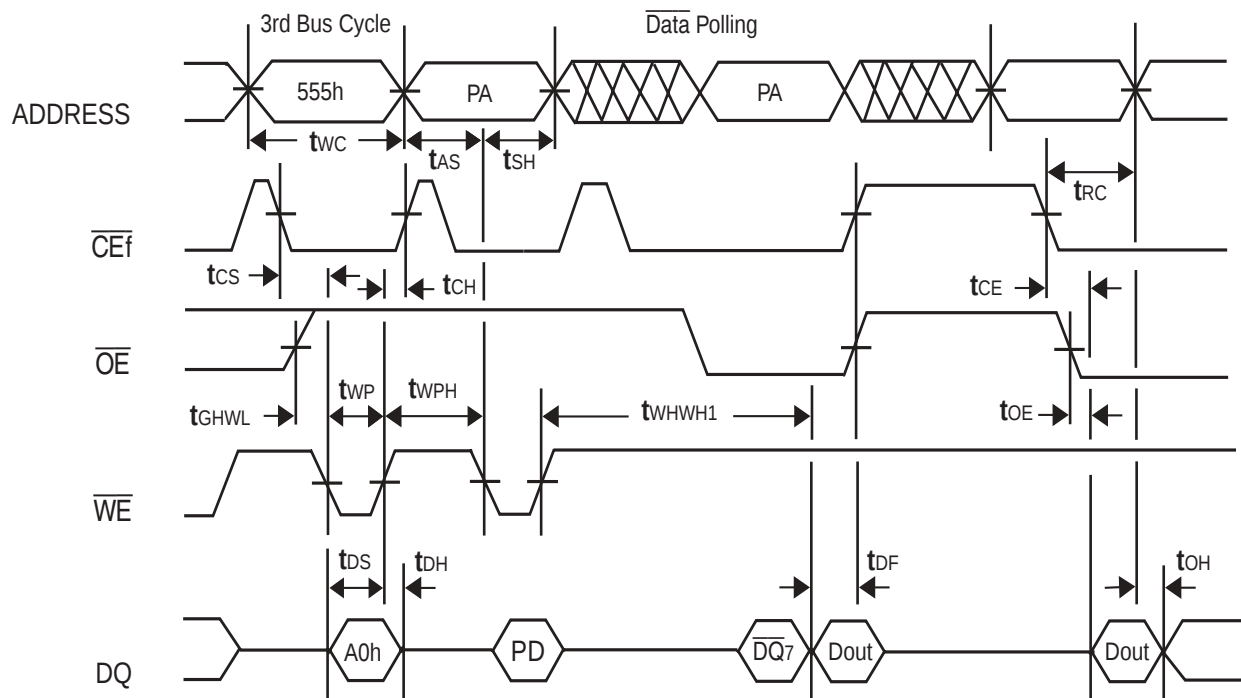
FLASH Erase/Program Operation Characteristics Continued (Over Operating Range)

Symbol	Parameter	-70 ns		Unit
		Min.	Max.	
t _{VLHT}	Voltage Transition Time ⁽²⁾	4	-	μs
t _{VIDR}	Rise Time to V _{ID} ⁽²⁾	500	-	ns
t _{VACCR}	Rise Time to V _{ACC}	500	-	ns
t _{RB}	Recovery Time from RY/ $\overline{\text{BY}}$	0	-	ns
t _{RP}	$\overline{\text{RESET}}$ Pulse Width	500	-	ns
t _{EOE}	Delay Time from Embedded Output Enable	-	70	ns
t _{RH}	$\overline{\text{RESET}}$ High Level Period Before Read	200	-	ns
t _{BUSY}	Program/Erase Valid to RY/ $\overline{\text{BY}}$ Delay	-	90	ns
t _{TOW}	Erase Time-out Time ⁽³⁾	50	-	μs
t _{SPD}	Erase Suspend Transition Time ⁽⁴⁾	-	20	μs

Note:

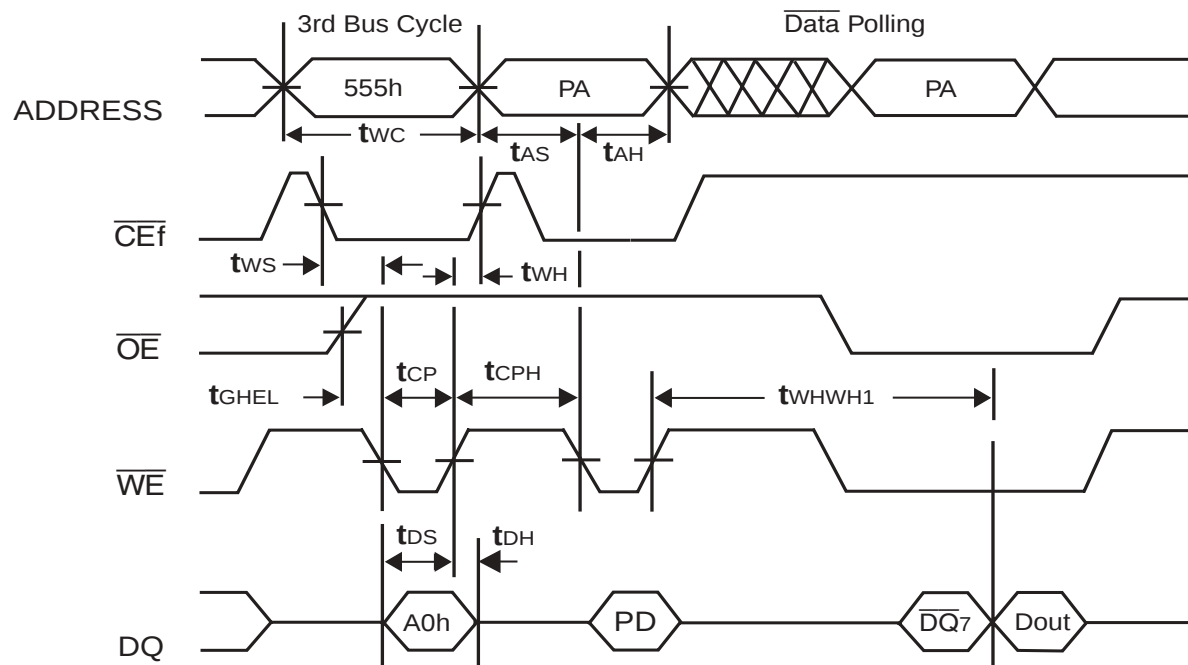
2. This timing is for Sector Protection Operation.
3. The time between writes must be less than "t_{TOW}" otherwise that command will not be accepted and erasure will start. A time-out or "t_{TOW}" from the rising edge of last $\overline{\text{CE}}$ or $\overline{\text{WE}}$ whichever happens first will initiate the execution of the Sector Erase command(s).
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t_{SPD}" to suspend the erase operation.

FLASH WRITE CYCLE

($\overline{\text{WE}}$ Control)**Notes:**

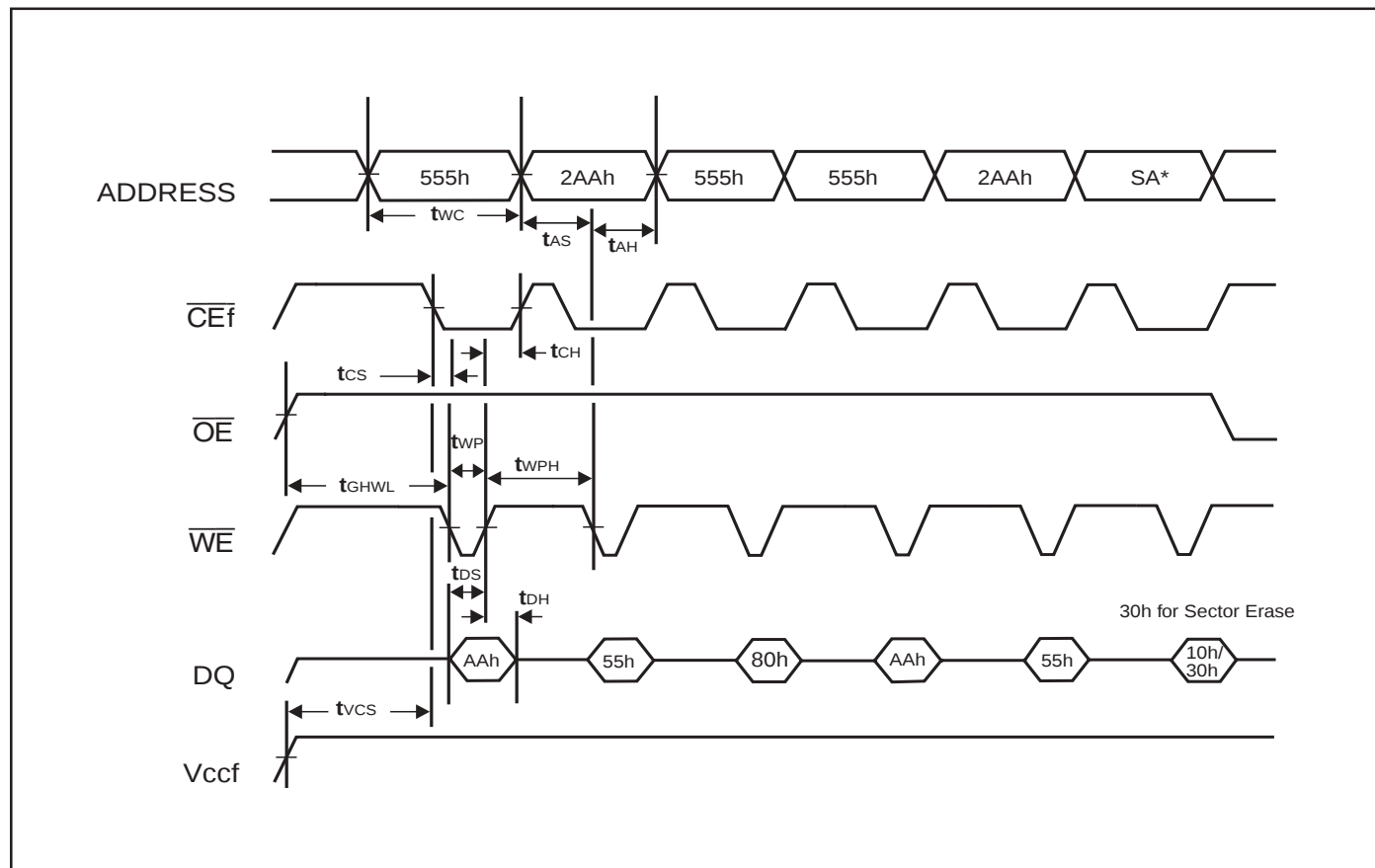
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the $\times 16$ mode (the addresses differ from $\times 8$ mode, i.e. AAAh).

FLASH WRITE CYCLE

($\overline{\text{CEf}}$ Control)**Notes:**

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the $\times 16$ mode (the addresses differ from $\times 8$ mode, i.e. AAAh).

FLASH AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

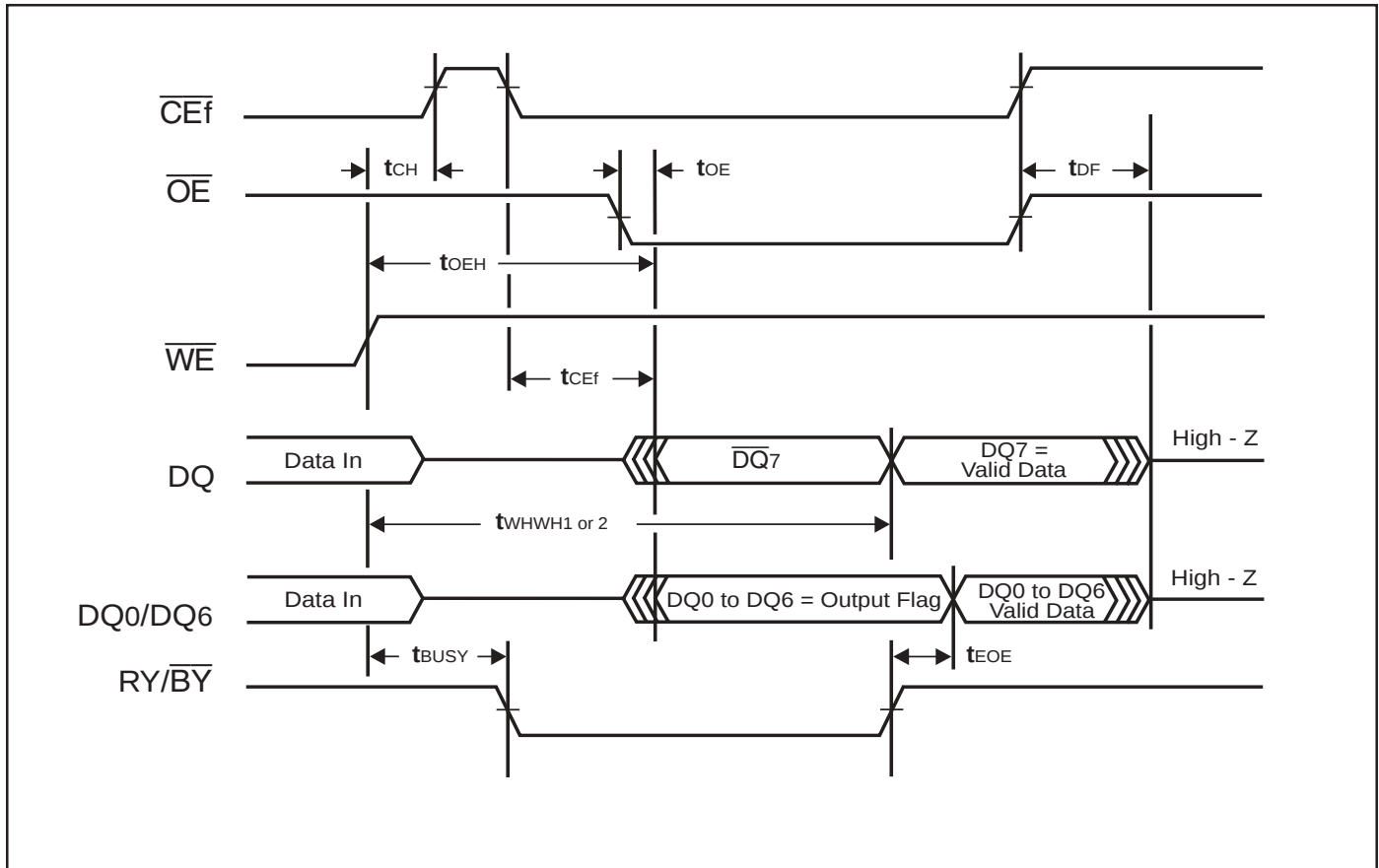


*SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

Note:

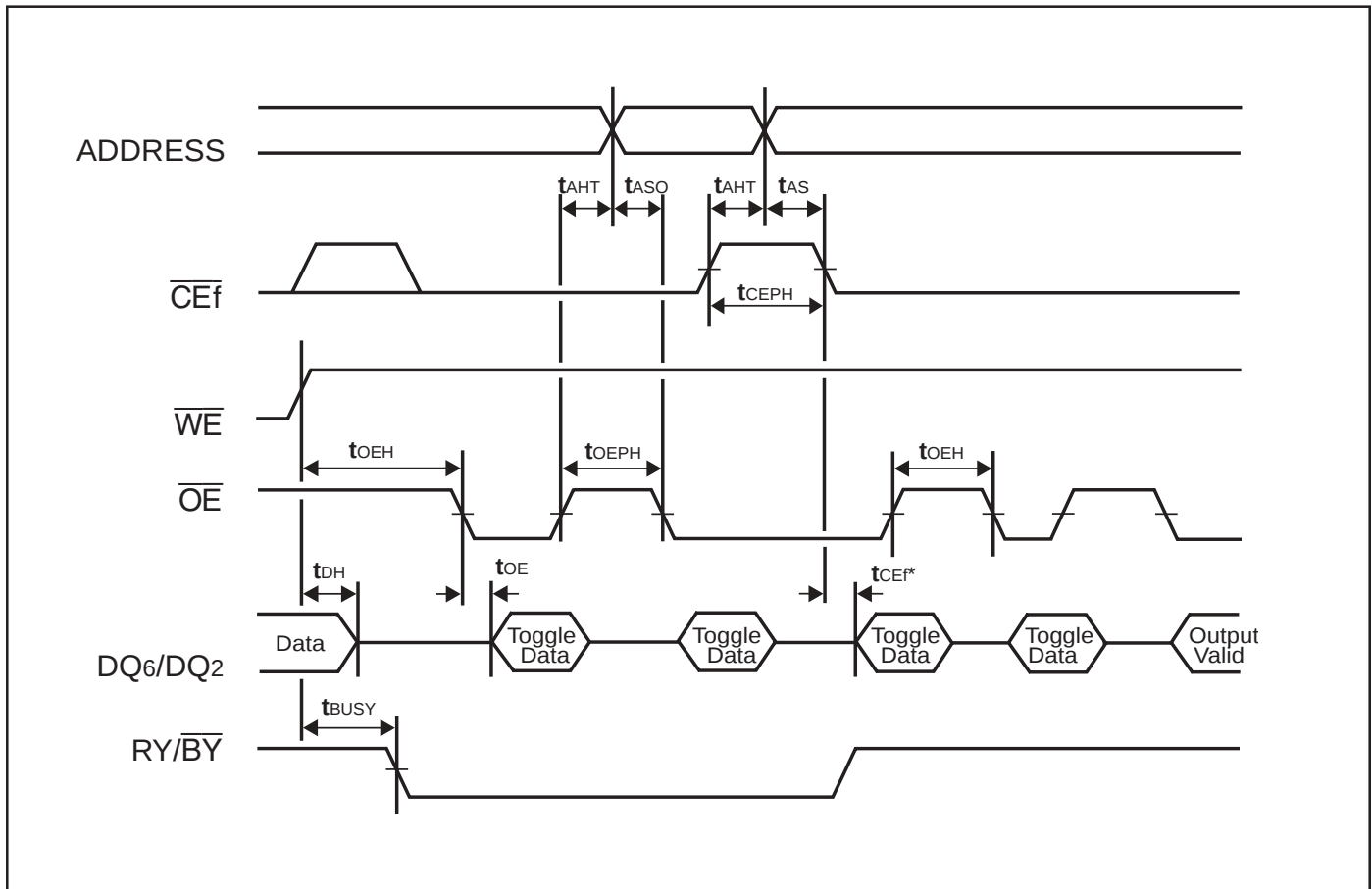
These waveforms are for the ×16 mode (the addresses differ from ×8 mode: AAh, 555h, AAh, AAh, 555h, SA*).

FLASH AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALOGRITHM OPERATIONS



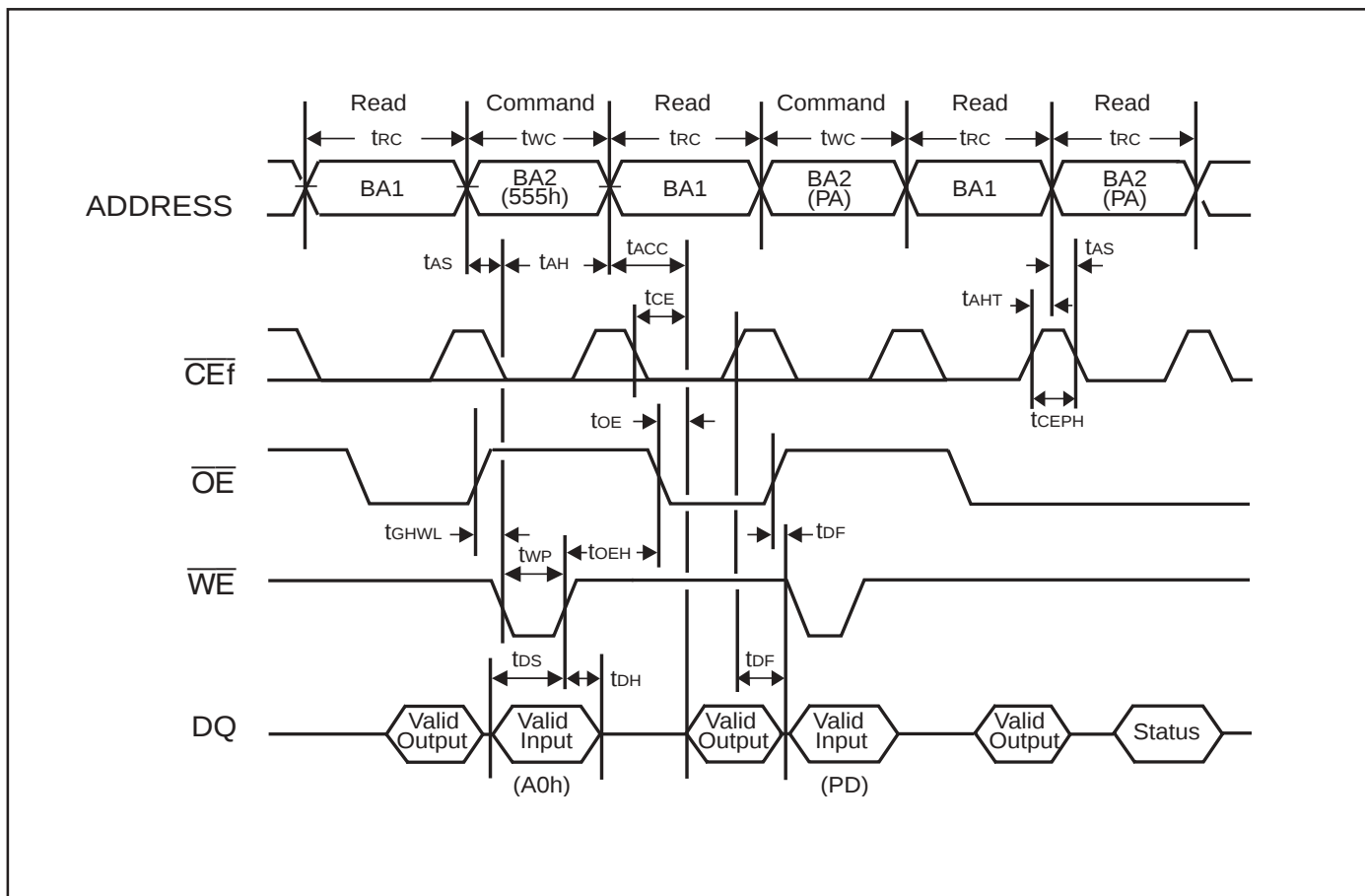
*DQ7 = Valid Data (the device has completed the Embedded operation.)

FLASH AC WAVEFORMS FOR TOGGLE BIT DURING EMBEDDED ALGORITHM OPERATIONS



* DQ6 stops toggling (the device has completed the Embedded operation).

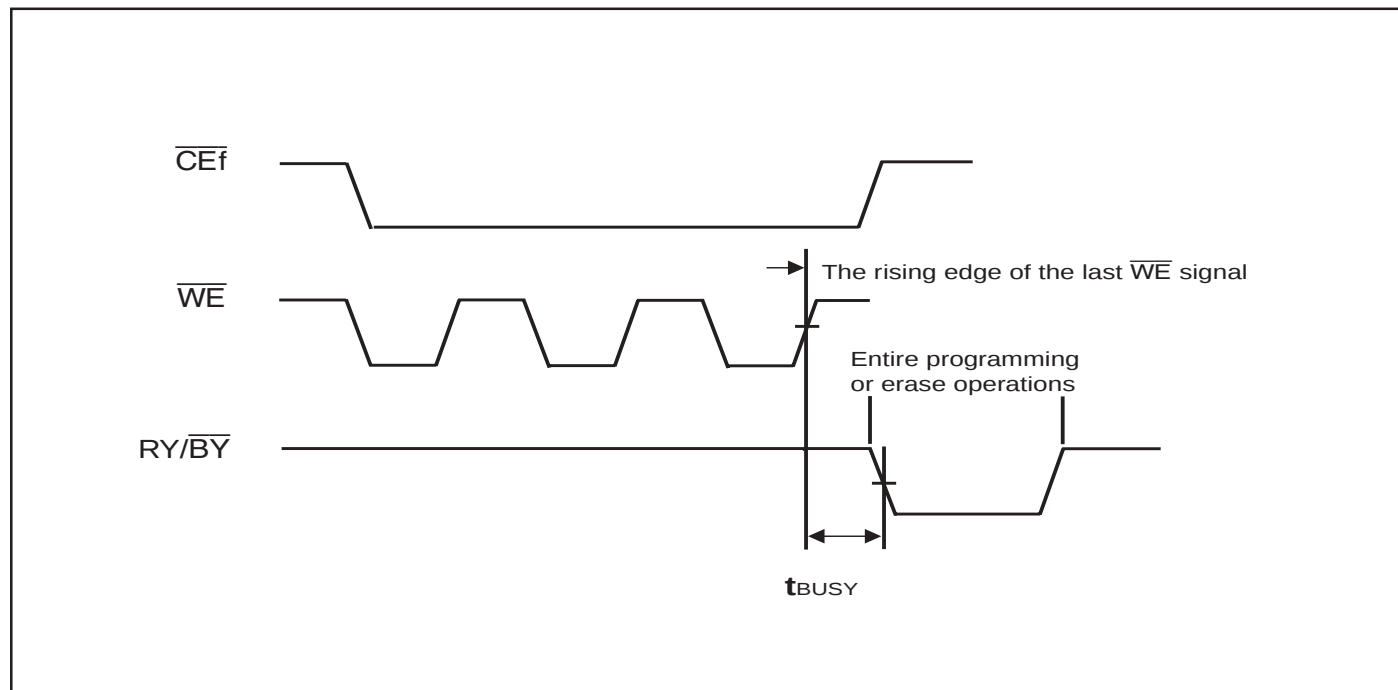
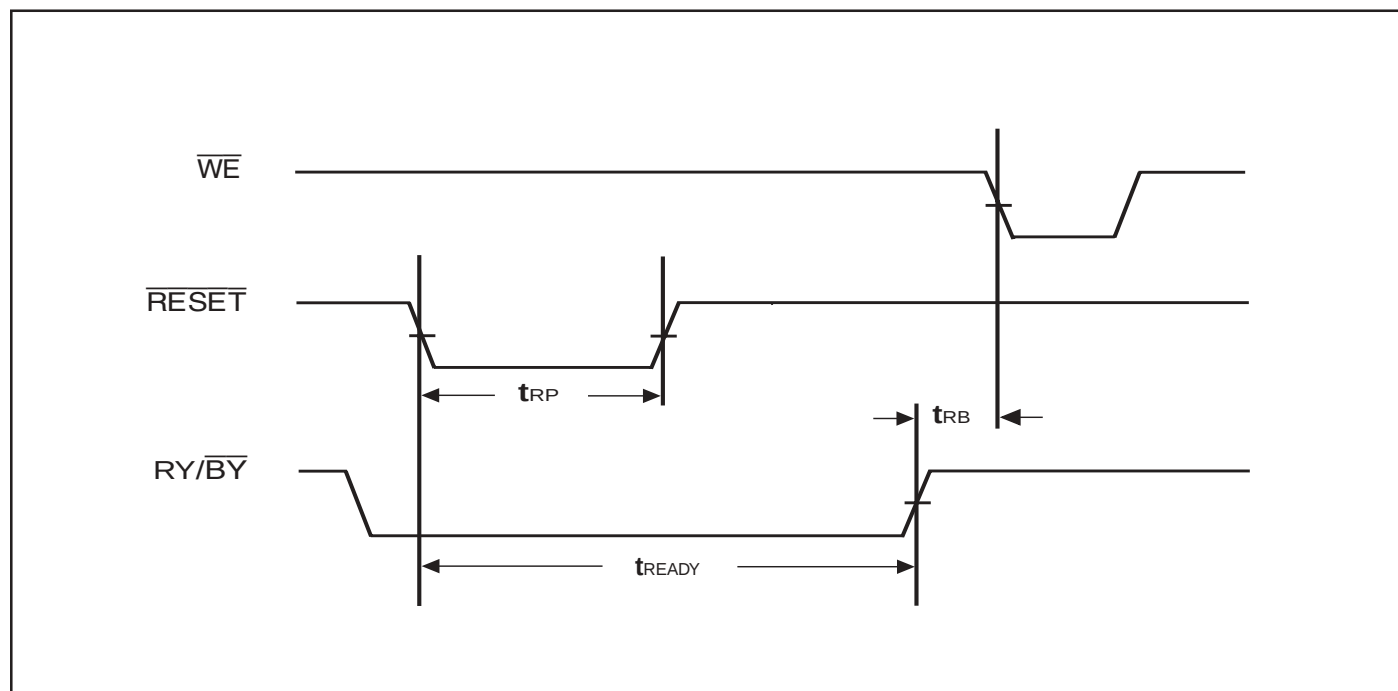
FLASH BACK-TO-BACK READ/WRITE TIMING DIAGRAM

**Note:**

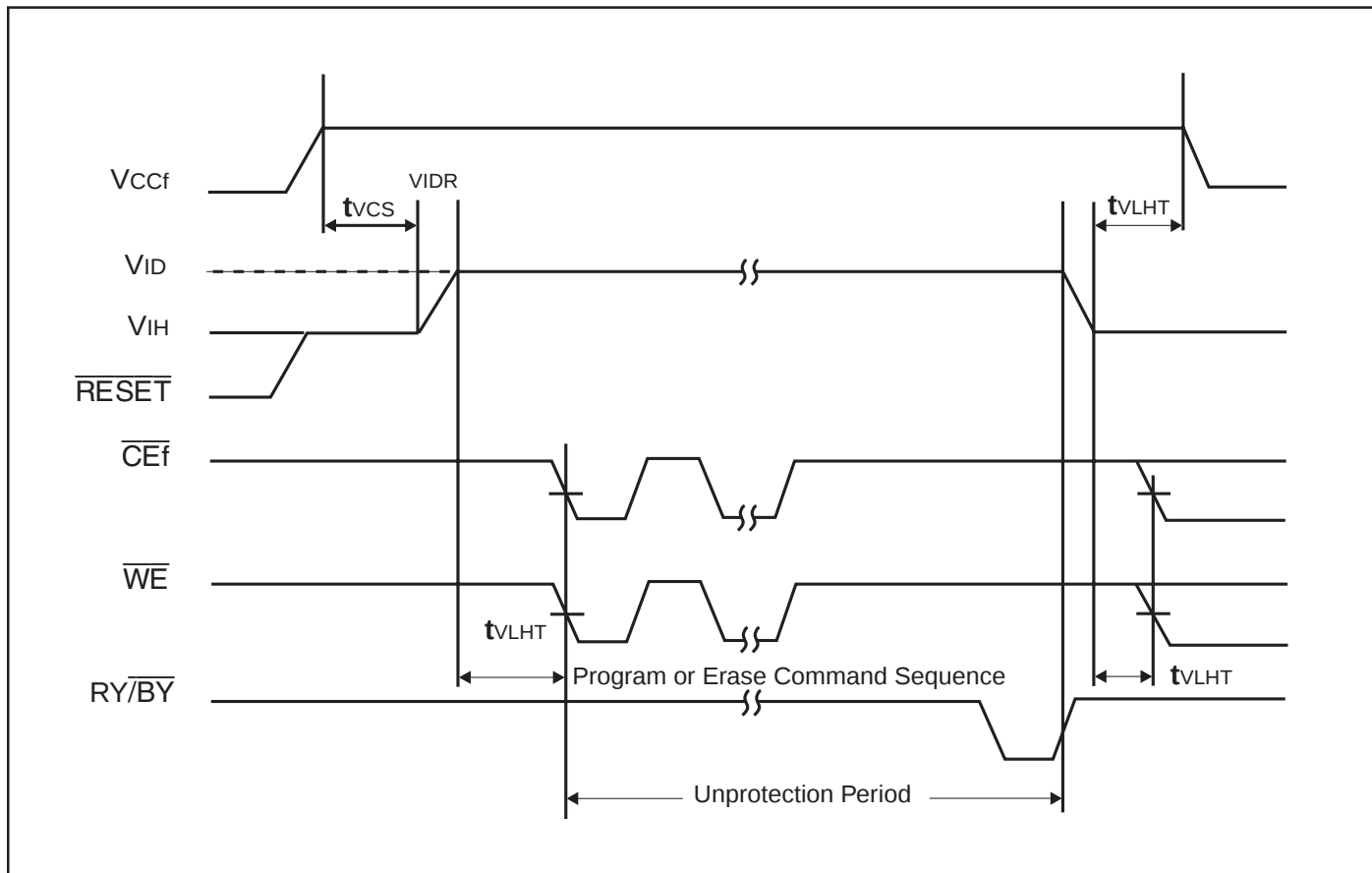
This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.

BA1: Address of Bank 1.

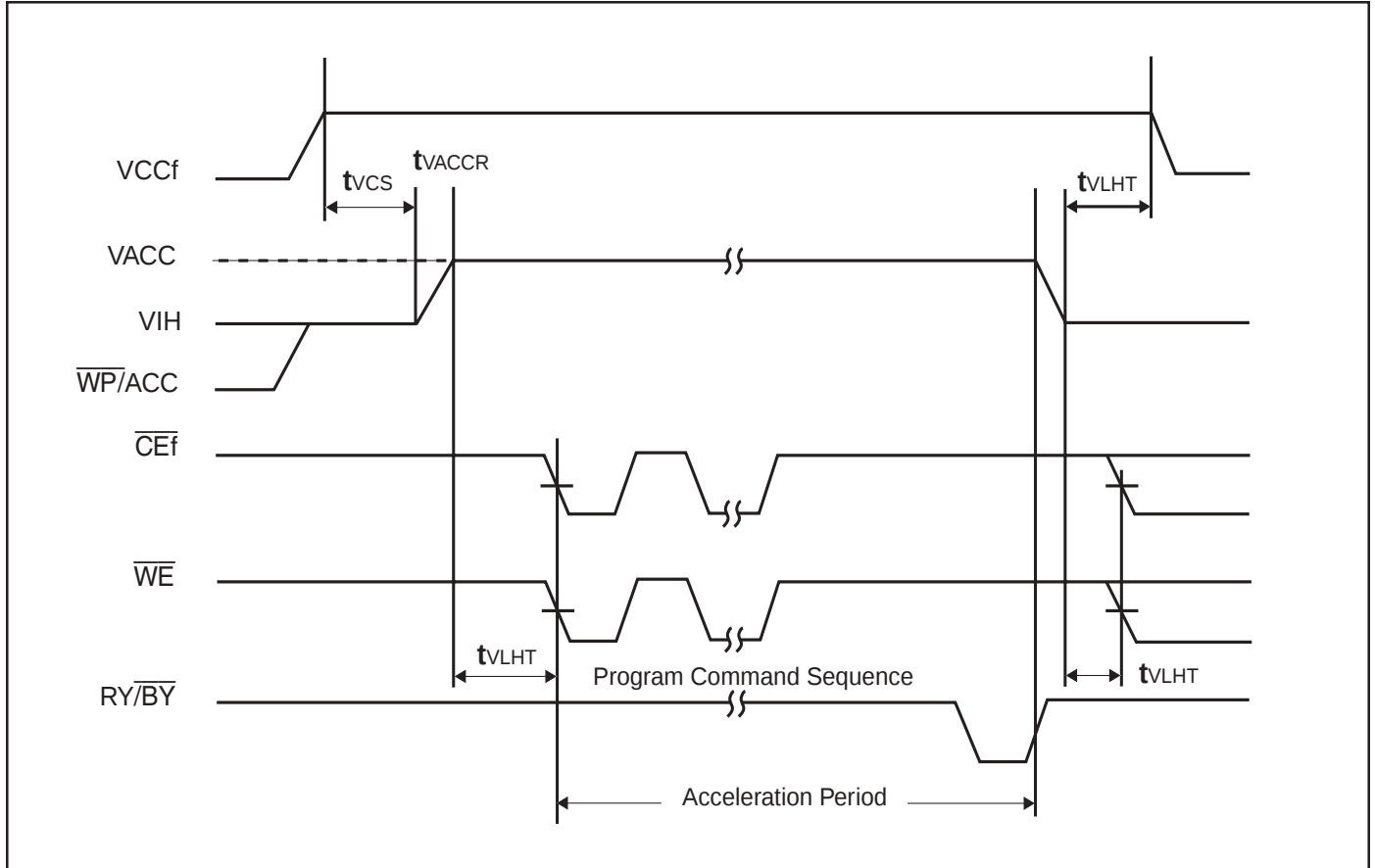
BA2: Address of Bank 2.

FLASH RY/ $\overline{\text{BY}}$ TIMING DIAGRAM DURING WRITE/ERASE OPERATIONSFLASH $\overline{\text{RESET}}$ RY/ $\overline{\text{BY}}$ TIMING DIAGRAM

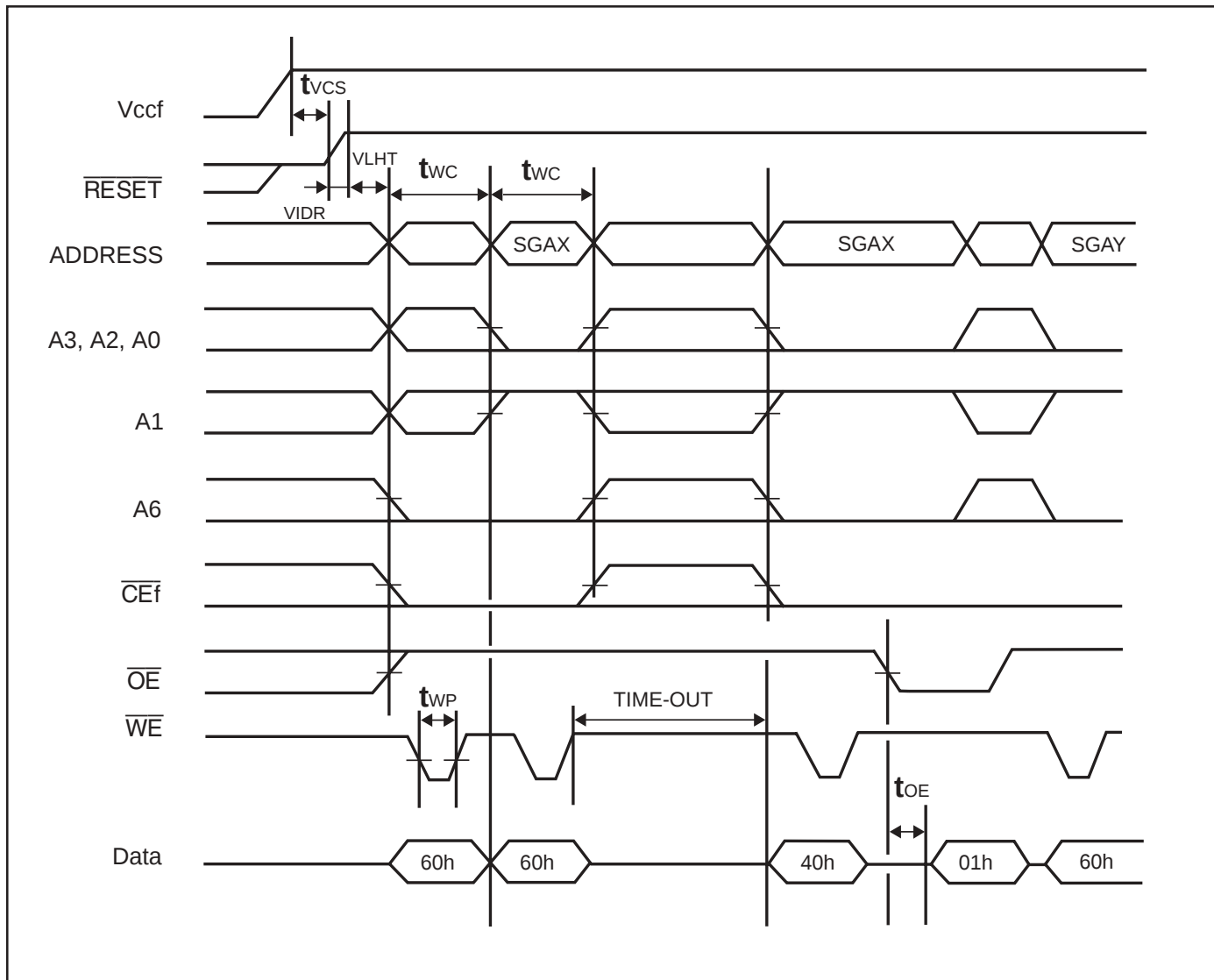
FLASH TEMPORARY SECTOR GROUP UNPROTECTION



FLASH ACCELERATED PROGRAM



FLASH EXTENDED SECTOR GROUP PROTECTION



SGAx: Sector Group Address to be protected. SGAY: Next Group Sector Address to be protected

UNPROTECTION: Implement with A6 = 1, A1 = 1, A0 = 0. Time-out approximately 15 ms.

TIME-OUT : Time-Out window = 250 μ s (Min.)

SRAM POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _{CC}	V _{CC} Dynamic Operating Supply Current	V _{CCS} = Max., f = 10Mhz	—	50	mA
I _{CC1}	Operating Supply Current	V _{CCS} = Max., f = 1Mhz	—	10	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CCS} = Max., $\overline{CE1}_s \geq V_{CCS} - 0.2V$, $CE2_s \leq 0.2V$, $V_{IN} \geq V_{CCS} - 0.2V$, or $V_{IN} \leq 0.2V$ f = 0	—	15	μA

Note:

1. f = 0 means no input lines change.

SRAM READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	70 ns		Unit
		Min.	Max.	
t _{RC}	Read Cycle Time	70	—	ns
t _{AA}	Address Access Time	—	70	ns
t _{OHA}	Output Hold Time	10	—	ns
t _{ACE1}	$\overline{CE1}_s$ Access Time	—	70	ns
t _{DOE}	$\overline{OE}$ Access Time	—	35	ns
t _{HZOE} ⁽²⁾	$\overline{OE}$ to High-Z Output	—	25	ns
t _{LZOE} ⁽²⁾	$\overline{OE}$ to Low-Z Output	0	—	ns
t _{HZCE1} ⁽²⁾	$\overline{CE1}_s$ to High-Z Output	0	25	ns
t _{LZCE1} ⁽²⁾	$\overline{CE1}_s$ to Low-Z Output	5	—	ns
t _{BA}	$\overline{LB}_s, \overline{UB}_s$ Access Time	—	70	ns
t _{HZB}	$\overline{LB}_s, \overline{UB}_s$ to High-Z Output	0	25	ns
t _{LZB}	$\overline{LB}_s, \overline{UB}_s$ to Low-Z Output	0	—	ns

Notes:

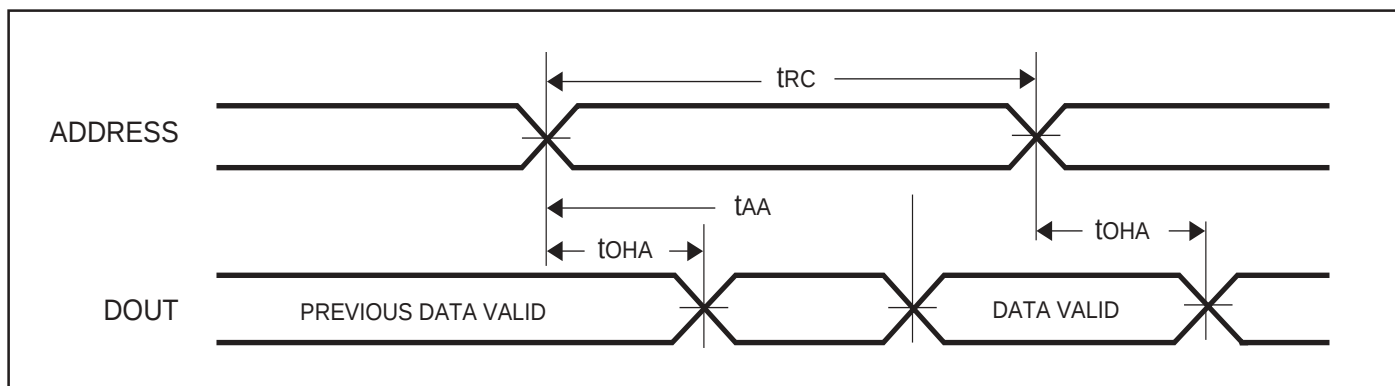
1. See SRAM AC TEST CONDITIONS.
2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

SRAM AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	V _{CCS} /2
Output Load	1 TTL gate and 30pF

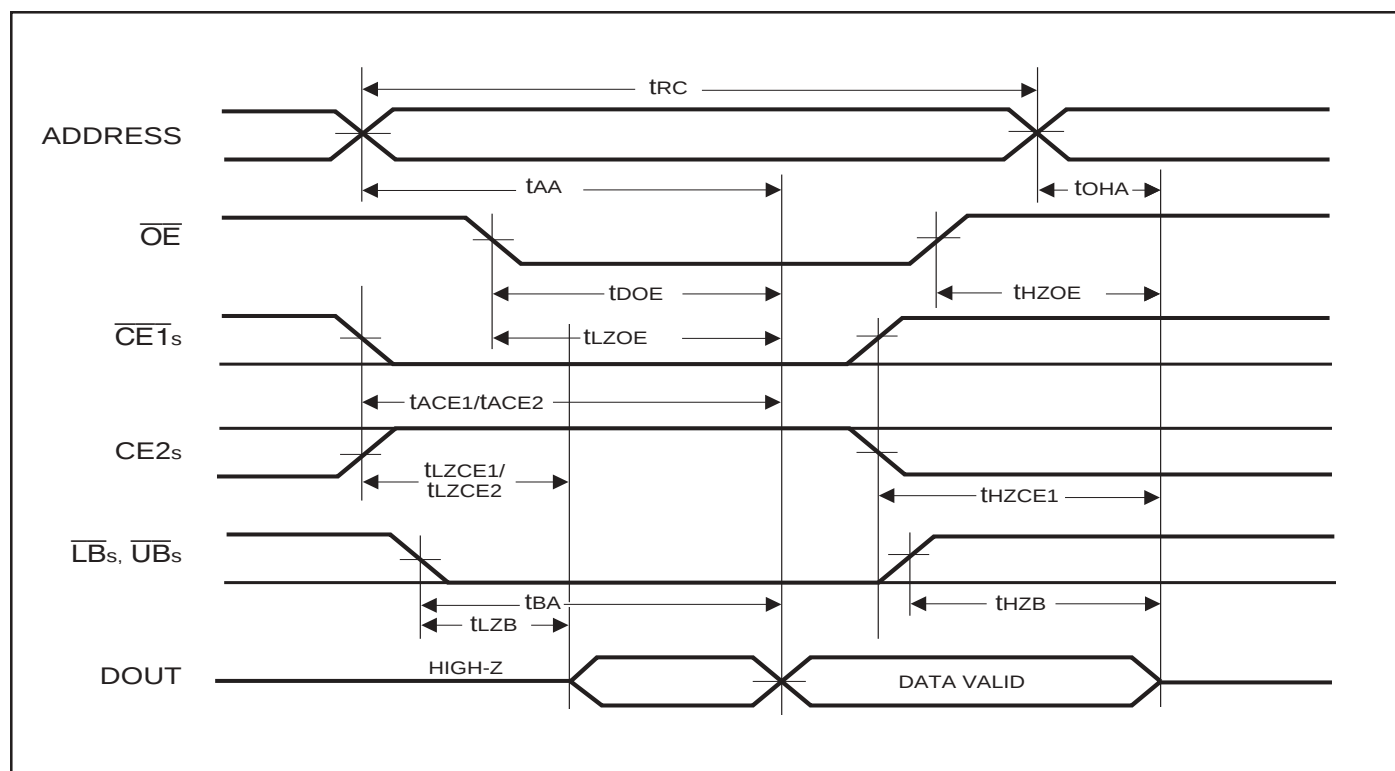
AC WAVEFORMS

SRAM READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE1}_s = \overline{OE} = V_{IL}$, $\overline{UB}_s$ or $\overline{LB}_s = V_{IL}$)



AC WAVEFORMS

SRAM READ CYCLE NO. 2^(1,3) ($\overline{CE1}_s$, $\overline{OE}$, AND $\overline{UB}_s / \overline{LB}_s$ Controlled)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}_s$, $\overline{UB}_s$, or $\overline{LB}_s = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE1}_s$ LOW transition.

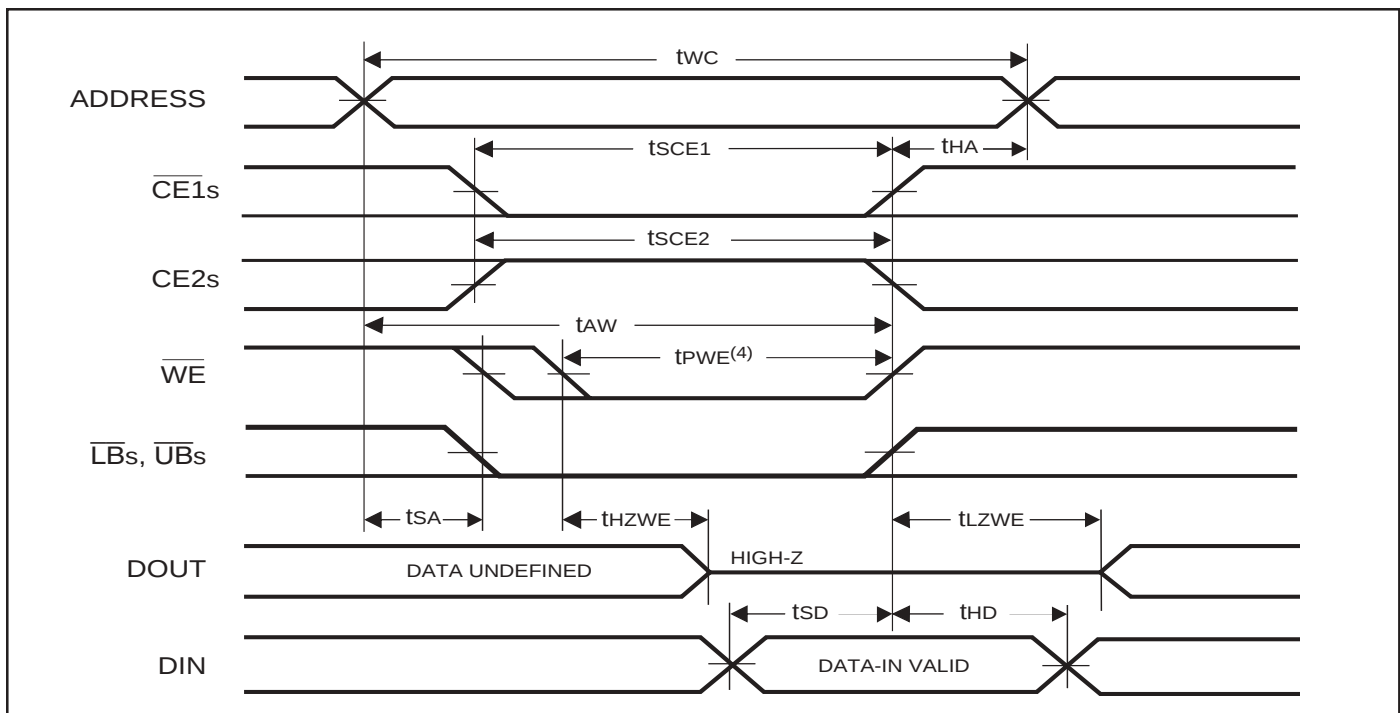
WRITE CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	70 ns		Unit
		Min.	Max.	
t _{WC}	Write Cycle Time	70	—	ns
t _{SCE1}	$\overline{CE1}_s$ to Write End	55	—	ns
t _{AW}	Address Setup Time to Write End	55	—	ns
t _{HA}	Address Hold from Write End	0	—	ns
t _{SA}	Address Setup Time	0	—	ns
t _{PWB}	$\overline{LB}_s, \overline{UB}_s$ Valid to End of Write	55	—	ns
t _{PWE}	$\overline{WE}$ Pulse Width	50	—	ns
t _{SD}	Data Setup to Write End	30	—	ns
t _{HD}	Data Hold from Write End	0	—	ns
t _{HZWE} ⁽²⁾	$\overline{WE}$ LOW to High-Z Output	—	25	ns
t _{LZWE} ⁽²⁾	$\overline{WE}$ HIGH to Low-Z Output	0	—	ns

Notes:

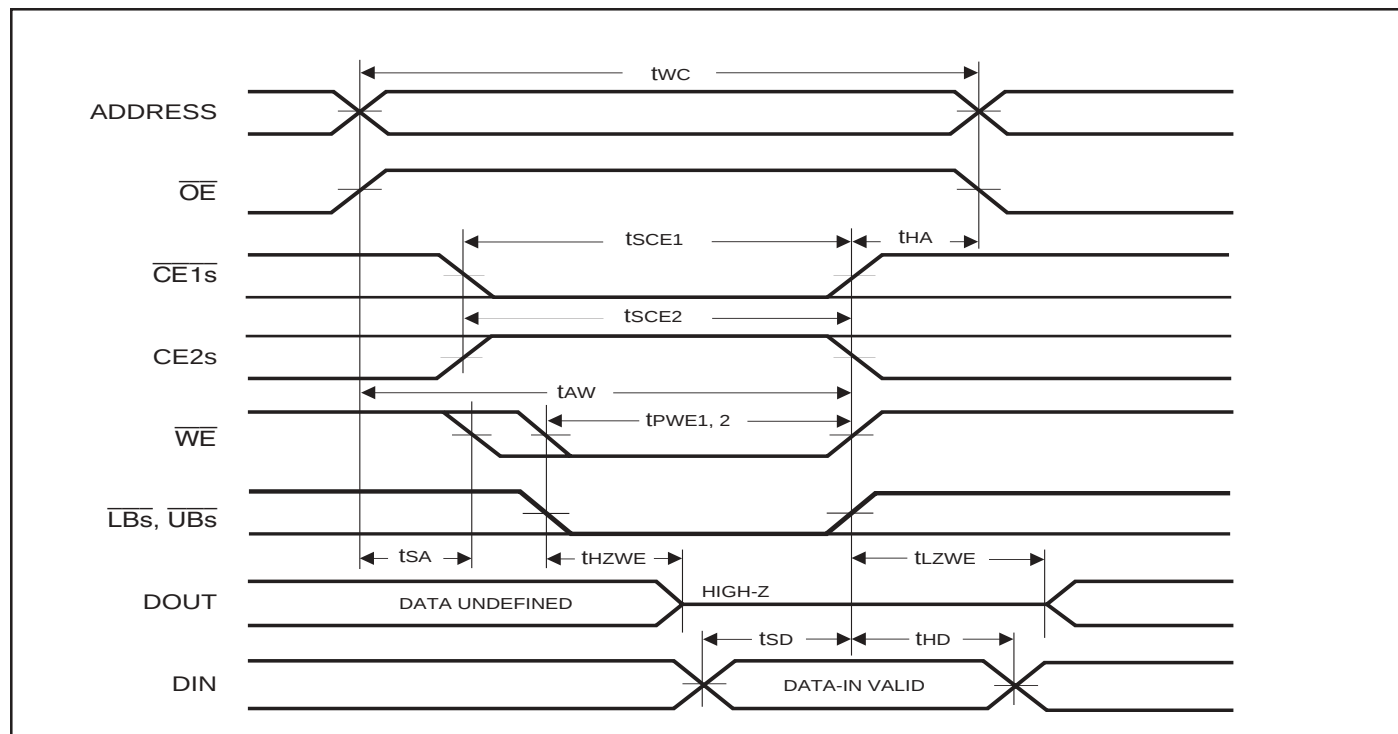
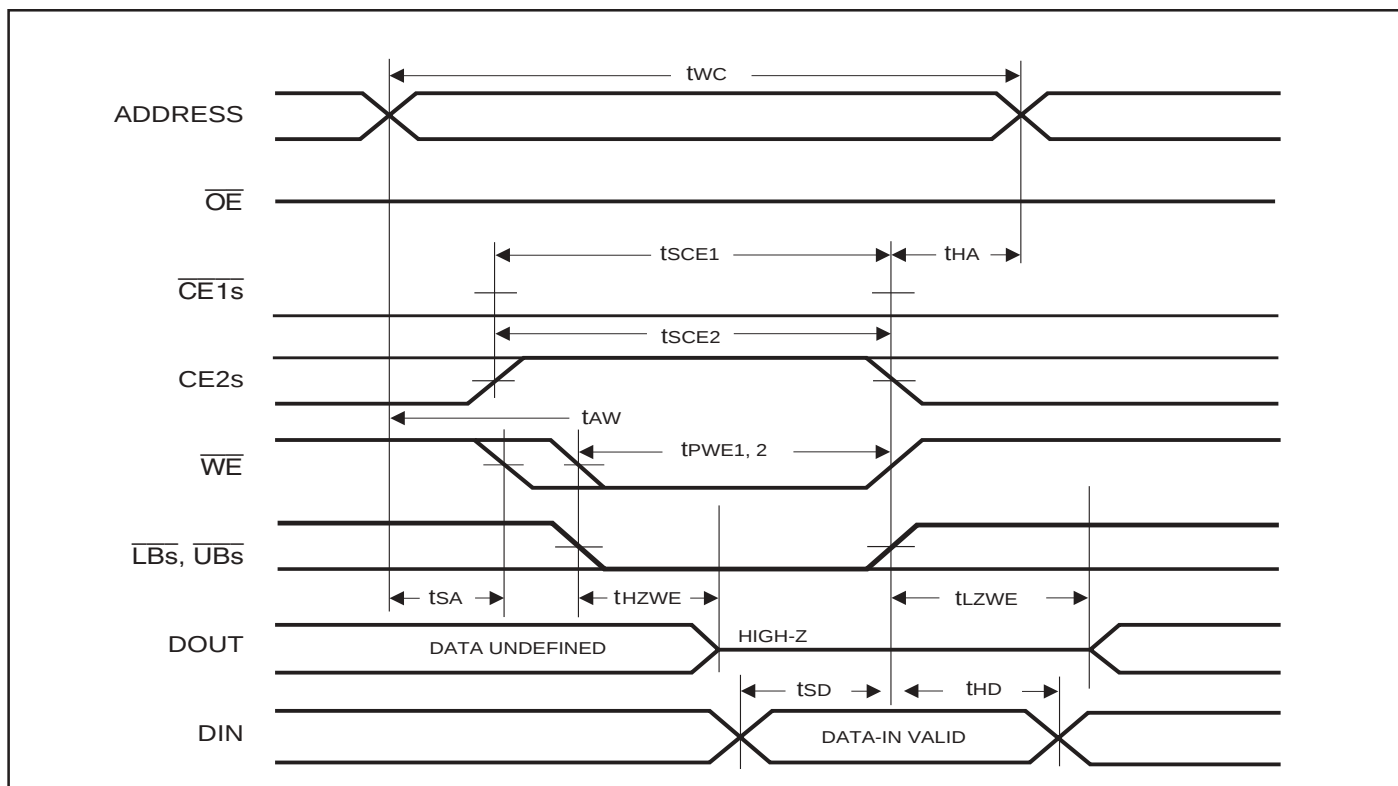
1. See SRAM AC TEST CONDITIONS.
2. Transition is measured ± 500 mV from steady-state voltage.

AC WAVEFORMS

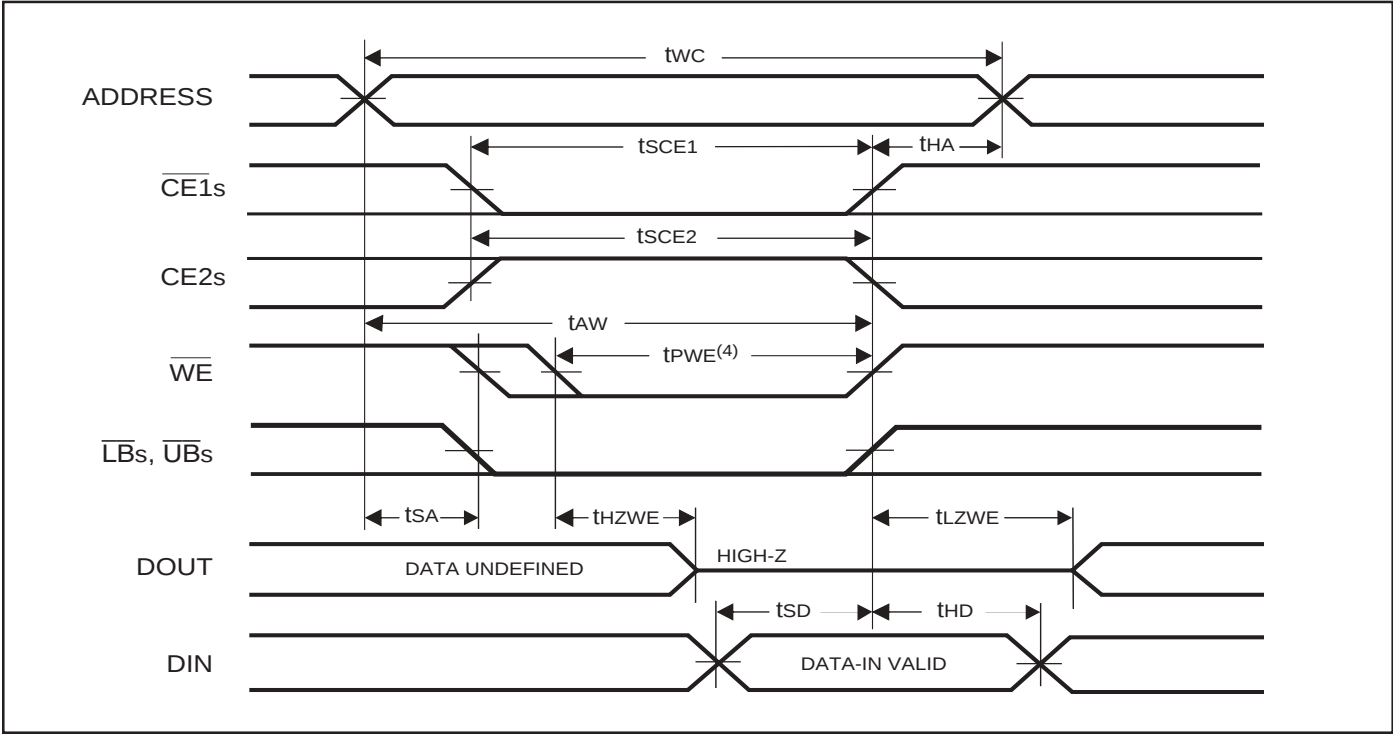
SRAM WRITE CYCLE NO. 1^(1,2) ($\overline{CE1}_s$ Controlled, $\overline{OE}$ = HIGH or LOW)

Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE1}_s$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}_s$ and $\overline{UB}_s$ inputs being in the LOW state.
2. WRITE = ($\overline{CE1}_s$) [($\overline{LB}_s$) = ($\overline{UB}_s$)] ($\overline{WE}$).

SRAM WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)

SRAM WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)


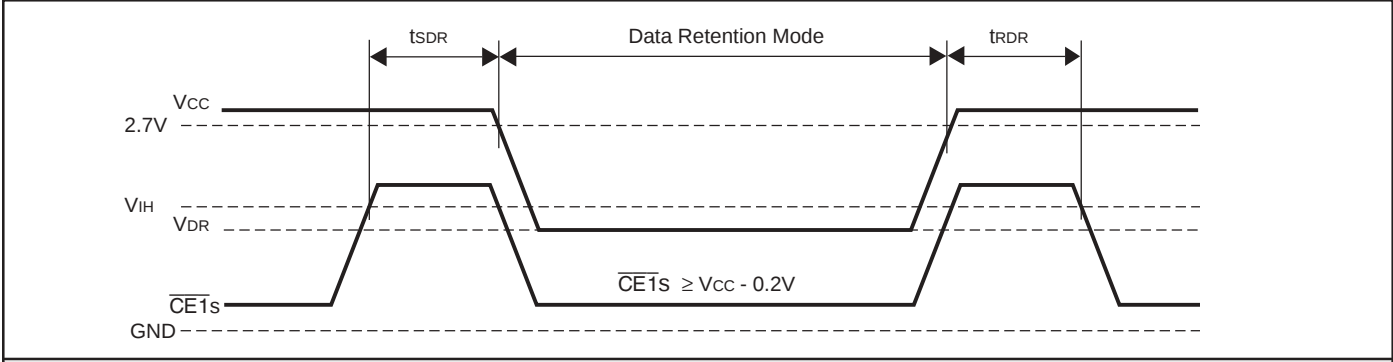
WRITE CYCLE NO. 4 ($\overline{UB}_s/\overline{LB}_s$ Controlled, $\overline{CE1}_s$ is LOW, $CE2_s$ is HIGH)

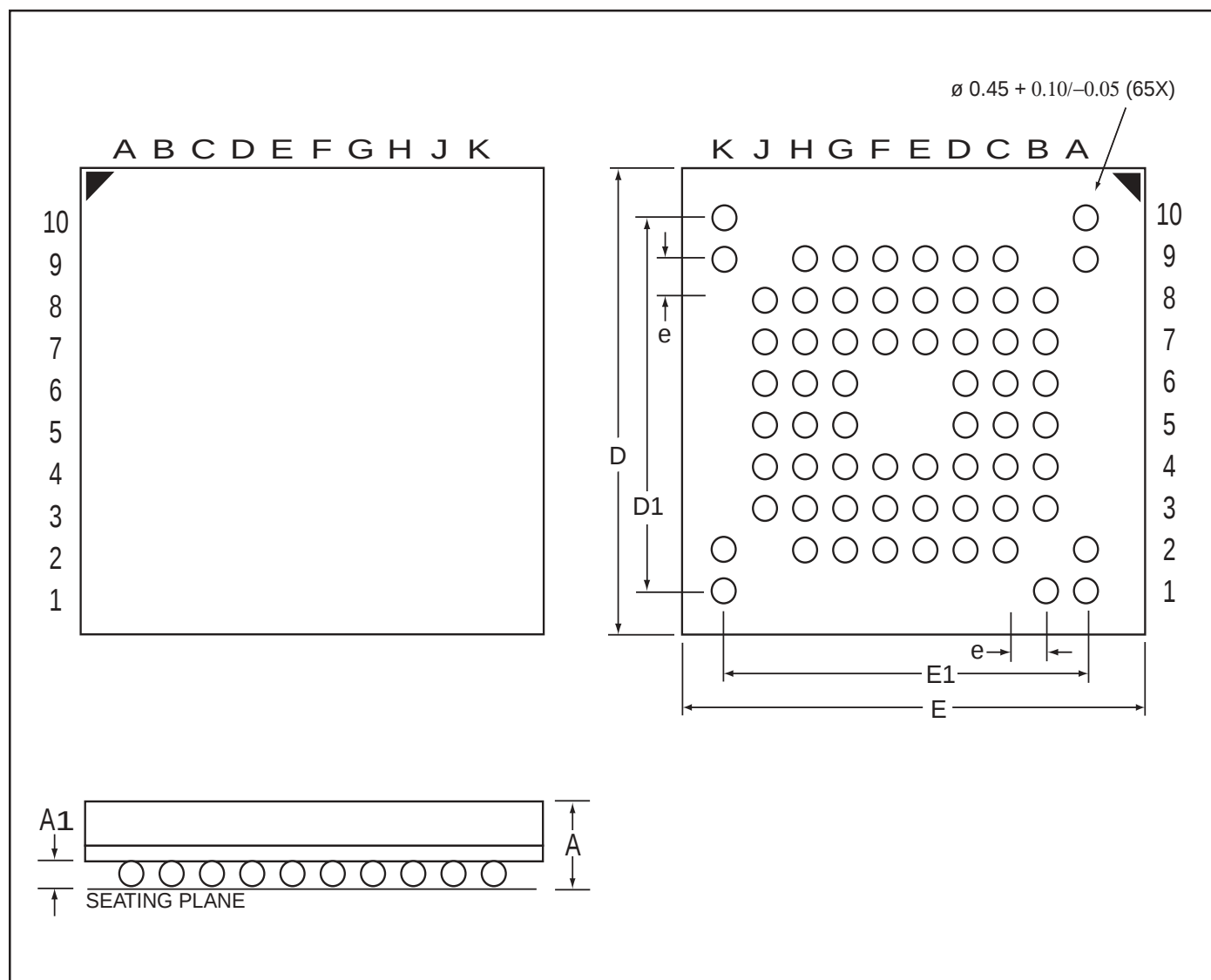


SRAM DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform	1.5	3.1	V
I_{DR}	Data Retention Current	$V_{CC} = 1.5V, \overline{CE1}_s \geq V_{CC} - 0.2V$	—	6	μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{rc}	—	ns

SRAM DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



BALL GRID ARRAY – 65-Ball FBGA**PACKAGE CODE: D - 9.0 mm x 9.0 mm Body, 0.8 mm Ball Pitch**

Symbol	Min.	Typ.	Max.	Units
A	1.09	1.19	1.34	mm
A1	0.29	0.39	0.49	mm
D	8.90	9.00	9.10	mm
D1	—	7.20	—	mm
E	8.90	9.00	9.10	mm
E1	—	7.20	—	mm
e	—	0.80	—	mm

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	SRAM Data Bus	Flash Bank Organization	Flash Speed(ns)	SRAM Speed(ns)	Package
IS71VPCF64GS08-7070DI	8/16	User Configurable	70	70	65-ball BGA