

## 3.0 Volt-Only Flash & SRAM COMBO with Stacked Multi-Chip Package (MCP) — 64 Mbit Simultaneous Operation Flash Memory and 8 Mbit Static RAM

PRELIMINARY INFORMATION  
JULY 2002

### MCP FEATURES

- Power supply voltage 2.7V to 3.3V
- High performance:  
Flash: 70 ns maximum access time  
SRAM: 70 ns maximum access time
- Package: 101-ball BGA & 73-ball BGA
- Industrial Temperature: -40C to +85C

### FLASH FEATURES

- Power Dissipation:  
Read Current at 1 Mhz: 7 mA maximum  
Read Current at 5 Mhz: 18 mA maximum  
Sleep Mode: 5  $\mu$ A maximum
- Simultaneous R/W Operations (dual virtual bank):  
Zero latency between read and write operations; Data can be programmed or erased in one bank while data is simultaneously being read from the other bank
- Low-Power Mode:  
A period of no activity causes flash to enter a low-power state
- Erase Suspend/Resume:  
Suspends of erase activity to allow a read in the same bank
- Sector Erase Architecture:  
16 words of 4k size and 126 words of 32K size (32 Mbit)  
Any combination of sectors, or the entire flash can be simultaneously erased
- Erase Algorithms:  
Automatically preprograms/erases the flash memory entirely, or by sector
- Program Algorithms:  
Automatically writes and verifies data at specified address
- Hidden ROM Region:  
256 byte with a Factory-serialized secure electronic serial number (ESN), which is accessible through a command sequence
- Data Polling and Toggle Bit:  
Allow for detection of program or erase cycle completion
- Ready-Busy output (RY/ $\overline{\text{BY}}$ )  
Detection of program or erase cycle completion

- Over 100,000 write/erase cycles
- Low supply voltage ( $V_{\text{ccf}} \leq 2.5\text{V}$ ) inhibits writes
- $\overline{\text{WP}}/\text{ACC}$  input pin:  
If  $V_{\text{IL}}$ , allows partial protection of boot sectors  
If  $V_{\text{IH}}$ , allows removal of boot sector protection  
If  $V_{\text{acc}}$ , program time is improved

### SRAM FEATURES (8 Mb density)

- Power Dissipation:  
Operating: 25 mA maximum  
Standby: 15  $\mu$ A maximum
- Chip Selects:  $\overline{\text{CE}}1\text{s}$ ,  $\text{CE}2\text{s}$
- Power down feature using  $\overline{\text{CE}}1\text{s}$ , or  $\text{CE}2\text{s}$ , or  $\overline{\text{LBs}}$  &  $\overline{\text{UBs}}$
- Data retention supply voltage: 1.0 to 3.3 volt
- Byte data control:  $\overline{\text{LBs}}$  (DQ0–DQ7),  $\overline{\text{UBs}}$  (DQ8–DQ15) — on x16 version

### GENERAL DESCRIPTION

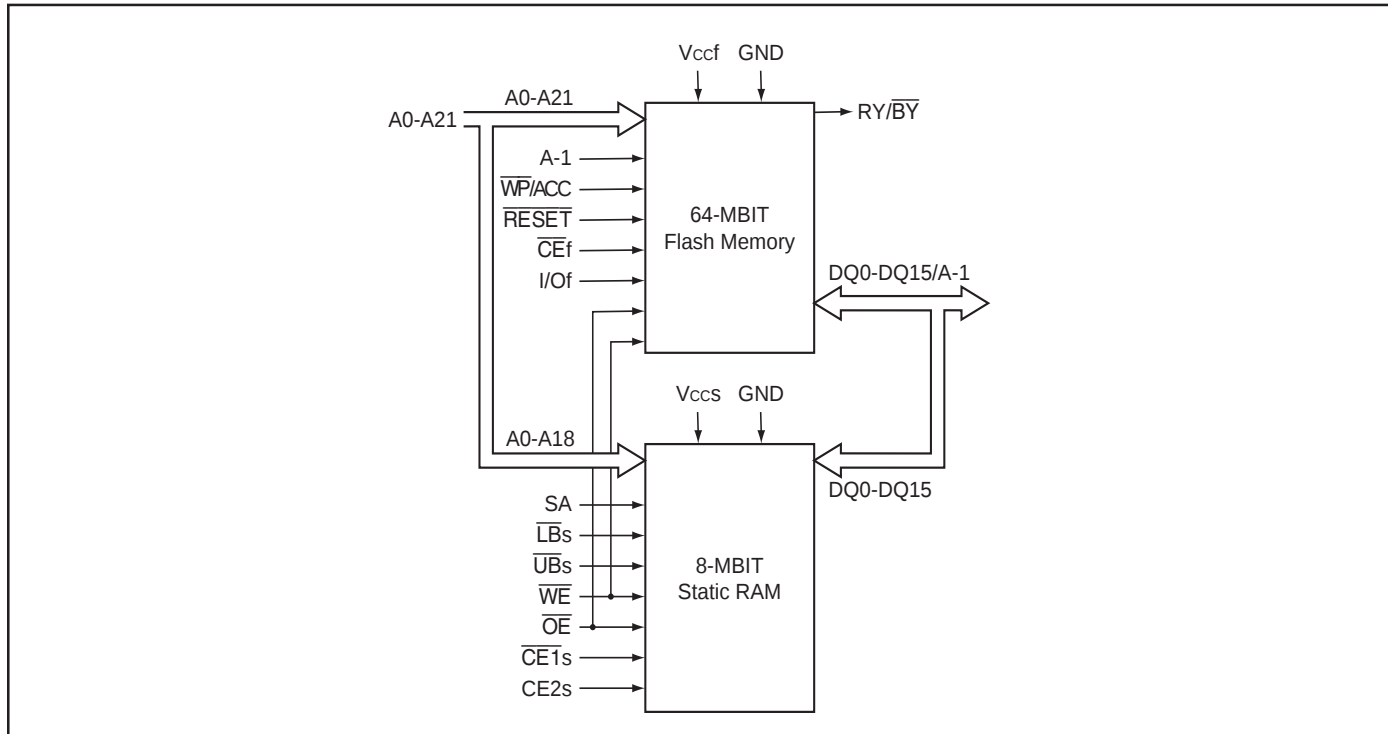
The flash and SRAM MCP is available in 64 Mbit Flash/8 Mbit SRAM, with a data bus of either x8 or x16. The 64 Mbit flash is composed of 4,194,304 words of 16 bits or 8,388,608 bytes of 8 bits. The 8Mbit SRAM has 524,288 words of 16 bits or 1,048,576 bytes of 8 bits. Data lines DQ0-DQ7 handle the x8 format, while lines DQ0-DQ15 handle the x16 format.

The package uses a 3.0V power supply for all operations. No other source is required for program and erase operations. The flash can be programmed in system using this 3.0V supply, or can be programmed in a standard EPROM programmer.

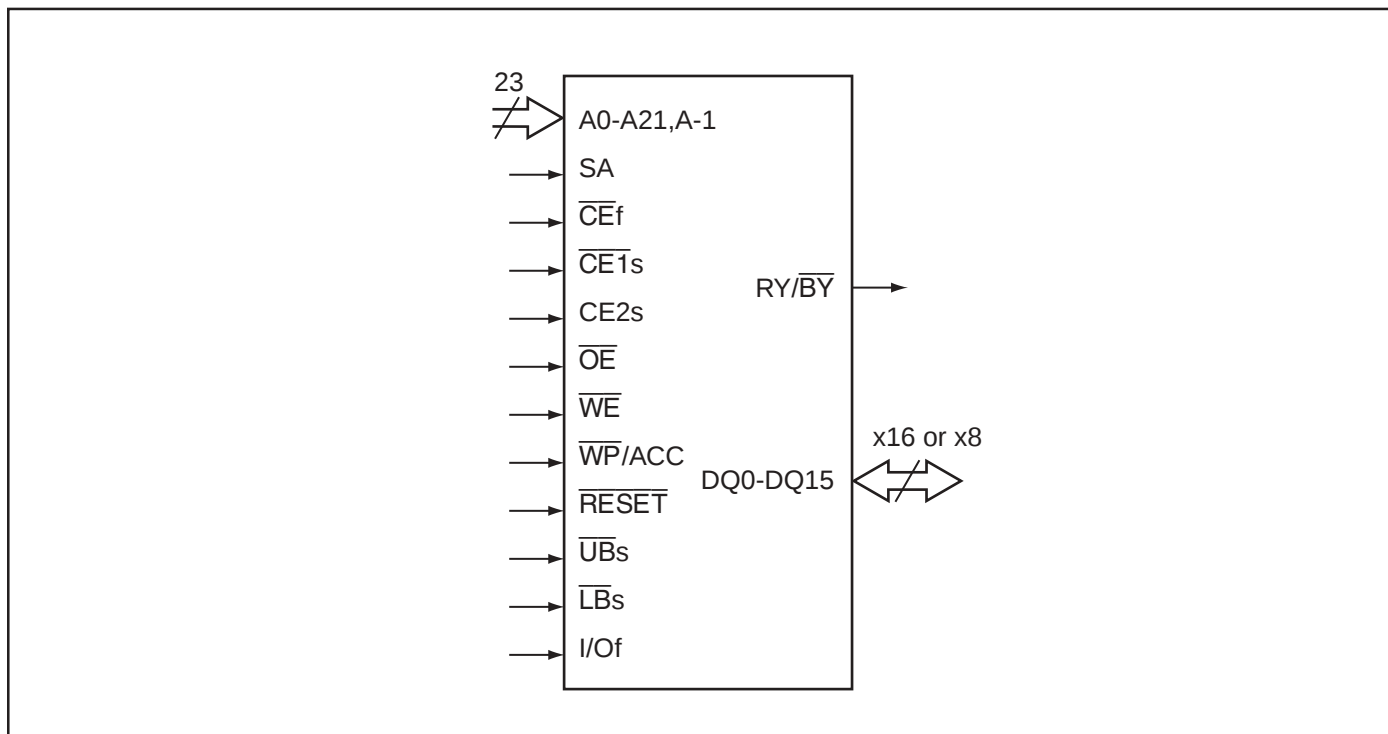
The 64 Mbit flash/8 Mbit SRAM is offered in a 73-ball BGA or 101-ball BGA package. The flash is compatible with the JEDEC Flash command set standard. The flash access time is 70 or 85 ns and the SRAM access time is 70 ns.

The Flash architecture is composed of two virtual banks made of a combination of four physical banks, which allows simultaneous operation on each. Optimized performance can be achieved by first initializing a program or erase function in one bank, then immediately starting a read from the other bank. Both operations would then be operating simultaneously, with zero latency.

## MCP BLOCK DIAGRAM

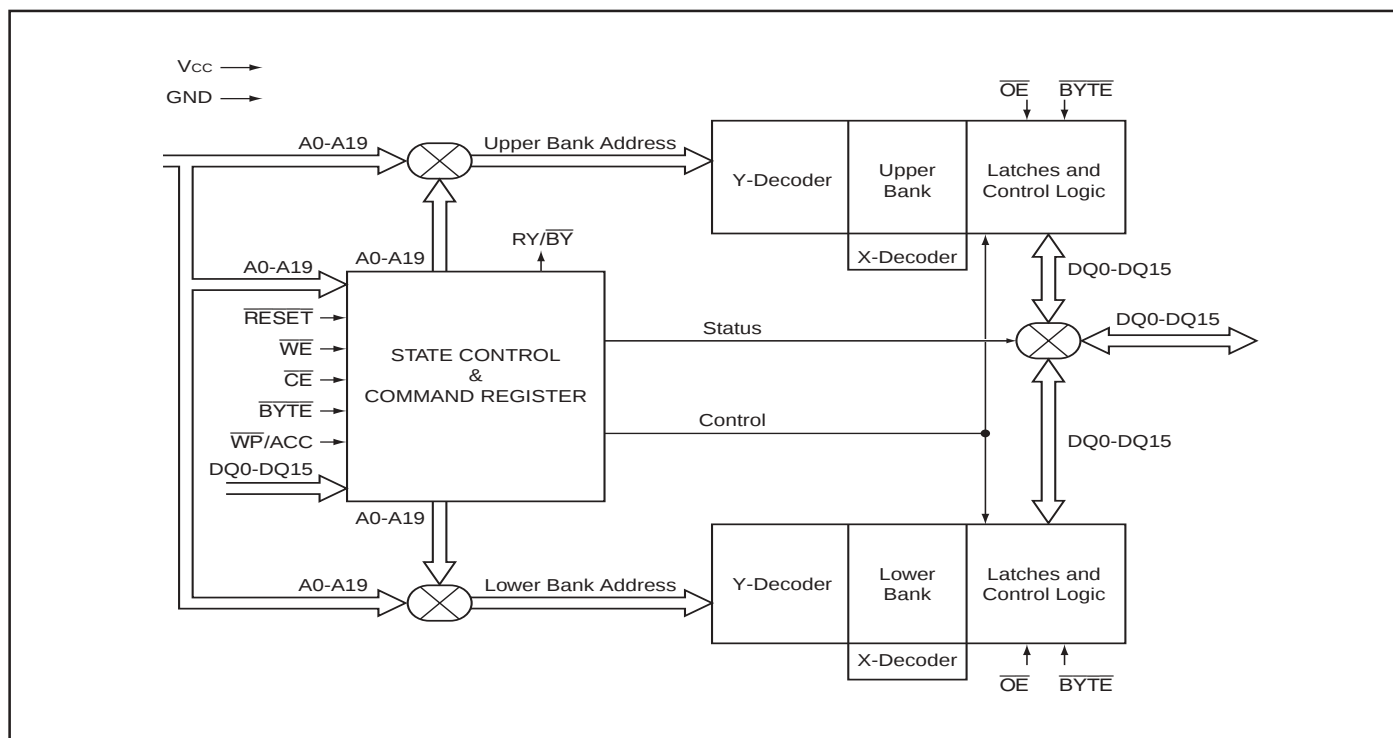


## LOGIC SYMBOL



# IS71V08F64GS08, IS71V16F64GS08

## FLASH MEMORY BLOCK DIAGRAM



## FLASH BANK ORGANIZATION

| Physical Bank | Bank Size | Number of Sectors | Sector Size |
|---------------|-----------|-------------------|-------------|
| 1             | 8Mb       | 8                 | 8KB / 4KW   |
|               |           | 15                | 64KB / 32KW |
| 2             | 24Mb      | 48                | 64KB / 32KW |
| 3             | 24Mb      | 48                | 64KB / 32KW |
| 4             | 8Mb       | 15                | 64KB / 32KW |
|               |           | 8                 | 8KB / 4KW   |

### Note:

Groups of banks can be configured into two virtual banks.

**PIN CONFIGURATION (64 Mb Flash and 8 Mb SRAM)**

73 BALL FBGA (Top View)

|   | 1  | 2                        | 3                      | 4                      | 5                          | 6                      | 7    | 8        | 9    | 10 |
|---|----|--------------------------|------------------------|------------------------|----------------------------|------------------------|------|----------|------|----|
| A | NC |                          |                        |                        |                            |                        |      |          |      | NC |
| B | NC |                          |                        |                        | NC                         | NC                     |      |          |      | NC |
| C | NC |                          | A7                     | $\overline{\text{LB}}$ | $\overline{\text{WP/ACC}}$ | $\overline{\text{WE}}$ | A8   | A11      |      |    |
| D |    | A3                       | A6                     | $\overline{\text{UB}}$ | $\overline{\text{RESET}}$  | CE2s                   | A19  | A12      | A15  |    |
| E |    | A2                       | A5                     | A18                    | RY/BY                      | A20                    | A9   | A13      | A21  |    |
| F | NC | A1                       | A4                     | A17                    |                            |                        | A10  | A14      | NC   | NC |
| G | NC | A0                       | GND                    | DQ1                    |                            |                        | DQ6  | SA       | A16  | NC |
| H |    | $\overline{\text{CEf}}$  | $\overline{\text{OE}}$ | DQ9                    | DQ3                        | DQ4                    | DQ13 | DQ15/A-1 | I/Of |    |
| J |    | $\overline{\text{CE1s}}$ | DQ0                    | DQ10                   | Vccf                       | Vccs                   | DQ12 | DQ7      | GND  |    |
| K |    |                          | DQ8                    | DQ2                    | DQ11                       | NC                     | DQ5  | DQ14     |      |    |
| L | NC |                          |                        |                        | NC                         | NC                     |      |          |      | NC |
| M | NC |                          |                        |                        |                            |                        |      |          |      | NC |

- ☐ Shared  
☒ Flash only  
☒ SRAM only

**PIN DESCRIPTIONS**

|                                 |                          |
|---------------------------------|--------------------------|
| A0-A18                          | Address Inputs, Common   |
| A19-A21, A-1                    | Address Inputs, Flash    |
| DQ0-DQ15/A-1                    | Data Inputs/Outputs      |
| $\overline{\text{RESET}}$       | Reset                    |
| $\overline{\text{CE1s}}$ , CE2s | Chip Selects, SRAM       |
| I/Of                            | I/O Configuration, Flash |
| $\overline{\text{CEf}}$         | Chip Enable Input, Flash |
| $\overline{\text{OE}}$          | Output Enable Input      |
| $\overline{\text{WE}}$          | Write Enable Input       |

|                            |                                       |
|----------------------------|---------------------------------------|
| $\overline{\text{LBs}}$    | Lower-byte Control (DQ0-DQ7), SRAM    |
| $\overline{\text{UBs}}$    | Upper-byte Control (DQ8-DQ15), SRAM   |
| $\overline{\text{WP/ACC}}$ | Write Protect/Acceleration Pin, Flash |
| RY/BY                      | Ready/Busy Output                     |
| SA                         | High Order Address Pin, SRAM (x8)     |
| NC                         | No Connection                         |
| Vccf                       | Power, Flash                          |
| Vccs                       | Power, SRAM                           |
| GND                        | Ground                                |

**PIN CONFIGURATION (64 Mb Flash and 8 Mb SRAM)**

101 BALL FBGA (Top View)

|   | 1  | 2  | 3                        | 4                      | 5                       | 6                          | 7                      | 8    | 9        | 10   | 11 | 12 |
|---|----|----|--------------------------|------------------------|-------------------------|----------------------------|------------------------|------|----------|------|----|----|
| A | NC | NC | NC                       |                        |                         |                            |                        |      |          | NC   | NC | NC |
| B | NC | NC | NC                       |                        |                         |                            |                        |      |          | NC   | NC | NC |
| C | NC | NC | NC                       |                        |                         | NC                         | NC                     |      |          | NC   | NC | NC |
| D |    | NC |                          | A7                     | $\overline{\text{LBs}}$ | $\overline{\text{WP/ACC}}$ | $\overline{\text{WE}}$ | A8   | A11      |      |    |    |
| E |    |    | A3                       | A6                     | $\overline{\text{UBs}}$ | RESET                      | CE2s                   | A19  | A12      | A15  |    |    |
| F |    |    | A2                       | A5                     | A18                     | RY/ $\overline{\text{BY}}$ | A20                    | A9   | A13      | A21  |    |    |
| G |    | NC | A1                       | A4                     | A17                     |                            |                        | A10  | A14      | NC   | NC |    |
| H |    | NC | A0                       | GND                    | DQ1                     |                            |                        | DQ6  | SA       | A16  | NC |    |
| J |    |    | $\overline{\text{CEf}}$  | $\overline{\text{OE}}$ | DQ9                     | DQ3                        | DQ4                    | DQ13 | DQ15/A-1 | I/Of |    |    |
| K |    |    | $\overline{\text{CE1s}}$ | DQ0                    | DQ10                    | Vccf                       | Vccs                   | DQ12 | DQ7      | GND  |    |    |
| L |    |    |                          | DQ8                    | DQ2                     | DQ11                       | NC                     | DQ5  | DQ14     |      |    |    |
| M | NC | NC | NC                       |                        |                         | NC                         | NC                     |      |          | NC   | NC | NC |
| N | NC | NC | NC                       |                        |                         |                            |                        |      |          | NC   | NC | NC |
| P | NC | NC | NC                       |                        |                         |                            |                        |      |          | NC   | NC | NC |

- ☐ Shared  
☒ Flash only  
☒ SRAM only

**PIN DESCRIPTIONS**

|                                 |                          |
|---------------------------------|--------------------------|
| A0-A18                          | Address Inputs, Common   |
| A19-A21, A-1                    | Address Inputs, Flash    |
| DQ0-DQ15/A-1                    | Data Inputs/Outputs      |
| RESET                           | Reset                    |
| $\overline{\text{CE1s}}$ , CE2s | Chip Selects, SRAM       |
| I/Of                            | I/O Configuration, Flash |
| $\overline{\text{CEf}}$         | Chip Enable Input, Flash |
| $\overline{\text{OE}}$          | Output Enable Input      |
| $\overline{\text{WE}}$          | Write Enable Input       |

|                            |                                       |
|----------------------------|---------------------------------------|
| $\overline{\text{LBs}}$    | Lower-byte Control (DQ0-DQ7), SRAM    |
| $\overline{\text{UBs}}$    | Upper-byte Control (DQ8-DQ15), SRAM   |
| $\overline{\text{WP/ACC}}$ | Write Protect/Acceleration Pin, Flash |
| RY/ $\overline{\text{BY}}$ | Ready/Busy Output, Flash              |
| SA                         | Address Input Pin, SRAM (x8)          |
| NC                         | No Connection                         |
| Vccf                       | Power, Flash                          |
| Vccs                       | Power, SRAM                           |
| GND                        | Ground                                |

## DEVICE BUS OPERATIONS

User Bus Operations (Flash = WORD mode: I/Of = Vccf, SRAM = x16 version)

| OPERATION <sup>(1,3)</sup>                         | $\overline{CE}f$ | $\overline{CE}1s$ | CE2s | $\overline{OE}$ | $\overline{WE}$ | SA <sup>(6)</sup> | $\overline{LB}s$ | $\overline{UB}s$ | DQ <sub>0</sub> -DQ <sub>7</sub> | DQ <sub>8</sub> -DQ <sub>15</sub> | $\overline{RESET}$ | $\overline{WP}/ACC^{(5)}$ |
|----------------------------------------------------|------------------|-------------------|------|-----------------|-----------------|-------------------|------------------|------------------|----------------------------------|-----------------------------------|--------------------|---------------------------|
| Full Standby                                       | H                | H                 | X    | X               | X               | X                 | X                | X                | High-Z                           | High-Z                            | H                  | X                         |
|                                                    | H                | X                 | L    | X               | X               | X                 | X                | X                | High-Z                           | High-Z                            | H                  | X                         |
| Output Disable                                     | H                | L                 | H    | H               | H               | X                 | X                | X                | High-Z                           | High-Z                            | H                  | X                         |
|                                                    | H                | L                 | H    | X               | X               | X                 | H                | H                | High-Z                           | High-Z                            | H                  | X                         |
|                                                    | L                | H                 | X    | H               | H               | X                 | X                | X                | High-Z                           | High-Z                            | H                  | X                         |
|                                                    | L                | X                 | L    | H               | H               | X                 | X                | X                | High-Z                           | High-Z                            | H                  | X                         |
| Read from Flash <sup>(2)</sup>                     | L                | H                 | X    | L               | H               | X                 | X                | X                | DOUT                             | DOUT                              | H                  | X                         |
|                                                    | L                | X                 | L    | L               | H               | X                 | X                | X                | DOUT                             | DOUT                              | H                  | X                         |
| Write to Flash                                     | L                | H                 | X    | H               | L               | X                 | X                | X                | DIN                              | DIN                               | H                  | X                         |
|                                                    | L                | X                 | L    | H               | L               | X                 | X                | X                | DIN                              | DIN                               | H                  | X                         |
| Read from SRAM                                     | H                | L                 | H    | L               | H               | X                 | L                | L                | DOUT                             | DOUT                              | H                  | X                         |
|                                                    | H                | L                 | H    | L               | H               | X                 | H                | L                | High-Z                           | DOUT                              | H                  | X                         |
|                                                    | H                | L                 | H    | L               | H               | X                 | L                | H                | DOUT                             | High-Z                            | H                  | X                         |
| Write to SRAM                                      | H                | L                 | H    | X               | L               | X                 | L                | L                | DIN                              | DIN                               | H                  | X                         |
|                                                    | H                | L                 | H    | X               | L               | X                 | H                | L                | High-Z                           | DIN                               | H                  | X                         |
|                                                    | H                | L                 | H    | X               | L               | X                 | L                | H                | DIN                              | High-Z                            | H                  | X                         |
| Temporary Sector Group Unprotection <sup>(4)</sup> | X                | X                 | X    | X               | X               | X                 | X                | X                | X                                | X                                 | V <sub>ID(8)</sub> | X                         |
| Flash Hardware                                     | X                | H                 | X    | X               | X               | X                 | X                | X                | High-Z                           | High-Z                            | L                  | X                         |
| Reset                                              | X                | X                 | L    | X               | X               | X                 | X                | X                | High-Z                           | High-Z                            | L                  | X                         |
| Boot Block Sector                                  | X                | X                 | X    | X               | X               | X                 | X                | X                | X                                | X                                 | X                  | L                         |
| Write Protection                                   |                  |                   |      |                 |                 |                   |                  |                  |                                  |                                   |                    |                           |

## Notes:

- Any operations not indicated this column are inhibited.
- $\overline{WE}$  can be VIL if  $\overline{OE}$  is VIL,  $\overline{OE}$  at VIH initiates the write operations.
- Do not apply  $\overline{CE}f = VIL$ ,  $\overline{CE}1s = VIL$  and CE2s = VIH all at once.
- It is also used for the extended sector group protections.
- $\overline{WP}/ACC = VIL$ : protection of boot sectors.  
 $\overline{WP}/ACC = VIH$ : removal of boot sectors protection.  
 $\overline{WP}/ACC = VACC$  (9V): Program time will reduce by 40%.
- SA: Don't care or open.
- L = VIL, H = VIH, X = VIL or VIH.
- See DC CHARACTERISTICS.

## DEVICE BUS OPERATIONS

User Bus Operations (Flash = BYTE mode: I/O = GND, SRAM = x16 version)

| OPERATION <sup>(1,3)</sup>                         | $\overline{CE}_f$ | $\overline{CE}_{1s}$ | CE2s | DQ <sub>15</sub> /A-1 | $\overline{OE}$ | $\overline{WE}$ | SA <sup>(6)</sup> | $\overline{LB}_s$ | $\overline{UB}_s$ | DQ <sub>0</sub> -DQ <sub>7</sub> | DQ <sub>8</sub> -DQ <sub>15</sub> | $\overline{RESET}$ | WPI/ACC <sup>(5)</sup> |
|----------------------------------------------------|-------------------|----------------------|------|-----------------------|-----------------|-----------------|-------------------|-------------------|-------------------|----------------------------------|-----------------------------------|--------------------|------------------------|
| Full Standby                                       | H                 | H                    | X    | X                     | X               | X               | X                 | X                 | X                 | High-Z                           | High-Z                            | H                  | X                      |
|                                                    | H                 | X                    | L    | X                     | X               | X               | X                 | X                 | X                 | High-Z                           | High-Z                            | H                  | X                      |
| Output Disable                                     | H                 | L                    | H    | X                     | H               | H               | X                 | X                 | X                 | High-Z                           | High-Z                            | H                  | X                      |
|                                                    | H                 | L                    | H    | X                     | X               | X               | X                 | H                 | H                 | High-Z                           | High-Z                            | H                  | X                      |
|                                                    | L                 | H                    | X    | A-1                   | H               | H               | X                 | X                 | X                 | High-Z                           | High-Z                            | H                  | X                      |
|                                                    | L                 | X                    | L    | A-1                   | H               | H               | X                 | X                 | X                 | High-Z                           | High-Z                            | H                  | X                      |
| Read from Flash <sup>(2)</sup>                     | L                 | H                    | X    | A-1                   | L               | H               | X                 | X                 | X                 | DOUT                             | DOUT                              | H                  | X                      |
|                                                    | L                 | X                    | L    | A-1                   | L               | H               | X                 | X                 | X                 | DOUT                             | DOUT                              | H                  | X                      |
| Write to Flash                                     | L                 | H                    | X    | A-1                   | H               | L               | X                 | X                 | X                 | DIN                              | DIN                               | H                  | X                      |
|                                                    | L                 | X                    | L    | A-1                   | H               | L               | X                 | X                 | X                 | DIN                              | DIN                               | H                  | X                      |
| Read from SRAM                                     | H                 | L                    | H    | X                     | L               | H               | X                 | L                 | L                 | DOUT                             | DOUT                              | H                  | X                      |
|                                                    | H                 | L                    | H    | X                     | L               | H               | X                 | H                 | L                 | High-Z                           | DOUT                              | H                  | X                      |
|                                                    | H                 | L                    | H    | X                     | L               | H               | X                 | L                 | H                 | DOUT                             | High-Z                            | H                  | X                      |
| Write to SRAM                                      | H                 | L                    | H    | X                     | X               | L               | X                 | L                 | L                 | DIN                              | DIN                               | H                  | X                      |
|                                                    | H                 | L                    | H    | X                     | X               | L               | X                 | H                 | L                 | High-Z                           | DIN                               | H                  | X                      |
|                                                    | H                 | L                    | H    | X                     | X               | L               | X                 | L                 | H                 | DIN                              | High-Z                            | H                  | X                      |
| Temporary Sector Group Unprotection <sup>(4)</sup> | X                 | X                    | X    | X                     | X               | X               | X                 | X                 | X                 | X                                | X                                 | V <sub>ID(8)</sub> | X                      |
| Flash Hardware Reset                               | X                 | H                    | X    | X                     | X               | X               | X                 | X                 | X                 | High-Z                           | High-Z                            | L                  | X                      |
|                                                    | X                 | X                    | L    | X                     | X               | X               | X                 | X                 | X                 | High-Z                           | High-Z                            | L                  | X                      |
| Boot Block Sector Write Protection                 | X                 | X                    | X    | X                     | X               | X               | X                 | X                 | X                 | X                                | X                                 | X                  | L                      |

## Notes:

- Any operations not indicated this column are inhibited..
- $\overline{WE}$  can be VIL if  $\overline{OE}$  is VIL,  $\overline{OE}$  at VIH initiates the write operations.
- Do not apply  $\overline{CE}_f$  = VIL,  $\overline{CE}_{1s}$  = VIL and CE2s = VIH all at once.
- It is also used for the extended sector group protections.
- $\overline{WP}/ACC$  = VIL: protection of boot sectors.  
 $\overline{WP}/ACC$  = VIH: removal of boot sectors protection.  
 $\overline{WP}/ACC$  = VACC (9V): Program time will reduce by 40%.
- SA: Don't care or open.
- L = VIL, H = VIH, X = VIL or VIH.
- See DC CHARACTERISTICS.

## DEVICE BUS OPERATIONS

User Bus Operations (Flash = WORD mode: I/Of = Vccf, SRAM = x8 version)

| OPERATION <sup>(1,3)</sup>                         | $\overline{CE}f$ | $\overline{CE}1s$ | $CE2s$ | $\overline{OE}$ | $\overline{WE}$ | SA | $\overline{LB}s^{(6)}$ | $\overline{UB}s^{(6)}$ | $DQ_0-DQ_7$ | $DQ_8-DQ_{15}$ | $\overline{RESET}$ | $\overline{WP}/ACC^{(5)}$ |
|----------------------------------------------------|------------------|-------------------|--------|-----------------|-----------------|----|------------------------|------------------------|-------------|----------------|--------------------|---------------------------|
| Full Standby                                       | H                | H                 | X      | X               | X               | X  | X                      | X                      | High-Z      | High-Z         | H                  | X                         |
|                                                    | H                | X                 | L      | X               | X               | X  | X                      | X                      | High-Z      | High-Z         | H                  | X                         |
| Output Disable                                     | H                | L                 | H      | H               | H               | X  | X                      | X                      | High-Z      | High-Z         | H                  | X                         |
|                                                    | H                | L                 | H      | X               | X               | X  | H                      | H                      | High-Z      | High-Z         | H                  | X                         |
|                                                    | L                | H                 | X      | H               | H               | X  | X                      | X                      | High-Z      | High-Z         | H                  | X                         |
|                                                    | L                | X                 | L      | H               | H               | X  | X                      | X                      | High-Z      | High-Z         | H                  | X                         |
| Read from Flash <sup>(2)</sup>                     | L                | H                 | X      | L               | H               | X  | X                      | X                      | DOUT        | DOUT           | H                  | X                         |
|                                                    | L                | X                 | L      | L               | H               | X  | X                      | X                      | DOUT        | DOUT           | H                  | X                         |
| Write to Flash                                     | L                | H                 | X      | H               | L               | X  | X                      | X                      | DIN         | DIN            | H                  | X                         |
|                                                    | L                | X                 | L      | H               | L               | X  | X                      | X                      | DIN         | DIN            | H                  | X                         |
| Read from SRAM                                     | H                | L                 | H      | L               | H               | SA | X                      | X                      | DOUT        | High-Z         | H                  | X                         |
| Write to SRAM                                      | H                | L                 | H      | X               | L               | SA | X                      | X                      | DIN         | High-Z         | H                  | X                         |
| Temporary Sector Group Unprotection <sup>(4)</sup> | X                | X                 | X      | X               | X               | X  | X                      | X                      | X           | X              | V <sub>ID(8)</sub> | X                         |
| Flash Hardware Reset                               | X                | H                 | X      | X               | X               | X  | X                      | X                      | High-Z      | High-Z         | L                  | X                         |
|                                                    | X                | X                 | L      | X               | X               | X  | X                      | X                      | High-Z      | High-Z         | L                  | X                         |
| Boot Block Sector Write Protection                 | X                | X                 | X      | X               | X               | X  | X                      | X                      | X           | X              | X                  | L                         |

## Notes:

- Any operations not indicated this column are inhibited..
- $\overline{WE}$  can be VIL if  $\overline{OE}$  is VIL,  $\overline{OE}$  at VIH initiates the write operations.
- Do not apply  $\overline{CE}f = VIL$ ,  $\overline{CE}1s = VIL$  and  $CE2s = VIH$  all at once.
- It is also used for the extended sector group protections.
- $\overline{WP}/ACC = VIL$ : protection of boot sectors.  
 $\overline{WP}/ACC = VIH$ : removal of boot sectors protection.  
 $\overline{WP}/ACC = VACC (9V)$ : Program time will reduce by 40%.
- $\overline{LB}s$ ,  $\overline{UB}s$ : Don't care or open.
- L = VIL, H = VIH, X = VIL or VIH.
- See DC CHARACTERISTICS.

## DEVICE BUS OPERATIONS

User Bus Operations (Flash = BYTE mode: I/Of = GND, SRAM = x8 version)

| OPERATION <sup>(1,3)</sup>                         | $\overline{CE}_f$ | $\overline{CE}_{1s}$ | CE2s | DQ <sub>15</sub> /A-1 | $\overline{OE}$ | $\overline{WE}$ | SA | $\overline{LB}_s^{(6)}$ | $\overline{UB}_s^{(6)}$ | DQ <sub>0</sub> -DQ <sub>7</sub> | DQ <sub>8</sub> -DQ <sub>15</sub> | $\overline{RESET}$ | WP/ACC <sup>(5)</sup> |
|----------------------------------------------------|-------------------|----------------------|------|-----------------------|-----------------|-----------------|----|-------------------------|-------------------------|----------------------------------|-----------------------------------|--------------------|-----------------------|
| Full Standby                                       | H                 | H                    | X    | X                     | X               | X               | X  | X                       | X                       | High-Z                           | High-Z                            | H                  | X                     |
|                                                    | H                 | X                    | L    | X                     | X               | X               | X  | X                       | X                       | High-Z                           | High-Z                            | H                  | X                     |
| Output Disable                                     | H                 | L                    | H    | X                     | H               | H               | X  | X                       | X                       | High-Z                           | High-Z                            | H                  | X                     |
|                                                    | H                 | L                    | H    | X                     | X               | X               | X  | H                       | H                       | High-Z                           | High-Z                            | H                  | X                     |
|                                                    | L                 | H                    | X    | A-1                   | H               | H               | X  | X                       | X                       | High-Z                           | High-Z                            | H                  | X                     |
|                                                    | L                 | X                    | L    | A-1                   | H               | H               | X  | X                       | X                       | High-Z                           | High-Z                            | H                  | X                     |
| Read from Flash <sup>(2)</sup>                     | L                 | H                    | X    | A-1                   | L               | H               | X  | X                       | X                       | DOUT                             | DOUT                              | H                  | X                     |
|                                                    | L                 | X                    | L    | A-1                   | L               | H               | X  | X                       | X                       | DOUT                             | DOUT                              | H                  | X                     |
| Write to Flash                                     | L                 | H                    | X    | A-1                   | H               | L               | X  | X                       | X                       | DIN                              | DIN                               | H                  | X                     |
|                                                    | L                 | X                    | L    | A-1                   | H               | L               | X  | X                       | X                       | DIN                              | DIN                               | H                  | X                     |
| Read from SRAM                                     | H                 | L                    | H    | X                     | L               | H               | SA | X                       | X                       | DOUT                             | High-Z                            | H                  | X                     |
| Write to SRAM                                      | H                 | L                    | H    | X                     | X               | L               | SA | X                       | X                       | DIN                              | High-Z                            | H                  | X                     |
| Temporary Sector Group Unprotection <sup>(4)</sup> | X                 | X                    | X    | X                     | X               | X               | X  | X                       | X                       | X                                | X                                 | V <sub>ID(8)</sub> | X                     |
| Flash Hardware Reset                               | X                 | H                    | X    | X                     | X               | X               | X  | X                       | X                       | High-Z                           | High-Z                            | L                  | X                     |
| Boot Block Sector Write Protection                 | X                 | X                    | L    | X                     | X               | X               | X  | X                       | X                       | High-Z                           | High-Z                            | L                  | X                     |
| Boot Block Sector                                  | X                 | X                    | X    | X                     | X               | X               | X  | X                       | X                       | X                                | X                                 | X                  | L                     |

## Notes:

- Any operations not indicated this column are inhibited.
- $\overline{WE}$  can be VIL if  $\overline{OE}$  is VIL,  $\overline{OE}$  at VIH initiates the write operations.
- Do not apply  $\overline{CE}_f = \text{VIL}$ ,  $\overline{CE}_{1s} = \text{VIL}$  and CE2s = VIH all at once.
- It is also used for the extended sector group protections.
- $\overline{WP}/\text{ACC} = \text{VIL}$ : protection of boot sectors.  
 $\overline{WP}/\text{ACC} = \text{VIH}$ : removal of boot sectors protection.  
 $\overline{WP}/\text{ACC} = \text{VACC (9V)}$ : Program time will reduce by 40%.
- $\overline{LB}_s$ ,  $\overline{UB}_s$ : Don't care or open.
- L = VIL, H = VIH, X = VIL or VIH.
- See DC CHARACTERISTICS.

## FLASH - SECTOR ADDRESS

| Bank   | Sector | Sector Address<br>A21-A12 | Sector Size<br>KB/KW | (x8)<br>Address Range | (x16)<br>Address Range |
|--------|--------|---------------------------|----------------------|-----------------------|------------------------|
| Bank 1 | SA0    | 0000000000                | 8/4                  | 000000h–001FFFh       | 00000h–00FFFh          |
| Bank 1 | SA1    | 0000000001                | 8/4                  | 002000h–003FFFh       | 01000h–01FFFh          |
| Bank 1 | SA2    | 0000000010                | 8/4                  | 004000h–005FFFh       | 02000h–02FFFh          |
| Bank 1 | SA3    | 0000000011                | 8/4                  | 006000h–007FFFh       | 03000h–03FFFh          |
| Bank 1 | SA4    | 0000000100                | 8/4                  | 008000h–009FFFh       | 04000h–04FFFh          |
| Bank 1 | SA5    | 0000000101                | 8/4                  | 00A000h–00BFFFh       | 05000h–05FFFh          |
| Bank 1 | SA6    | 0000000110                | 8/4                  | 00C000h–00DFFFh       | 06000h–06FFFh          |
| Bank 1 | SA7    | 0000000111                | 8/4                  | 00E000h–00FFFFh       | 07000h–07FFFh          |
| Bank 1 | SA8    | 0000001xxx                | 64/32                | 010000h–01FFFFh       | 08000h–0FFFFh          |
| Bank 1 | SA9    | 0000010xxx                | 64/32                | 020000h–02FFFFh       | 10000h–17FFFh          |
| Bank 1 | SA10   | 0000011xxx                | 64/32                | 030000h–03FFFFh       | 18000h–1FFFFh          |
| Bank 1 | SA11   | 0000100xxx                | 64/32                | 040000h–04FFFFh       | 20000h–27FFFh          |
| Bank 1 | SA12   | 0000101xxx                | 64/32                | 050000h–05FFFFh       | 28000h–2FFFFh          |
| Bank 1 | SA13   | 0000110xxx                | 64/32                | 060000h–06FFFFh       | 30000h–37FFFh          |
| Bank 1 | SA14   | 0000111xxx                | 64/32                | 070000h–07FFFFh       | 38000h–3FFFFh          |
| Bank 1 | SA15   | 0001000xxx                | 64/32                | 080000h–08FFFFh       | 40000h–47FFFh          |
| Bank 1 | SA16   | 0001001xxx                | 64/32                | 090000h–09FFFFh       | 48000h–4FFFFh          |
| Bank 1 | SA17   | 0001010xxx                | 64/32                | 0A0000h–0AFFFFh       | 50000h–57FFFh          |
| Bank 1 | SA18   | 0001011xxx                | 64/32                | 0B0000h–0BFFFFh       | 58000h–5FFFFh          |
| Bank 1 | SA19   | 0001100xxx                | 64/32                | 0C0000h–0CFFFFh       | 60000h–67FFFh          |
| Bank 1 | SA20   | 0001101xxx                | 64/32                | 0D0000h–0DFFFFh       | 68000h–6FFFFh          |
| Bank 1 | SA21   | 0001110xxx                | 64/32                | 0E0000h–0EFFFFh       | 70000h–77FFFh          |
| Bank 1 | SA22   | 0001111xxx                | 64/32                | 0F0000h–0FFFFFh       | 78000h–7FFFFh          |
| Bank 2 | SA23   | 0010000xxx                | 64/32                | 100000h–00FFFFh       | 80000h–87FFFh          |
| Bank 2 | SA24   | 0010001xxx                | 64/32                | 110000h–11FFFFh       | 88000h–8FFFFh          |
| Bank 2 | SA25   | 0010010xxx                | 64/32                | 120000h–12FFFFh       | 90000h–97FFFh          |
| Bank 2 | SA26   | 0010011xxx                | 64/32                | 130000h–13FFFFh       | 98000h–9FFFFh          |
| Bank 2 | SA27   | 0010100xxx                | 64/32                | 140000h–14FFFFh       | A0000h–A7FFFh          |
| Bank 2 | SA28   | 0010101xxx                | 64/32                | 150000h–15FFFFh       | A8000h–AFFFFh          |
| Bank 2 | SA29   | 0010110xxx                | 64/32                | 160000h–16FFFFh       | B0000h–B7FFFh          |
| Bank 2 | SA30   | 0010111xxx                | 64/32                | 170000h–17FFFFh       | B8000h–BFFFFh          |
| Bank 2 | SA31   | 0011000xxx                | 64/32                | 180000h–18FFFFh       | C0000h–C7FFFh          |
| Bank 2 | SA32   | 0011001xxx                | 64/32                | 190000h–19FFFFh       | C8000h–CFFFFh          |
| Bank 2 | SA33   | 0011010xxx                | 64/32                | 1A0000h–1AFFFFh       | D0000h–D7FFFh          |
| Bank 2 | SA34   | 0011011xxx                | 64/32                | 1B0000h–1BFFFFh       | D8000h–DFFFFh          |
| Bank 2 | SA35   | 0011100xxx                | 64/32                | 1C0000h–1CFFFFh       | E0000h–E7FFFh          |

## FLASH - SECTOR ADDRESS Continued:

| Bank   | Sector | Sector Address<br>A21-A12 | Sector Size<br>KB/KW | (x8)<br>Address Range | (x16)<br>Address Range |
|--------|--------|---------------------------|----------------------|-----------------------|------------------------|
| Bank 2 | SA36   | 0011101xxx                | 64/32                | 1D0000h–1DFFFFh       | E8000h–EFFFFh          |
| Bank 2 | SA37   | 0011110xxx                | 64/32                | 1E0000h–1EFFFFh       | F0000h–F7FFFh          |
| Bank 2 | SA38   | 0011111xxx                | 64/32                | 1F0000h–1FFFFFFh      | F8000h–FFFFFFh         |
| Bank 2 | SA39   | 0100000xxx                | 64/32                | 200000h–20FFFFh       | F9000h–107FFFh         |
| Bank 2 | SA40   | 0100001xxx                | 64/32                | 210000h–21FFFFh       | 108000h–10FFFFh        |
| Bank 2 | SA41   | 0100010xxx                | 64/32                | 220000h–22FFFFh       | 110000h–117FFFh        |
| Bank 2 | SA42   | 0100011xxx                | 64/32                | 230000h–23FFFFh       | 118000h–11FFFFh        |
| Bank 2 | SA43   | 0100100xxx                | 64/32                | 240000h–24FFFFh       | 120000h–127FFFh        |
| Bank 2 | SA44   | 0100101xxx                | 64/32                | 250000h–25FFFFh       | 128000h–12FFFFh        |
| Bank 2 | SA45   | 0100110xxx                | 64/32                | 260000h–26FFFFh       | 130000h–137FFFh        |
| Bank 2 | SA46   | 0100111xxx                | 64/32                | 270000h–27FFFFh       | 138000h–13FFFFh        |
| Bank 2 | SA47   | 0101000xxx                | 64/32                | 280000h–28FFFFh       | 140000h–147FFFh        |
| Bank 2 | SA48   | 0101001xxx                | 64/32                | 290000h–29FFFFh       | 148000h–14FFFFh        |
| Bank 2 | SA49   | 0101010xxx                | 64/32                | 2A0000h–2AFFFFh       | 150000h–157FFFh        |
| Bank 2 | SA50   | 0101011xxx                | 64/32                | 2B0000h–2BFFFFh       | 158000h–15FFFFh        |
| Bank 2 | SA51   | 0101100xxx                | 64/32                | 2C0000h–2CFFFFh       | 160000h–167FFFh        |
| Bank 2 | SA52   | 0101101xxx                | 64/32                | 2D0000h–2DFFFFh       | 168000h–16FFFFh        |
| Bank 2 | SA53   | 0101110xxx                | 64/32                | 2E0000h–2EFFFFh       | 170000h–177FFFh        |
| Bank 2 | SA54   | 0101111xxx                | 64/32                | 2F0000h–2FFFFFFh      | 178000h–17FFFFh        |
| Bank 2 | SA55   | 0110000xxx                | 64/32                | 300000h–30FFFFh       | 180000h–187FFFh        |
| Bank 2 | SA56   | 0110001xxx                | 64/32                | 310000h–31FFFFh       | 188000h–18FFFFh        |
| Bank 2 | SA57   | 0110010xxx                | 64/32                | 320000h–32FFFFh       | 190000h–197FFFh        |
| Bank 2 | SA58   | 0110011xxx                | 64/32                | 330000h–33FFFFh       | 198000h–19FFFFh        |
| Bank 2 | SA59   | 0110100xxx                | 64/32                | 340000h–34FFFFh       | 1A0000h–1A7FFFh        |
| Bank 2 | SA60   | 0110101xxx                | 64/32                | 350000h–35FFFFh       | 1A8000h–1AFFFFh        |
| Bank 2 | SA61   | 0110110xxx                | 64/32                | 360000h–36FFFFh       | 1B0000h–1B7FFFh        |
| Bank 2 | SA62   | 0110111xxx                | 64/32                | 370000h–37FFFFh       | 1B8000h–1BFFFFh        |
| Bank 2 | SA63   | 0111000xxx                | 64/32                | 380000h–38FFFFh       | 1C0000h–1C7FFFh        |
| Bank 2 | SA64   | 0111001xxx                | 64/32                | 390000h–39FFFFh       | 1C8000h–1CFFFFh        |
| Bank 2 | SA65   | 0111010xxx                | 64/32                | 3A0000h–3AFFFFh       | 1D0000h–1D7FFFh        |
| Bank 2 | SA66   | 0111011xxx                | 64/32                | 3B0000h–3BFFFFh       | 1D8000h–1DFFFFh        |
| Bank 2 | SA67   | 0111100xxx                | 64/32                | 3C0000h–3CFFFFh       | 1E0000h–1E7FFFh        |
| Bank 2 | SA68   | 0111101xxx                | 64/32                | 3D0000h–3DFFFFh       | 1E8000h–1EFFFFh        |
| Bank 2 | SA69   | 0111110xxx                | 64/32                | 3E0000h–3EFFFFh       | 1F0000h–1F7FFFh        |
| Bank 2 | SA70   | 0111111xxx                | 64/32                | 3F0000h–3FFFFFFh      | 1F8000h–1FFFFFFh       |

## FLASH - SECTOR ADDRESS Continued:

| Bank   | Sector | Sector Address<br>A21-A12 | Sector Size<br>KB/KW | (x8)<br>Address Range | (x16)<br>Address Range |
|--------|--------|---------------------------|----------------------|-----------------------|------------------------|
| Bank 3 | SA71   | 1000000xxx                | 64/32                | 400000h–40FFFFh       | 200000h–207FFFh        |
| Bank 3 | SA72   | 1000001xxx                | 64/32                | 410000h–41FFFFh       | 208000h–20FFFFh        |
| Bank 3 | SA73   | 1000010xxx                | 64/32                | 420000h–42FFFFh       | 210000h–217FFFh        |
| Bank 3 | SA74   | 1000011xxx                | 64/32                | 430000h–43FFFFh       | 218000h–21FFFFh        |
| Bank 3 | SA75   | 1000100xxx                | 64/32                | 440000h–44FFFFh       | 220000h–227FFFh        |
| Bank 3 | SA76   | 1000101xxx                | 64/32                | 450000h–45FFFFh       | 228000h–22FFFFh        |
| Bank 3 | SA77   | 1000110xxx                | 64/32                | 460000h–46FFFFh       | 230000h–237FFFh        |
| Bank 3 | SA78   | 1000111xxx                | 64/32                | 470000h–47FFFFh       | 238000h–23FFFFh        |
| Bank 3 | SA79   | 1001000xxx                | 64/32                | 480000h–48FFFFh       | 240000h–247FFFh        |
| Bank 3 | SA80   | 1001001xxx                | 64/32                | 490000h–49FFFFh       | 248000h–24FFFFh        |
| Bank 3 | SA81   | 1001010xxx                | 64/32                | 4A0000h–4AFFFFh       | 250000h–257FFFh        |
| Bank 3 | SA82   | 1001011xxx                | 64/32                | 4B0000h–4BFFFFh       | 258000h–25FFFFh        |
| Bank 3 | SA83   | 1001100xxx                | 64/32                | 4C0000h–4CFFFFh       | 260000h–267FFFh        |
| Bank 3 | SA84   | 1001101xxx                | 64/32                | 4D0000h–4DFFFFh       | 268000h–26FFFFh        |
| Bank 3 | SA85   | 1001110xxx                | 64/32                | 4E0000h–4EFFFFh       | 270000h–277FFFh        |
| Bank 3 | SA86   | 1001111xxx                | 64/32                | 4F0000h–4FFFFFh       | 278000h–27FFFFh        |
| Bank 3 | SA87   | 1010000xxx                | 64/32                | 500000h–50FFFFh       | 280000h–28FFFFh        |
| Bank 3 | SA88   | 1010001xxx                | 64/32                | 510000h–51FFFFh       | 288000h–28FFFFh        |
| Bank 3 | SA89   | 1010010xxx                | 64/32                | 520000h–52FFFFh       | 290000h–297FFFh        |
| Bank 3 | SA90   | 1010011xxx                | 64/32                | 530000h–53FFFFh       | 298000h–29FFFFh        |
| Bank 3 | SA91   | 1010100xxx                | 64/32                | 540000h–54FFFFh       | 2A0000h–2A7FFFh        |
| Bank 3 | SA92   | 1010101xxx                | 64/32                | 550000h–55FFFFh       | 2A8000h–2AFFFFh        |
| Bank 3 | SA93   | 1010110xxx                | 64/32                | 560000h–56FFFFh       | 2B0000h–2B7FFFh        |
| Bank 3 | SA94   | 1010111xxx                | 64/32                | 570000h–57FFFFh       | 2B8000h–2BFFFFh        |
| Bank 3 | SA95   | 1011000xxx                | 64/32                | 580000h–58FFFFh       | 2C0000h–2C7FFFh        |
| Bank 3 | SA96   | 1011001xxx                | 64/32                | 590000h–59FFFFh       | 2C8000h–2CFFFFh        |
| Bank 3 | SA97   | 1011010xxx                | 64/32                | 5A0000h–5AFFFFh       | 2D0000h–2D7FFFh        |
| Bank 3 | SA98   | 1011011xxx                | 64/32                | 5B0000h–5BFFFFh       | 2D8000h–2DFFFFh        |
| Bank 3 | SA99   | 1011100xxx                | 64/32                | 5C0000h–5CFFFFh       | 2E0000h–2E7FFFh        |
| Bank 3 | SA100  | 1011101xxx                | 64/32                | 5D0000h–5DFFFFh       | 2E8000h–2EFFFFh        |
| Bank 3 | SA101  | 1011110xxx                | 64/32                | 5E0000h–5EFFFFh       | 2F0000h–2FFFFFh        |
| Bank 3 | SA102  | 1011111xxx                | 64/32                | 5F0000h–5FFFFFh       | 2F8000h–2FFFFFh        |
| Bank 3 | SA103  | 1100000xxx                | 64/32                | 600000h–60FFFFh       | 300000h–307FFFh        |
| Bank 3 | SA104  | 1100001xxx                | 64/32                | 610000h–61FFFFh       | 308000h–30FFFFh        |
| Bank 3 | SA105  | 1100010xxx                | 64/32                | 620000h–62FFFFh       | 310000h–317FFFh        |

## FLASH - SECTOR ADDRESS Continued:

| Bank   | Sector | Sector Address<br>A21-A12 | Sector Size<br>KB/KW | (x8)<br>Address Range | (x16)<br>Address Range |
|--------|--------|---------------------------|----------------------|-----------------------|------------------------|
| Bank 3 | SA106  | 1100011xxx                | 64/32                | 630000h–63FFFFh       | 318000h–31FFFFh        |
| Bank 3 | SA107  | 1100100xxx                | 64/32                | 640000h–64FFFFh       | 320000h–32FFFFh        |
| Bank 3 | SA108  | 1100101xxx                | 64/32                | 650000h–65FFFFh       | 328000h–32FFFFh        |
| Bank 3 | SA109  | 1100110xxx                | 64/32                | 660000h–66FFFFh       | 330000h–33FFFFh        |
| Bank 3 | SA110  | 1100111xxx                | 64/32                | 670000h–67FFFFh       | 338000h–33FFFFh        |
| Bank 3 | SA111  | 1101000xxx                | 64/32                | 680000h–68FFFFh       | 340000h–34FFFFh        |
| Bank 3 | SA112  | 1101001xxx                | 64/32                | 690000h–69FFFFh       | 348000h–34FFFFh        |
| Bank 3 | SA113  | 1101010xxx                | 64/32                | 6A0000h–6AFFFFh       | 350000h–35FFFFh        |
| Bank 3 | SA114  | 1101011xxx                | 64/32                | 6B0000h–6BFFFFh       | 358000h–35FFFFh        |
| Bank 3 | SA115  | 1101100xxx                | 64/32                | 6C0000h–6CFFFFh       | 360000h–36FFFFh        |
| Bank 3 | SA116  | 1101101xxx                | 64/32                | 6D0000h–6DFFFFh       | 368000h–36FFFFh        |
| Bank 3 | SA117  | 1101110xxx                | 64/32                | 6E0000h–6EFFFFh       | 370000h–37FFFFh        |
| Bank 3 | SA118  | 1101111xxx                | 64/32                | 6F0000h–6FFFFFh       | 378000h–37FFFFh        |
| Bank 4 | SA119  | 1110000xxx                | 64/32                | 700000h–70FFFFh       | 380000h–38FFFFh        |
| Bank 4 | SA120  | 1110001xxx                | 64/32                | 710000h–71FFFFh       | 388000h–38FFFFh        |
| Bank 4 | SA121  | 1110010xxx                | 64/32                | 720000h–72FFFFh       | 390000h–39FFFFh        |
| Bank 4 | SA122  | 1110011xxx                | 64/32                | 730000h–73FFFFh       | 398000h–39FFFFh        |
| Bank 4 | SA123  | 1110100xxx                | 64/32                | 740000h–74FFFFh       | 3A0000h–3A7FFFh        |
| Bank 4 | SA124  | 1110101xxx                | 64/32                | 750000h–75FFFFh       | 3A8000h–3AFFFFh        |
| Bank 4 | SA125  | 1110110xxx                | 64/32                | 760000h–76FFFFh       | 3B0000h–3B7FFFh        |
| Bank 4 | SA126  | 1110111xxx                | 64/32                | 770000h–77FFFFh       | 3B8000h–3BFFFFh        |
| Bank 4 | SA127  | 1111000xxx                | 64/32                | 780000h–78FFFFh       | 3C0000h–3C7FFFh        |
| Bank 4 | SA128  | 1111001xxx                | 64/32                | 790000h–79FFFFh       | 3C8000h–3CFFFFh        |
| Bank 4 | SA129  | 1111010xxx                | 64/32                | 7A0000h–7AFFFFh       | 3D0000h–3D7FFFh        |
| Bank 4 | SA130  | 1111011xxx                | 64/32                | 7B0000h–7BFFFFh       | 3D8000h–3DFFFFh        |
| Bank 4 | SA131  | 1111100xxx                | 64/32                | 7C0000h–7CFFFFh       | 3E0000h–3E7FFFh        |
| Bank 4 | SA132  | 1111101xxx                | 64/32                | 7D0000h–7DFFFFh       | 3E8000h–3EFFFFh        |
| Bank 4 | SA133  | 1111110xxx                | 64/32                | 7E0000h–7EFFFFh       | 3F0000h–3F7FFFh        |
| Bank 4 | SA134  | 1111111000                | 8/4                  | 7F0000h–7F1FFFh       | 3F8000h–3F8FFFh        |
| Bank 4 | SA135  | 1111111001                | 8/4                  | 7F2000h–7F3FFFh       | 3F9000h–3F9FFFh        |
| Bank 4 | SA136  | 1111111010                | 8/4                  | 7F4000h–7F5FFFh       | 3FA000h–3FAFFFh        |
| Bank 4 | SA137  | 1111111011                | 8/4                  | 7F6000h–7F7FFFh       | 3FB000h–3FBFFFh        |
| Bank 4 | SA138  | 1111111100                | 8/4                  | 7F8000h–7F9FFFh       | 3FC000h–3FCFFFh        |
| Bank 4 | SA139  | 1111111101                | 8/4                  | 7FA000h–7FBFFFh       | 3FD000h–3FDFFFh        |
| Bank 4 | SA140  | 1111111110                | 8/4                  | 7FC000h–7FDFFFh       | 3FE000h–3FEFFFh        |
| Bank 4 | SA141  | 1111111111                | 8/4                  | 7FE000h–7FFFFFFh      | 3FF000h–3FFFFFFh       |

**Note:** The address range is A21:A-1 in byte mode (I/O=VIL) or A21:A0 in word mode (I/O=VIH). The bank address bits are A21 - A19.

## FLASH - SECURITY SECTOR ADDRESSES

(Hidden-ROM)

| Sector<br>Address<br>A21-A12 | Size<br>Byte / Word | (x8)<br>Address Range | (x16)<br>Address Range |
|------------------------------|---------------------|-----------------------|------------------------|
| 0000000xxx                   | 256/128             | 00000h-0000FFh        | 00000h-0007Fh          |

## SECTOR GROUP ADDRESS

| Sector<br>Group | A21 | A20 | A19 | A18 | A17 | A16    | A15    | A14 | A13 | A12 | Sectors      |
|-----------------|-----|-----|-----|-----|-----|--------|--------|-----|-----|-----|--------------|
| SGA0            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 0   | 0   | 0   | SA0          |
| SGA1            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 0   | 0   | 1   | SA1          |
| SGA2            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 0   | 1   | 0   | SA2          |
| SGA3            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 0   | 1   | 1   | SA3          |
| SGA4            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 1   | 0   | 0   | SA4          |
| SGA5            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 1   | 0   | 1   | SA5          |
| SGA6            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 1   | 1   | 0   | SA6          |
| SGA7            | 0   | 0   | 0   | 0   | 0   | 0      | 0      | 1   | 1   | 1   | SA7          |
| SGA8            | 0   | 0   | 0   | 0   | 0   | 0<br>1 | 1<br>1 | X   | X   | X   | SA8 to SA10  |
| SGA9            | 0   | 0   | 0   | 0   | 1   | X      | X      | X   | X   | X   | SA11 to SA14 |
| SGA10           | 0   | 0   | 0   | 1   | 0   | X      | X      | X   | X   | X   | SA15 to SA18 |
| SGA11           | 0   | 0   | 0   | 1   | 1   | X      | X      | X   | X   | X   | SA19 to SA22 |
| SGA12           | 0   | 0   | 1   | 0   | 0   | X      | X      | X   | X   | X   | SA23 to SA26 |
| SGA13           | 0   | 0   | 1   | 0   | 1   | X      | X      | X   | X   | X   | SA27 to SA30 |
| SGA14           | 0   | 0   | 1   | 1   | 0   | X      | X      | X   | X   | X   | SA31 to SA34 |
| SGA15           | 0   | 0   | 1   | 1   | 1   | X      | X      | X   | X   | X   | SA35 to SA38 |
| SGA16           | 0   | 1   | 0   | 0   | 0   | X      | X      | X   | X   | X   | SA39 to SA42 |
| SGA17           | 0   | 1   | 0   | 0   | 1   | X      | X      | X   | X   | X   | SA43 to SA46 |
| SGA18           | 0   | 1   | 0   | 1   | 0   | X      | X      | X   | X   | X   | SA47 to SA50 |
| SGA19           | 0   | 1   | 0   | 1   | 1   | X      | X      | X   | X   | X   | SA51 to SA54 |
| SGA20           | 0   | 1   | 1   | 0   | 0   | X      | X      | X   | X   | X   | SA55 to SA58 |
| SGA21           | 0   | 1   | 1   | 0   | 1   | X      | X      | X   | X   | X   | SA59 to SA62 |
| SGA22           | 0   | 1   | 1   | 1   | 0   | X      | X      | X   | X   | X   | SA63 to SA66 |
| SGA23           | 0   | 1   | 1   | 1   | 1   | X      | X      | X   | X   | X   | SA67 to SA70 |
| SGA24           | 1   | 0   | 0   | 0   | 0   | X      | X      | X   | X   | X   | SA71 to SA74 |
| SGA25           | 1   | 0   | 0   | 0   | 1   | X      | X      | X   | X   | X   | SA75 to SA78 |

## SECTOR GROUP ADDRESS Continued:

| Sector Group | A21 | A20 | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | Sectors        |
|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------|
| SGA26        | 1   | 0   | 0   | 1   | 0   | X   | X   | X   | X   | X   | SA79 to SA82   |
| SGA27        | 1   | 0   | 0   | 1   | 1   | X   | X   | X   | X   | X   | SA83 to SA86   |
| SGA28        | 1   | 0   | 1   | 0   | 0   | X   | X   | X   | X   | X   | SA87 to SA90   |
| SGA29        | 1   | 0   | 1   | 0   | 1   | X   | X   | X   | X   | X   | SA91 to SA94   |
| SGA30        | 1   | 0   | 1   | 1   | 0   | X   | X   | X   | X   | X   | SA95 to SA98   |
| SGA31        | 1   | 0   | 1   | 1   | 1   | X   | X   | X   | X   | X   | SA99 to SA102  |
| SGA32        | 1   | 1   | 0   | 0   | 0   | X   | X   | X   | X   | X   | SA103 to SA106 |
| SGA33        | 1   | 1   | 0   | 0   | 1   | X   | X   | X   | X   | X   | SA107 to SA110 |
| SGA34        | 1   | 1   | 0   | 1   | 0   | X   | X   | X   | X   | X   | SA111 to SA114 |
| SGA35        | 1   | 1   | 0   | 1   | 1   | X   | X   | X   | X   | X   | SA115 to SA118 |
| SGA36        | 1   | 1   | 1   | 0   | 0   | X   | X   | X   | X   | X   | SA119 to SA122 |
| SGA37        | 1   | 1   | 1   | 0   | 1   | X   | X   | X   | X   | X   | SA123 to SA126 |
| SGA38        | 1   | 1   | 1   | 1   | 0   | X   | X   | X   | X   | X   | SA127 to SA130 |
| SGA39        | 1   | 1   | 1   | 1   | 1   | 0   | 0   | X   | X   | X   | SA131 to SA133 |
|              |     |     |     |     |     | 0   | 1   |     |     |     |                |
|              |     |     |     |     |     | 1   | 0   |     |     |     |                |
| SGA40        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 0   | 0   | SA134          |
| SGA41        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 0   | 1   | SA135          |
| SGA42        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 1   | 0   | SA136          |
| SGA43        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 1   | 1   | SA137          |
| SGA44        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 0   | SA138          |
| SGA45        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | 1   | SA139          |
| SGA46        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 0   | SA140          |
| SGA47        | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | SA141          |

## FLASH MEMORY AUTOSELECT CODES

| Type                                |                           | A <sub>21</sub> to A <sub>12</sub> | A <sub>6</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | A <sub>-1</sub> <sup>(1)</sup> | Code (HEX)         |
|-------------------------------------|---------------------------|------------------------------------|----------------|----------------|----------------|----------------|----------------|--------------------------------|--------------------|
| Manufacturer's Code                 |                           | BA                                 | VIL            | VIL            | VIL            | VIL            | VIL            | VIL                            | 04h                |
| Device Code                         | Byte                      | BA                                 | VIL            | VIL            | VIL            | VIL            | VIH            | VIL                            | 7Eh                |
|                                     | Word                      | BA                                 | VIL            | VIL            | VIL            | VIL            | VIH            | X                              | 227Eh              |
| Extended Device Code <sup>(3)</sup> | Byte                      | BA                                 | VIL            | VIH            | VIH            | VIH            | VIL            | VIL                            | 02h                |
|                                     | Word                      | BA                                 | VIL            | VIH            | VIH            | VIH            | VIL            | X                              | 2202h              |
| Extended Device Code <sup>(3)</sup> | Byte                      | BA                                 | VIL            | VIH            | VIH            | VIH            | VIH            | VIL                            | 01h                |
|                                     | Word                      | BA                                 | VIL            | VIH            | VIH            | VIH            | VIH            | X                              | 2201h              |
| Sector Group Protection             | Sector Group<br>Addresses | VIL                                | VIL            | VIL            | VIH            | VIL            | VIL            | VIL                            | 01h <sup>(2)</sup> |

**Note:**

1. A-1 is used for Byte mode.
2. Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.
3. At WORD mode, a read cycle at address (BA) 01h (at BYTE mode, (BA) 02h) outputs device code. When 227Eh (at BYTE mode, 7Eh) was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh (at BYTE mode, (BA) 1Ch) , as well as at (BA) 0Fh (at BYTE mode, (BA) 1Eh) .

## FLASH MEMORY COMMAND DEFINITIONS

| Command Sequence<br>Bus                    |              | Bus<br>Write<br>Cycle<br>Req'd | First Bus<br>Cycle |      | Second Bus<br>Write Cycle |       | Third Bus<br>Write Cycle         |      | Fourth Bus<br>Read/Write |      | Fifth Bus<br>Cycle |      | Sixth Bus<br>Cycle |      |
|--------------------------------------------|--------------|--------------------------------|--------------------|------|---------------------------|-------|----------------------------------|------|--------------------------|------|--------------------|------|--------------------|------|
|                                            |              |                                | Addr.              | Data | Addr.                     | Data  | Addr.                            | Data | Addr.                    | Data | Addr.              | Data | Addr.              | Data |
| Read / Reset                               |              |                                | XXH                | F0H  | —                         | —     | —                                | —    | —                        | —    | —                  | —    | —                  | —    |
| Read / Reset * 1                           | Word<br>Byte | 1                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | F0H  | RA                       | RD   | —                  | —    | —                  | —    |
| Autoselect                                 | Word<br>Byte | 3                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | (BA)<br>555H<br>(BA)<br>AAAH     | 90H  | —                        | —    | —                  | —    | —                  | —    |
| Program                                    | Word<br>Byte | 3                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | A0H  | PA                       | PD   | —                  | —    | —                  | —    |
| Chip Erase                                 | Word<br>Byte | 4                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | 80H  | 555H<br>AAAH             | AAH  | 2AAH<br>555H       | 55H  | 555H<br>AAAH       | 10H  |
| Sector Erase                               | Word<br>Byte | 6                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | 80H  | 555H<br>AAAH             | AAH  | 2AAH<br>555H       | 55H  | SA                 | 30H  |
| Sector Erase<br>Suspend                    | Word<br>Byte | 1                              | BA                 | B0H  | —                         | —     | —                                | —    | —                        | —    | —                  | —    | —                  | —    |
| Sector Erase<br>Resume                     | Word<br>Byte | 1                              | BA                 | 30H  | —                         | —     | —                                | —    | —                        | —    | —                  | —    | —                  | —    |
| Set to Fast Mode                           | Word<br>Byte | 3                              | 555H<br>AAH        | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | 20H  | —                        | —    | —                  | —    | —                  | —    |
| Fast Program * 2                           | Word<br>Byte | 2                              | XXH                | A0H  | PA                        | PD    | —                                | —    | —                        | —    | —                  | —    | —                  | —    |
| Reset from Fast<br>Mode * 2                | Word<br>Byte | 2                              | BA                 | 90H  | XXH                       | F0H*6 | —                                | —    | —                        | —    | —                  | —    | —                  | —    |
| Extended Sector<br>Group Protection<br>* 3 | Word<br>Byte | 4                              | XXH                | 60H  | SPA                       | 60H   | SPA                              | 40H  | SPA                      | SD   | —                  | —    | —                  | —    |
| Query * 4                                  | Word<br>Byte | 1                              | 55H<br>AAH         | 98h  | —                         | —     | —                                | —    | —                        | —    | —                  | —    | —                  | —    |
| Hidden-ROM<br>Entry                        | Word<br>Byte | 3                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | 88H  | —                        | —    | —                  | —    | —                  | —    |
| Hidden-ROM<br>Program<br>* 5               | Word<br>Byte | 4                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | A0H  | PA                       | PD   | —                  | —    | —                  | —    |
| Hidden-ROM<br>Erase<br>* 5                 | Word<br>Byte | 6                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | 555H<br>AAAH                     | 80H  | 555H<br>AAAH             | AAH  | 2AAH<br>555H       | 55H  | HRA                | 30H  |
| Hidden-Rom Exit<br>* 5                     | Word<br>Byte | 4                              | 555H<br>AAAH       | AAH  | 2AAH<br>555H              | 55H   | (HRBA)<br>555H<br>(HRBA)<br>AAAH | 90H  | XXH                      | 00H  | —                  | —    | —                  | —    |

**Note:**

\*1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

\*2: This command is valid during Fast Mode.

\*3: This command is valid while RESET=VID.

\*4: The valid Address is A0 to A6.

\*5: This command is valid during Hi-ROM mode.

\*6: The data "00h" is also acceptable.

**FLASH MEMORY COMMAND DEFINITIONS Continued:**

Address bits A21 to A11 = X = "H" or "L" for all address commands except for Program Address (PA), Sector Address (SA), and Bank Address (BA).

Bus operations are defined in "Device Bus Operations".  
RA = Address of the memory location to be read  
PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.  
SA = Address of the sector to be erased.

The combination of A21, A20, A19, A18, A17, A16, A15, A14, A13, and A12 will uniquely select any sector.  
BA = Bank address (A21 to A19)  
SPA = Sector group address to be protected.

Set sector group address (SGA) and (A6, A3, A2, A1, A0) = (0, 0, 0, 1, 0) for protect; or SGA and (A6, A3, A2, A1, A0) = (1, 0, 0, 1, 0) for unprotect.

HRA= Address of the Hidden-ROM area  
Word mode: 000000h to 00007Fh  
Byte mode: 000000h to 0000FFh

HRBA = Bank address of the Hidden-ROM area  
A21 = A20 = A19 = 0

RD = Data read from location RA during read operation.  
PD = Data to be programmed at location PA.  
SD = Sector protection verify data.

Output 01h at protected sector addresses and output 00h at unprotected sector addresses.

The system should generate the following address patterns;  
Word mode : 555h or 2AAh to addresses A0 to A10  
Byte mode : AAAh or 555h to addresses A–1 and A0 to A10

**MCP ABSOLUTE MAXIMUM RATINGS<sup>(1,2,3)</sup>**

| Symbol                             | Parameter                                                  | Value                                                            | Unit   |
|------------------------------------|------------------------------------------------------------|------------------------------------------------------------------|--------|
| T <sub>BIAS</sub>                  | Temperature Under Bias                                     | –40 to +85                                                       | °C     |
| T <sub>STG</sub>                   | Storage Temperature                                        | –55 to +125                                                      | °C     |
| P <sub>D</sub>                     | Power Dissipation                                          | 1.6                                                              | W      |
| I <sub>OUT</sub>                   | Output Current (per I/O)                                   | 100                                                              | mA     |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage Relative to GND for Data, Address and Control Pins | –0.3 to V <sub>CCF</sub> + 0.3<br>–0.2 to V <sub>CCS</sub> + 0.3 | V<br>V |
| V <sub>IN</sub>                    | RESET <sup>(5)</sup>                                       | –0.5 to +13.0                                                    | V      |
| V <sub>IN</sub>                    | WP/ACC <sup>(6)</sup>                                      | –0.5 to +10.5                                                    | V      |
| V <sub>CCF</sub> /V <sub>CCS</sub> | Voltage on Vcc Supply Relative to GND <sup>(4)</sup>       | –0.3 to 3.6                                                      | V      |

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.
4. Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V<sub>SS</sub> to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V<sub>CCF</sub>+0.3 V or V<sub>CCS</sub>+0.3 V. During voltage transitions, input or I/O pins may overshoot to V<sub>CCF</sub>+2.0 V or V<sub>CCS</sub>+2.0 V for periods of up to 20 ns.
5. Minimum DC input voltage on RESET pin is –0.5 V. During voltage transitions, RESET pin may undershoot V<sub>SS</sub> to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V<sub>IN</sub>–V<sub>CCF</sub> or V<sub>CCS</sub>) does not exceed 9.0 V. Maximum DC input voltage on RESET pin is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
6. Minimum DC input voltage on WP/ACC pin is –0.5 V. During voltage transitions, WP/ACC pin may undershoot V<sub>SS</sub> to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on WP/ACC pin is +10.5 V which may overshoot to +12.0V for periods of up to 20 ns, when V<sub>CCF</sub> is applied.

## IS71V08F64GS08, IS71V16F64GS08

## MCP OPERATING RANGE

| Range      | Ambient Temperature | V <sub>CCF</sub> , V <sub>CCS</sub> |
|------------|---------------------|-------------------------------------|
| Industrial | –40°C to +85°C      | 2.7–3.3V                            |

STANDARD VOLTAGE RANGE V<sub>CC</sub> = 2.7-3.3 V

|                               | FLASH<br>MEMORY |    | SRAM | UNITS |
|-------------------------------|-----------------|----|------|-------|
| Max Access Time               | 70              | 85 | 70   | ns    |
| $\overline{\text{CE}}$ Access | 70              | 85 | 70   | ns    |
| $\overline{\text{OE}}$ Access | 30              | 40 | 35   | ns    |

CAPACITANCE<sup>(1)</sup>

| Symbol           | Parameter                                   | Conditions            | Typ. | Max. | Unit |
|------------------|---------------------------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance                           | V <sub>IN</sub> = 0V  | 11   | 14   | pF   |
| C <sub>OUT</sub> | Output Capacitance                          | V <sub>OUT</sub> = 0V | 12   | 16   | pF   |
| C <sub>IN2</sub> | Control Pin Capacitance                     | V <sub>IN</sub> = 0V  | 14   | 16   | pF   |
| C <sub>IN3</sub> | $\overline{\text{WP}}$ /ACC Pin Capacitance | V <sub>IN</sub> = 0V  | 21.5 | 26   | pF   |

## Notes:

1. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz

## MCP DC CHARACTERISTICS

| Symbol           | Parameter                                                                               | Test Conditions                                                                                               | Min. | Max.                                 | Unit |
|------------------|-----------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|------|--------------------------------------|------|
| I <sub>LI</sub>  | Input Leakage                                                                           | V <sub>IN</sub> =V <sub>SS</sub> to V <sub>ccf</sub> , V <sub>CCS</sub>                                       | -1.0 | 1.0                                  | μA   |
| I <sub>LO</sub>  | Output Leakage                                                                          | V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>ccf</sub> , V <sub>CCS</sub>                                      | -1.0 | 1.0                                  | μA   |
| V <sub>IL</sub>  | Input Low Level                                                                         |                                                                                                               | -0.2 | 0.5                                  | V    |
| V <sub>IH</sub>  | Input High Level                                                                        |                                                                                                               | 2.4  | V <sub>CC</sub> ± 0.3 <sup>(2)</sup> | V    |
| V <sub>ID</sub>  | Voltage for Sector Protection, and Temporary Sector Unprotection (RESET) <sup>(1)</sup> |                                                                                                               | 11.5 | 12.5                                 | V    |
| V <sub>ACC</sub> | Voltage for Program Acceleration ( WP/ACC) <sup>(1)</sup>                               |                                                                                                               | 8.5  | 9.5                                  | V    |
| V <sub>OL</sub>  | Output Low Level                                                                        | V <sub>ccf</sub> = V <sub>ccf</sub> min., V <sub>CCS</sub> =V <sub>CCS</sub> min.<br>I <sub>OL</sub> = 1.0mA  | —    | 0.4                                  | V    |
| V <sub>OH</sub>  | Output High Level                                                                       | V <sub>ccf</sub> = V <sub>ccf</sub> min., V <sub>CCS</sub> =V <sub>CCS</sub> min.<br>I <sub>OH</sub> = -0.5mA | 2.4  | —                                    | V    |
| V <sub>LKO</sub> | Flash Low V <sub>ccf</sub>                                                              |                                                                                                               | 2.3  | 2.5                                  | V    |

**Notes:**

1. Applicable for only V<sub>ccf</sub> applying.
2. V<sub>CC</sub> indicates lower of V<sub>ccf</sub> or V<sub>CCS</sub>.

## FLASH DC CHARACTERISTICS

| Symbol            | Parameter                                                                      | Test Conditions                                                                                                                                                                             | Min.             | Max.               | Unit |
|-------------------|--------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------------|------|
| I <sub>LIT</sub>  | RESET Inputs Leakage Current                                                   | V <sub>ccf</sub> =V <sub>ccf</sub> max., V <sub>ccs</sub> =V <sub>ccs</sub> max.<br>RESET = 12.5V                                                                                           | —                | 35                 | μA   |
| I <sub>LIA</sub>  | ACC Inputs Leakage Current                                                     | V <sub>ccf</sub> =V <sub>ccf</sub> max., V <sub>ccs</sub> =V <sub>ccs</sub> max.<br>WP/ACC = V <sub>acc</sub> max.                                                                          | —                | 20                 | μA   |
| I <sub>cc1f</sub> | FLASH V <sub>cc</sub> <sup>(1)</sup><br>Active Current (Read)                  | CEf=V <sub>IL</sub> tCycle = 5Mhz Byte<br>OE=V <sub>IH</sub> tCycle = 5Mhz Word<br>tCycle = 1Mhz Byte<br>tCycle = 1Mhz Word                                                                 | —<br>—<br>—<br>— | 16<br>18<br>7<br>7 | mA   |
| I <sub>cc2f</sub> | FLASH V <sub>cc</sub> Active <sup>(2)</sup><br>Current(Program/Erase)          | CEf=V <sub>IL</sub><br>OE=V <sub>IH</sub>                                                                                                                                                   | —                | 35                 | mA   |
| I <sub>cc3f</sub> | FLASH V <sub>cc</sub> Active <sup>(4)</sup><br>Current<br>(Read-While-Program) | CEf=V <sub>IL</sub> Byte<br>OE=V <sub>IH</sub> Word                                                                                                                                         | —                | 51<br>53           | mA   |
| I <sub>cc4f</sub> | FLASH V <sub>cc</sub> Active <sup>(4)</sup><br>Current<br>(Read-While-Erase)   | CEf=V <sub>IL</sub> Byte<br>OE=V <sub>IH</sub> Word                                                                                                                                         | —                | 51<br>53           | mA   |
| I <sub>cc5f</sub> | FLASH V <sub>cc</sub> Active<br>Current<br>(Erase-Suspend-Program)             | CEf=V <sub>IL</sub><br>OE=V <sub>IH</sub>                                                                                                                                                   | —                | 35                 | mA   |
| I <sub>SB1f</sub> | FLASH V <sub>cc</sub><br>Standby Current                                       | V <sub>ccf</sub> = V <sub>cc</sub> max, CEf= V <sub>ccf</sub> = ± 0.3V<br>RESET, CEf, WP/ACC = V <sub>ccf</sub> = ± 0.3V                                                                    | —                | 5                  | μA   |
| I <sub>SB2f</sub> | FLASH V <sub>cc</sub><br>Standby Current<br>(RESET)                            | V <sub>ccf</sub> = V <sub>cc</sub> max, RESET= V <sub>ss</sub> = ± 0.3V<br>WP/ACC = V <sub>ccf</sub> = ± 0.3V                                                                               | —                | 5                  | μA   |
| I <sub>SB3f</sub> | FLASH V <sub>cc</sub> <sup>(3)</sup><br>Standby Current<br>(Auto Sleep Mode)   | V <sub>ccf</sub> = V <sub>cc</sub> max. CEf, = V <sub>ss</sub> = ± 0.3V<br>RESET, WP/ACC = V <sub>ccf</sub> = ± 0.3V<br>V <sub>IN</sub> = V <sub>ccf</sub> ± 0.3V OR V <sub>ss</sub> ± 0.3V | —                | 5                  | μA   |

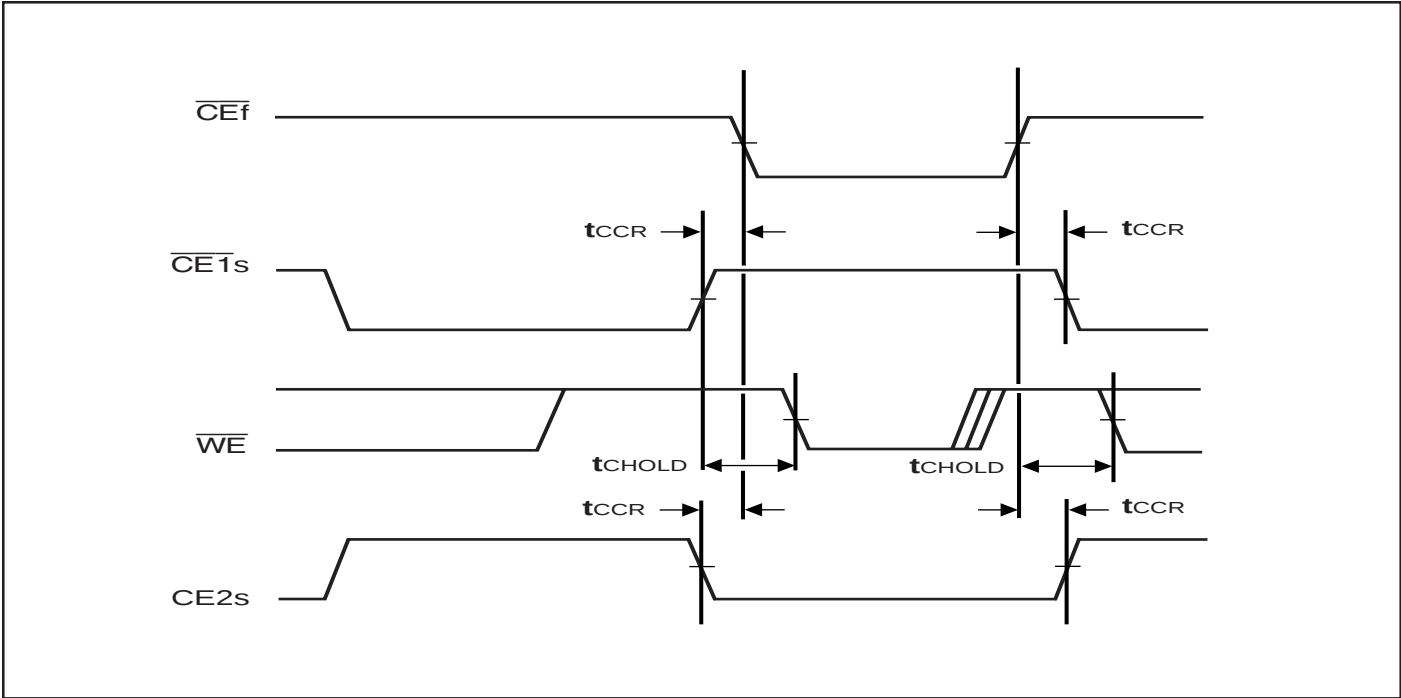
**Notes:**

1. The ICC current listed includes both the DC operating current and the frequency dependent component.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns..
4. Embedded Algorithm (program or erase) is in progress. (@5 MHz)

AC CHARACTERISTICS -  $\overline{CE}$  TIMING

| Parameter                    | JEDEC Symbol | Standard Symbol | Condition | Min | Unit |
|------------------------------|--------------|-----------------|-----------|-----|------|
| $\overline{CE}$ Recover Time | —            | $t_{CCR}$       | —         | 0   | ns   |
| $\overline{CE}$ Hold Time    | —            | $t_{CHOLD}$     | —         | 3   | ns   |

TIMING DIAGRAM FOR ALTERNATING SRAM TO FLASH



**FLASH READ ONLY SWITCHING CHARACTERISTICS**

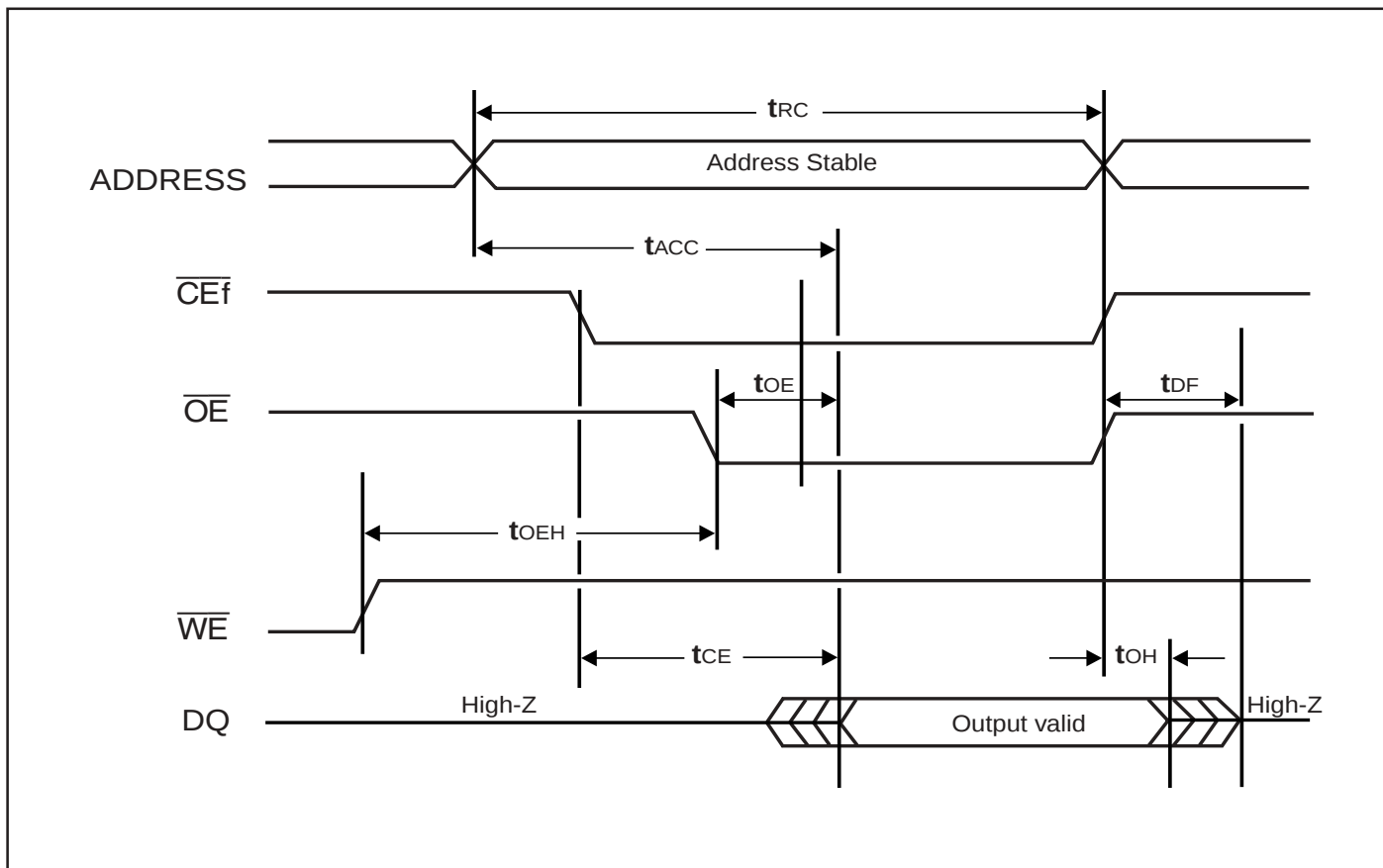
(Over Operating Range)

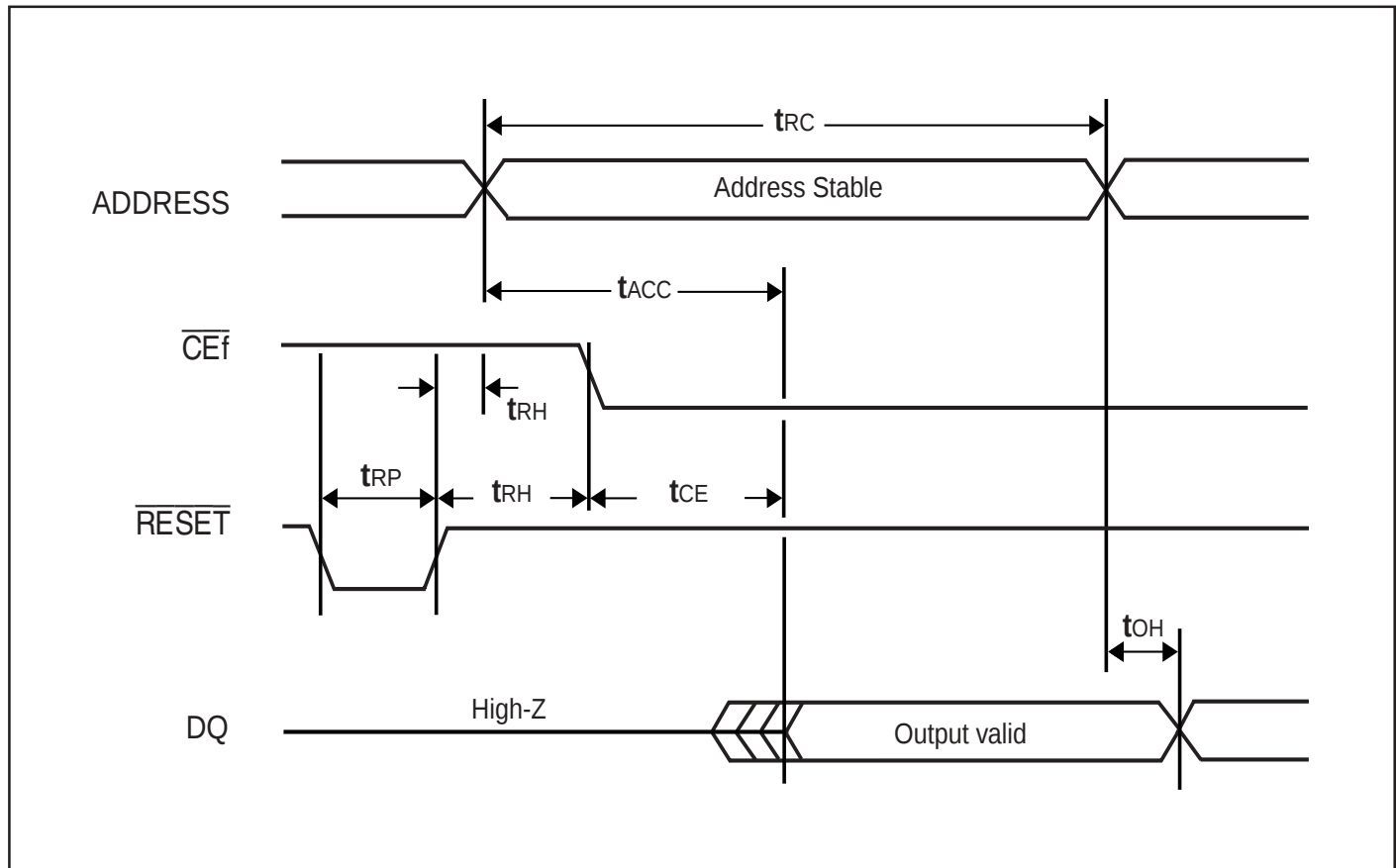
| Symbol             | Parameter                                                                        | Min. | Max. | Min. | Max. | Unit |
|--------------------|----------------------------------------------------------------------------------|------|------|------|------|------|
| t <sub>RC</sub>    | Cycle Time                                                                       | 70   |      | 85   | —    | ns   |
| t <sub>ACC</sub>   | Address to Output Delay                                                          | —    | 70   | —    | 85   | ns   |
| t <sub>CE</sub>    | Chip Enable to Output Delay                                                      | —    | 70   | —    | 85   | ns   |
| t <sub>OE</sub>    | Output Enable to Output Delay                                                    | —    | 30   | —    | 40   | ns   |
| t <sub>DF</sub>    | Chip Enable to Output High-Z                                                     | —    | 30   | —    | 30   | ns   |
| t <sub>DF</sub>    | Output Enable to Output High-Z                                                   | —    | 30   | —    | 30   | ns   |
| t <sub>OH</sub>    | Output Hold Time from Addresses, CE $\overline{f}$ or OE, Whichever Occurs First | 0    | —    | 0    | —    | ns   |
| t <sub>READY</sub> | $\overline{\text{RESET}}$ Pin Low to Read Mode                                   | —    | 20   | —    | 20   | μs   |

**FLASH AC TEST CONDITIONS**

| Parameter                                   | Unit                |
|---------------------------------------------|---------------------|
| Input Pulse Level                           | 0V to 3.0V          |
| Input Rise and Fall Times                   | 5 ns                |
| Input and Output Timing and Reference Level | 1.5V                |
| Output Load                                 | 1 TTL gate and 30pF |

## FLASH READ CYCLE



FLASH HARDWARE  $\overline{\text{RESET}}$  / READ OPERATION TIMING DIAGRAM

**FLASH Erase/Program Operation Characteristics** (Over Operating Range)

| Symbol             | Parameter                                                                                 | -70 ns |      | -85ns |      | Unit |
|--------------------|-------------------------------------------------------------------------------------------|--------|------|-------|------|------|
|                    |                                                                                           | Min.   | Max. | Min.  | Max. |      |
| t <sub>WC</sub>    | Write Cycle Time                                                                          | 70     | -    | 85    | -    | ns   |
| t <sub>AS</sub>    | Address Setup Time ( $\overline{WE}$ to Addr.)                                            | 0      | -    | 0     | -    | ns   |
| t <sub>ASO</sub>   | Address Setup Time to $\overline{CEf}$ Low During Toggle Bit Polling                      | 15     | -    | 15    | -    | ns   |
| t <sub>AH</sub>    | Address Hold Time ( $\overline{WE}$ to Addr.)                                             | 45     | -    | 45    | -    | ns   |
| t <sub>AHT</sub>   | Address Hold Time from $\overline{CEf}$ or $\overline{OE}$ High During Toggle Bit Polling | 0      | -    | 0     | -    | ns   |
| t <sub>DS</sub>    | Data Setup Time                                                                           | 35     | -    | 45    | -    | ns   |
| t <sub>DH</sub>    | Data Hold Time                                                                            | 0      | -    | 0     | -    | ns   |
| t <sub>OES</sub>   | Output Enable Setup Time                                                                  | 0      | -    | 0     | -    | ns   |
| t <sub>OEHL</sub>  | Output Enable Hold Time Read                                                              | 0      | -    | 0     | -    | ns   |
| t <sub>OEH</sub>   | Output Enable Hold Time Toggle and Data Polling                                           | 10     | -    | 10    | -    | ns   |
| t <sub>CEPH</sub>  | $\overline{CEf}$ High During Toggle Bit Polling                                           | 20     | -    | 20    | -    | ns   |
| t <sub>OEPH</sub>  | $\overline{OE}$ High During Toggle Bit Polling                                            | 20     | -    | 20    | -    | ns   |
| t <sub>GHEL</sub>  | Read Recover Time Before Write ( $\overline{OE}$ to $\overline{CEf}$ )                    | 0      | -    | 0     | -    | ns   |
| t <sub>GHWL</sub>  | Read Recover Time Before Write ( $\overline{OE}$ to $\overline{WE}$ )                     | 0      | -    | 0     | -    | ns   |
| t <sub>WS</sub>    | WE Setup Time ( $\overline{CEf}$ to $\overline{WE}$ )                                     | 0      | -    | 0     | -    | ns   |
| t <sub>CS</sub>    | $\overline{CEf}$ Setup Time ( $\overline{WE}$ to $\overline{CEf}$ )                       | 0      | -    | 0     | -    | ns   |
| t <sub>WH</sub>    | $\overline{WE}$ Hold Time ( $\overline{CEf}$ to $\overline{WE}$ )                         | 0      | -    | 0     | -    | ns   |
| t <sub>CH</sub>    | $\overline{CEf}$ Hold Time ( $\overline{WE}$ to $\overline{CEf}$ )                        | 0      | -    | 0     | -    | ns   |
| t <sub>WP</sub>    | Write Pulse Width                                                                         | 30     | -    | 35    | -    | ns   |
| t <sub>CP</sub>    | $\overline{CEf}$ Pulse Width                                                              | 30     | -    | 35    | -    | ns   |
| t <sub>WPH</sub>   | Write Pulse Width High                                                                    | 30     | -    | 30    | -    | ns   |
| t <sub>CPH</sub>   | $\overline{CEf}$ Pulse Width High                                                         | 30     | -    | 30    | -    | ns   |
| t <sub>WHWH1</sub> | Byte Programming Operation                                                                | -      | 12   | -     | 15   | μs   |
| t <sub>WHWH1</sub> | Word Programming Operation                                                                | -      | 15   | -     | 20   | μs   |
| t <sub>WHWH2</sub> | Sector Erase Operation <sup>(1)</sup>                                                     | -      | 0.7  | -     | 1    | s    |
| t <sub>VCS</sub>   | V <sub>ccf</sub> Setup Time                                                               | 50     | -    | 50    | -    | μs   |

**Note:**

1. This reflects typical value not maximum value and does not include the preprogramming time.

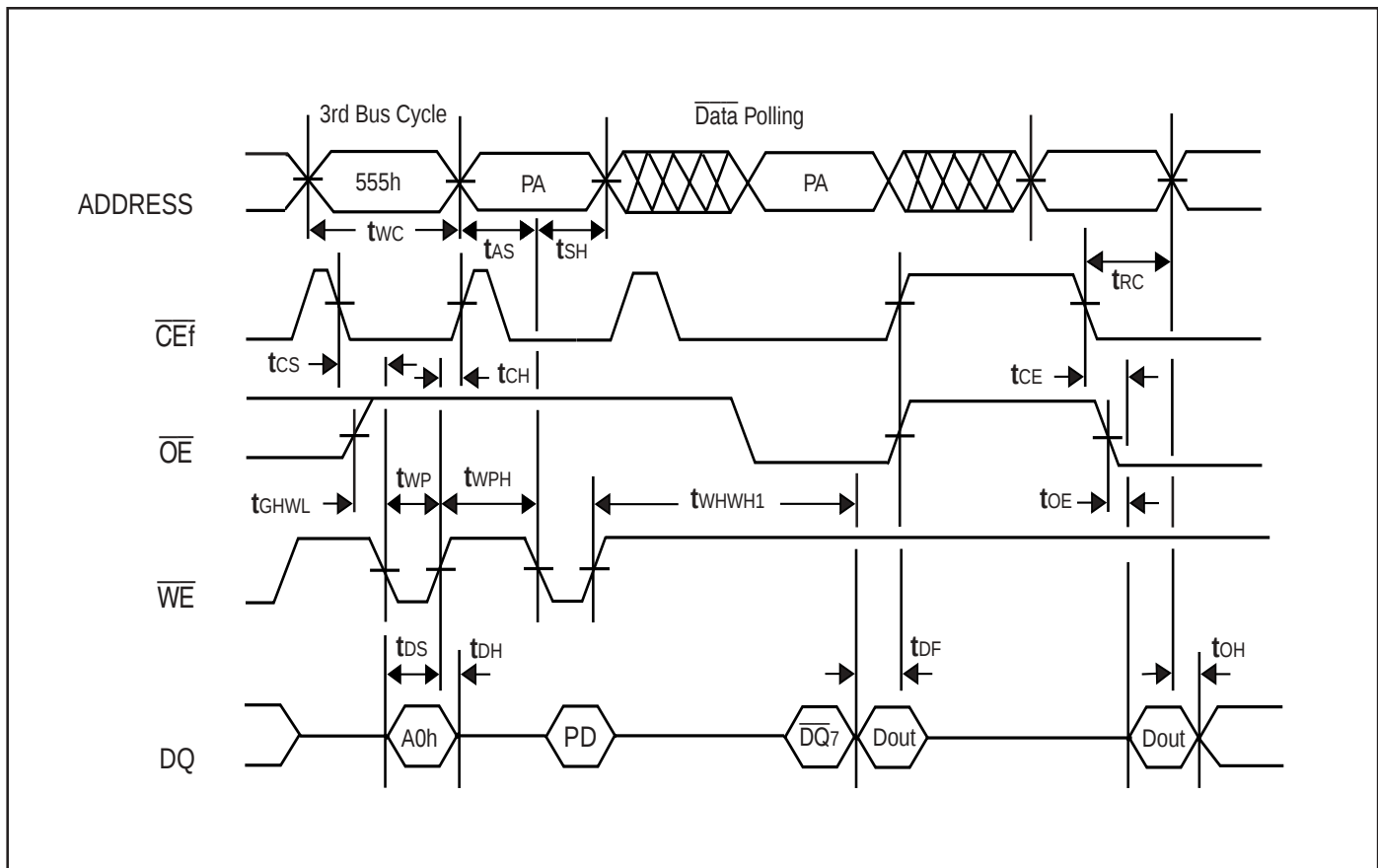
**FLASH Erase/Program Operation Characteristics** Continued (Over Operating Range)

| Symbol             | Parameter                                               | -70 ns |      | -85ns |      | Unit |
|--------------------|---------------------------------------------------------|--------|------|-------|------|------|
|                    |                                                         | Min.   | Max. | Min.  | Max. |      |
| t <sub>VLHT</sub>  | Voltage Transition Time <sup>(2)</sup>                  | 4      | -    | 4     | -    | μs   |
| t <sub>VIDR</sub>  | Rise Time to V <sub>ID</sub> <sup>(2)</sup>             | 500    | -    | 500   | -    | ns   |
| t <sub>VACCA</sub> | Rise Time to V <sub>ACC</sub>                           | 500    | -    | 500   | -    | ns   |
| t <sub>RB</sub>    | Recovery Time from RY/ $\overline{\text{BY}}$           | 0      | -    | 0     | -    | ns   |
| t <sub>RP</sub>    | $\overline{\text{RESET}}$ Pulse Width                   | 500    | -    | 500   | -    | ns   |
| t <sub>EOE</sub>   | Delay Time from Embedded Output Enable                  | -      | 70   | -     | 85   | ns   |
| t <sub>RH</sub>    | $\overline{\text{RESET}}$ High Level Period Before Read | 100    | -    | 200   | -    | ns   |
| t <sub>BUSY</sub>  | Program/Erase Valid to RY/ $\overline{\text{BY}}$ Delay | -      | 75   | -     | 90   | ns   |
| t <sub>TOW</sub>   | Erase Time-out Time <sup>(3)</sup>                      | 50     | -    | 50    | -    | μs   |
| t <sub>SPD</sub>   | Erase Suspend Transition Time <sup>(4)</sup>            | -      | 20   | -     | 20   | μs   |

**Note:**

2. This timing is for Sector Protection Operation.
3. The time between writes must be less than "t<sub>TOW</sub>" otherwise that command will not be accepted and erasure will start. A time-out or "t<sub>TOW</sub>" from the rising edge of last  $\overline{\text{CEf}}$  or  $\overline{\text{WE}}$  whichever happens first will initiate the execution of the Sector Erase command(s).
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t<sub>SPD</sub>" to suspend the erase operation.

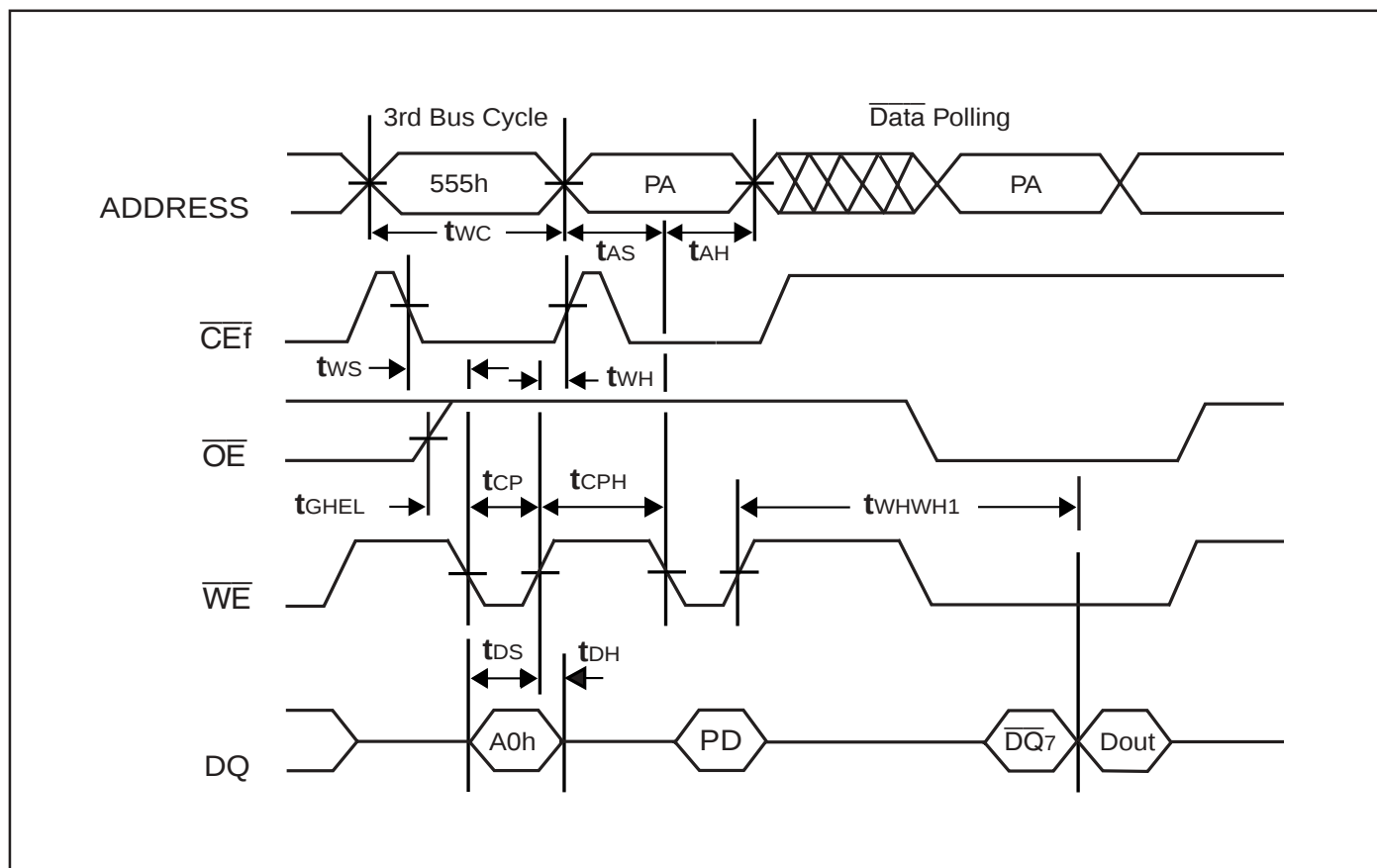
## FLASH WRITE CYCLE

( $\overline{\text{WE}}$  Control)

## Notes:

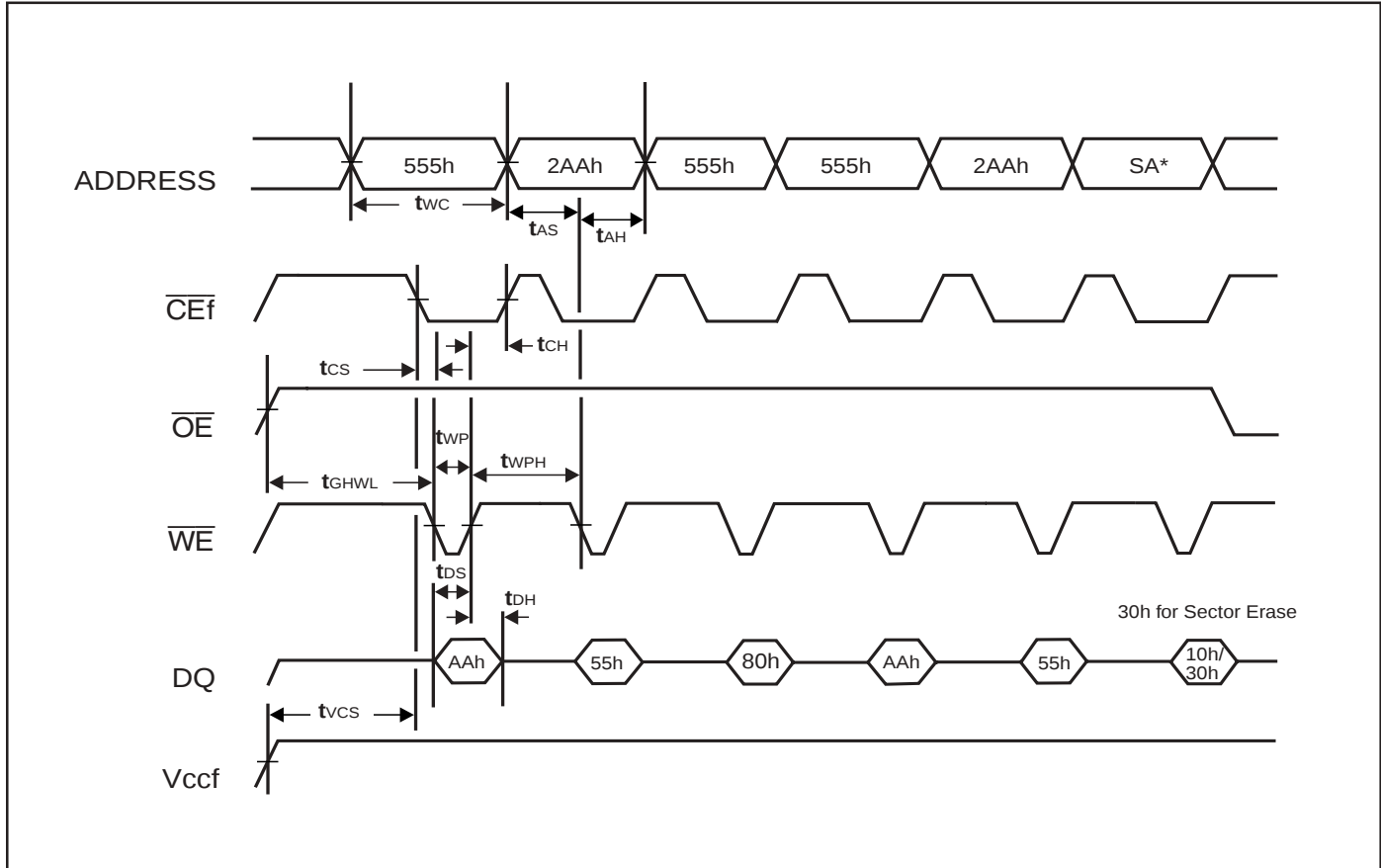
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the  $\times 16$  mode (the addresses differ from  $\times 8$  mode, i.e. AAAh).

## FLASH WRITE CYCLE

( $\overline{\text{CEf}}$  Control)**Notes:**

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the  $\times 16$  mode (the addresses differ from  $\times 8$  mode, i.e. AAAh).

## FLASH AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

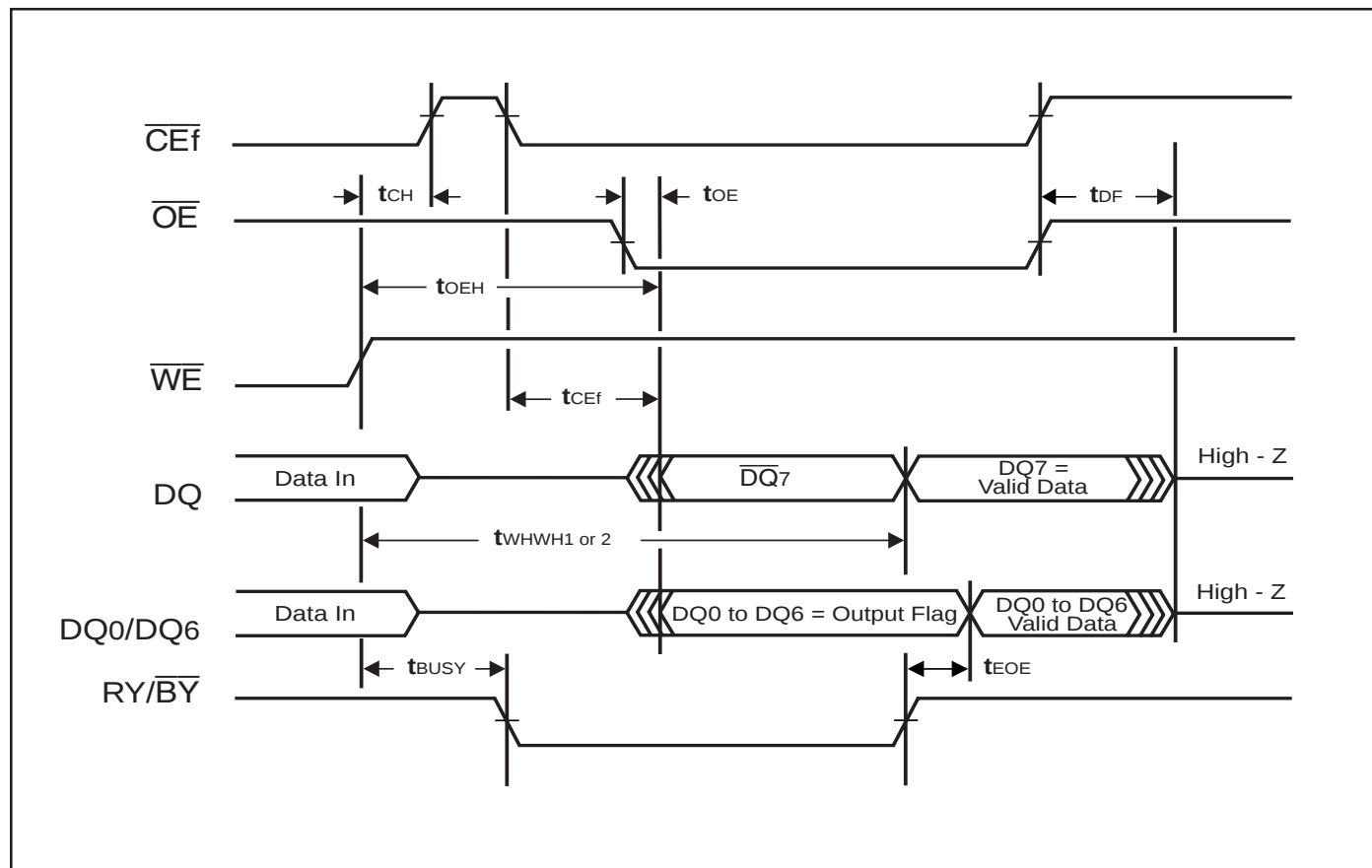


\*SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

**Note:**

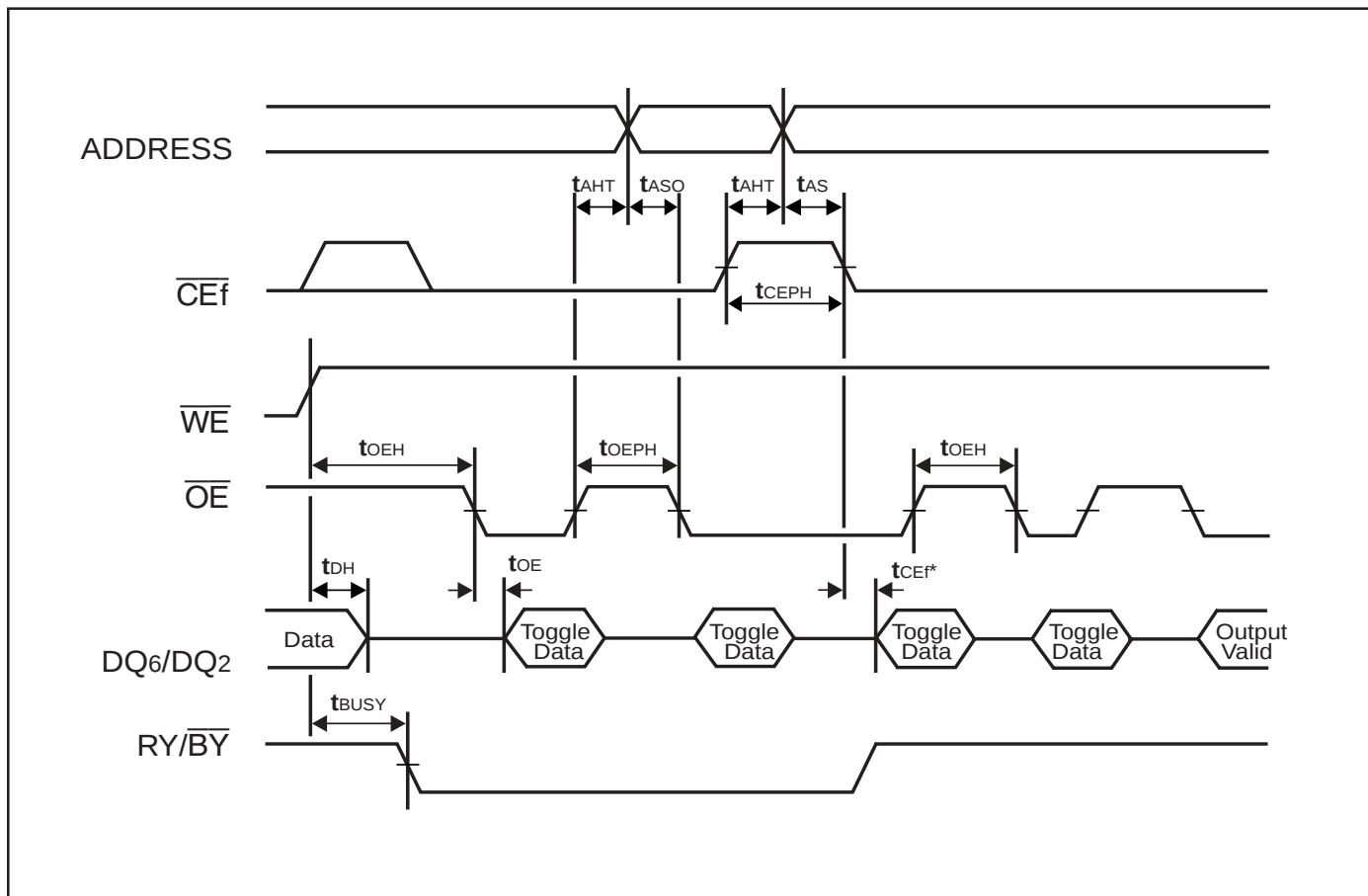
These waveforms are for the ×16 mode (the addresses differ from ×8 mode: AAh, 555h, AAh, AAh, 555h, SA\*).

# FLASH AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALOGRITHM OPERATIONS



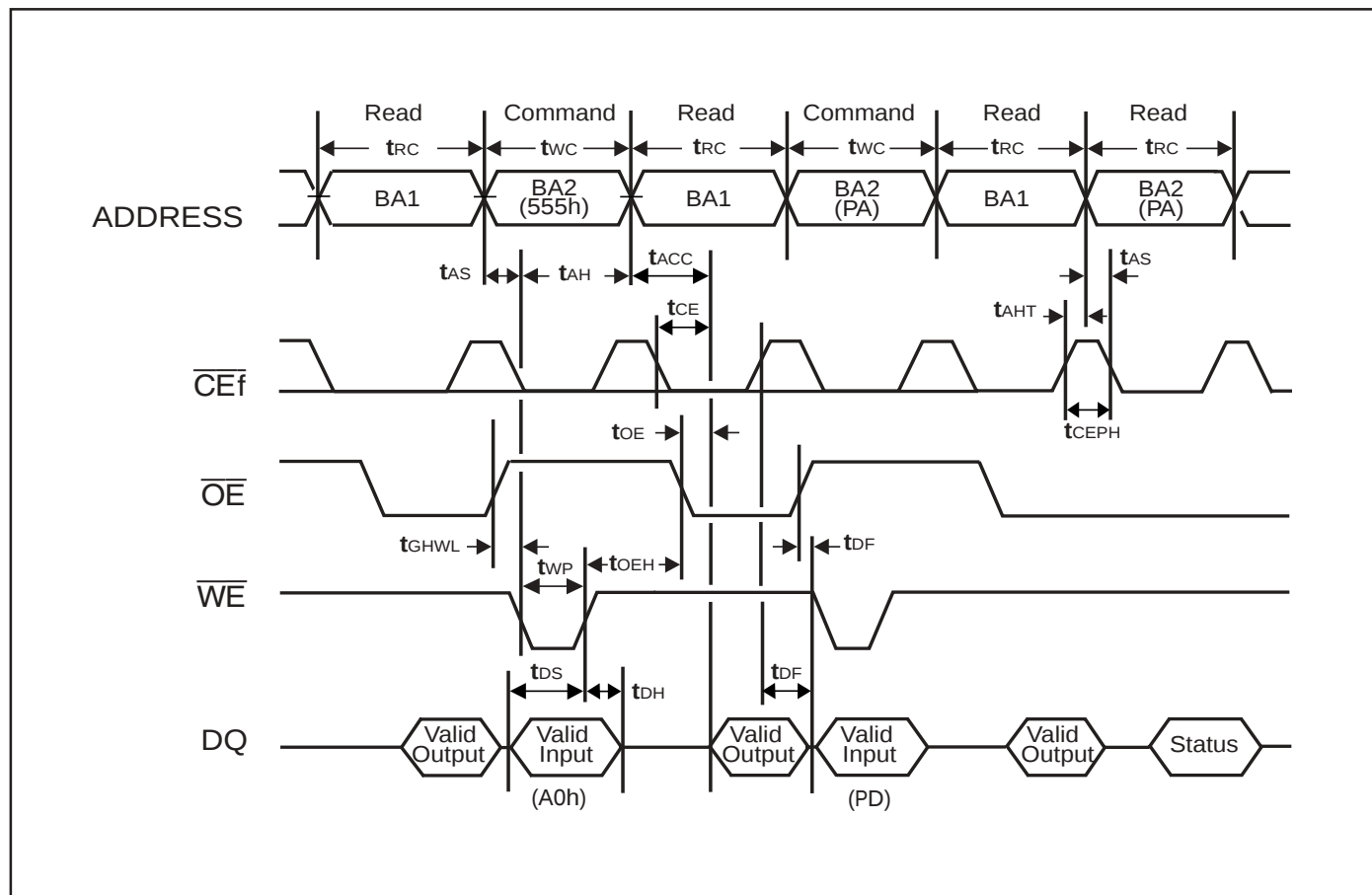
\*DQ7 = Valid Data (the device has completed the Embedded operation.)

## FLASH AC WAVEFORMS FOR TOGGLE BIT DURING EMBEDDED ALGORITHM OPERATIONS



\* DQ6 stops toggling (the device has completed the Embedded operation).

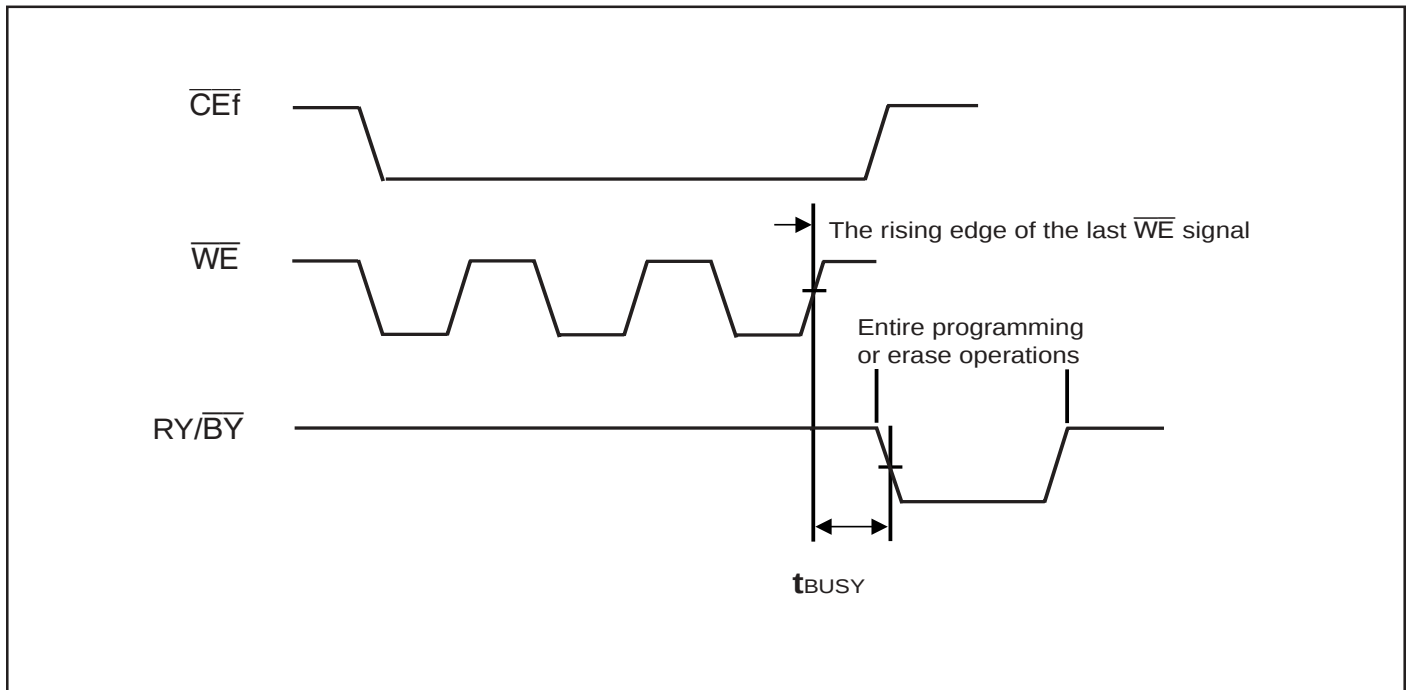
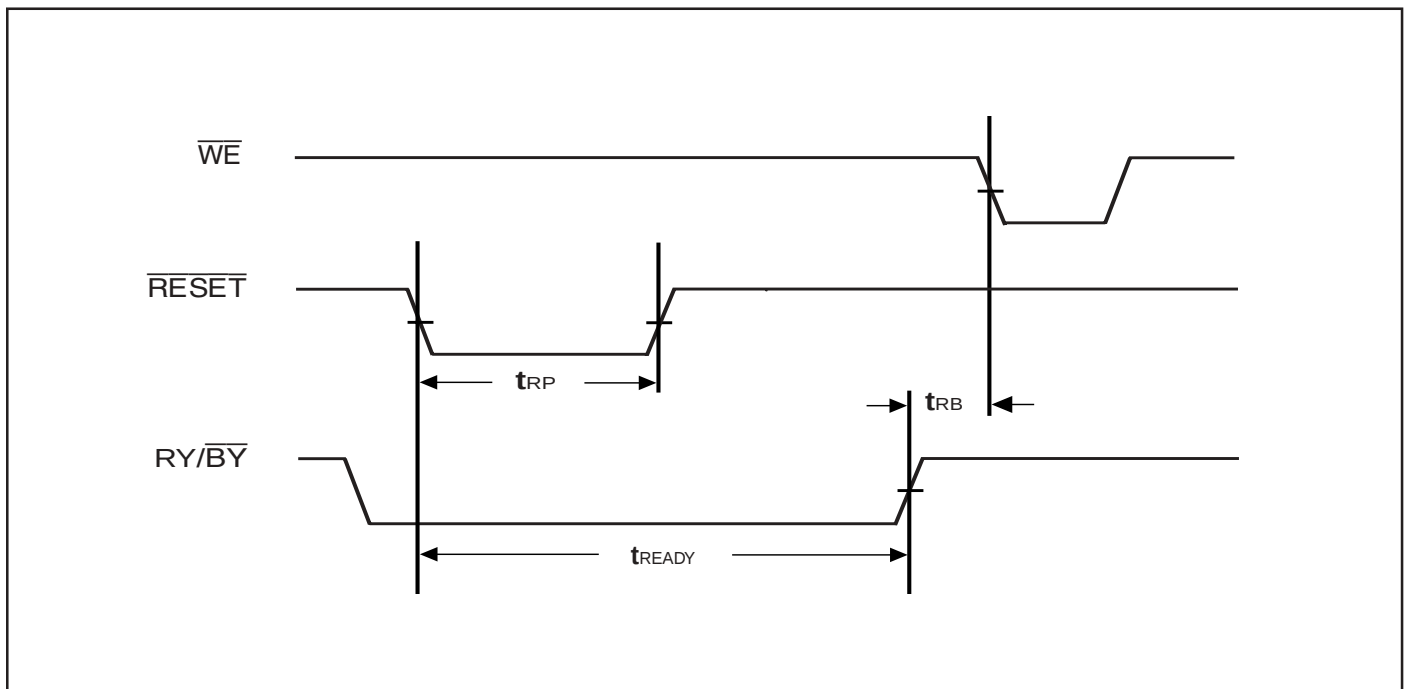
## FLASH BACK-TO-BACK READ/WRITE TIMING DIAGRAM

**Note:**

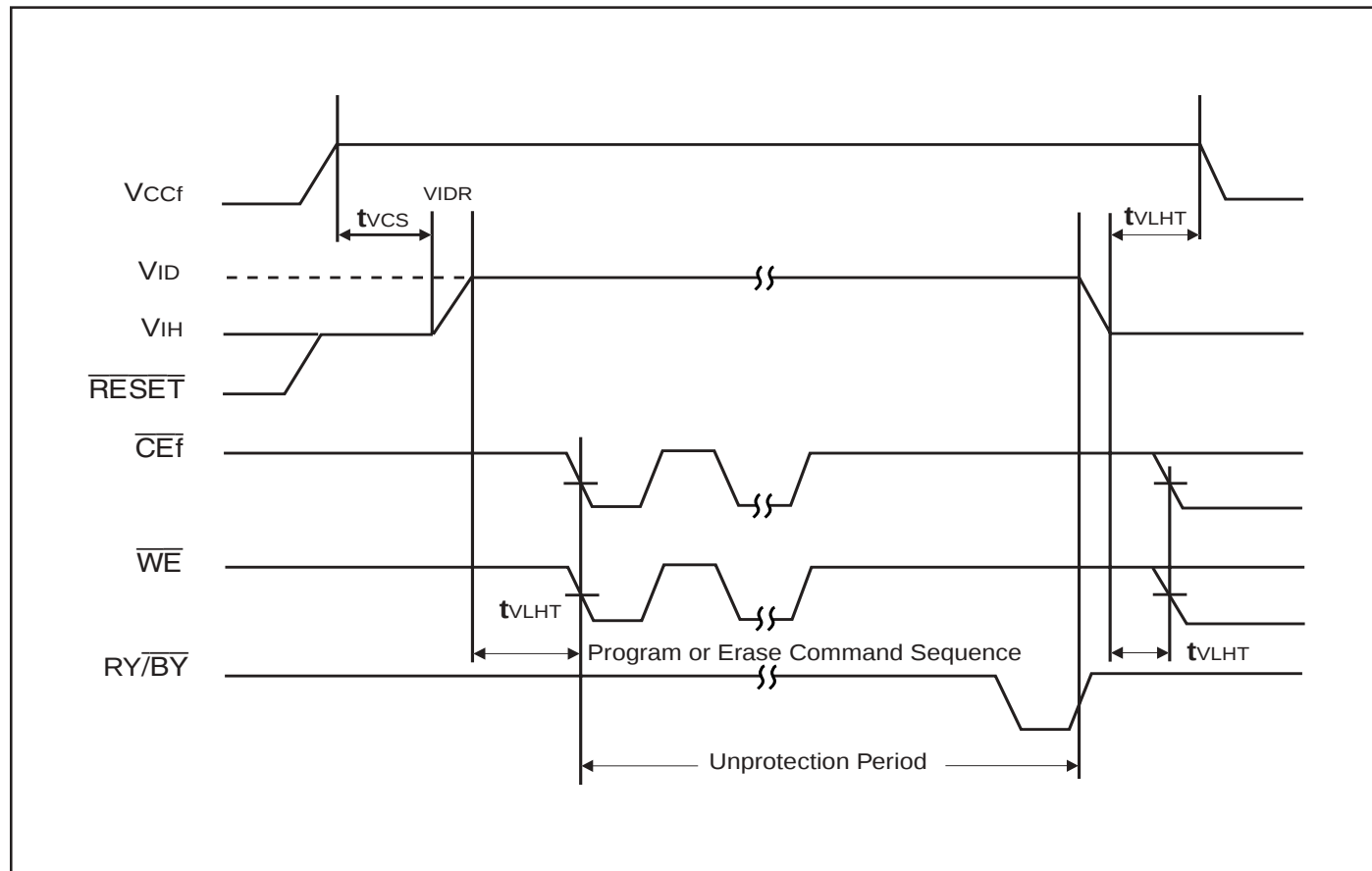
This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.

BA1: Address of Bank 1.

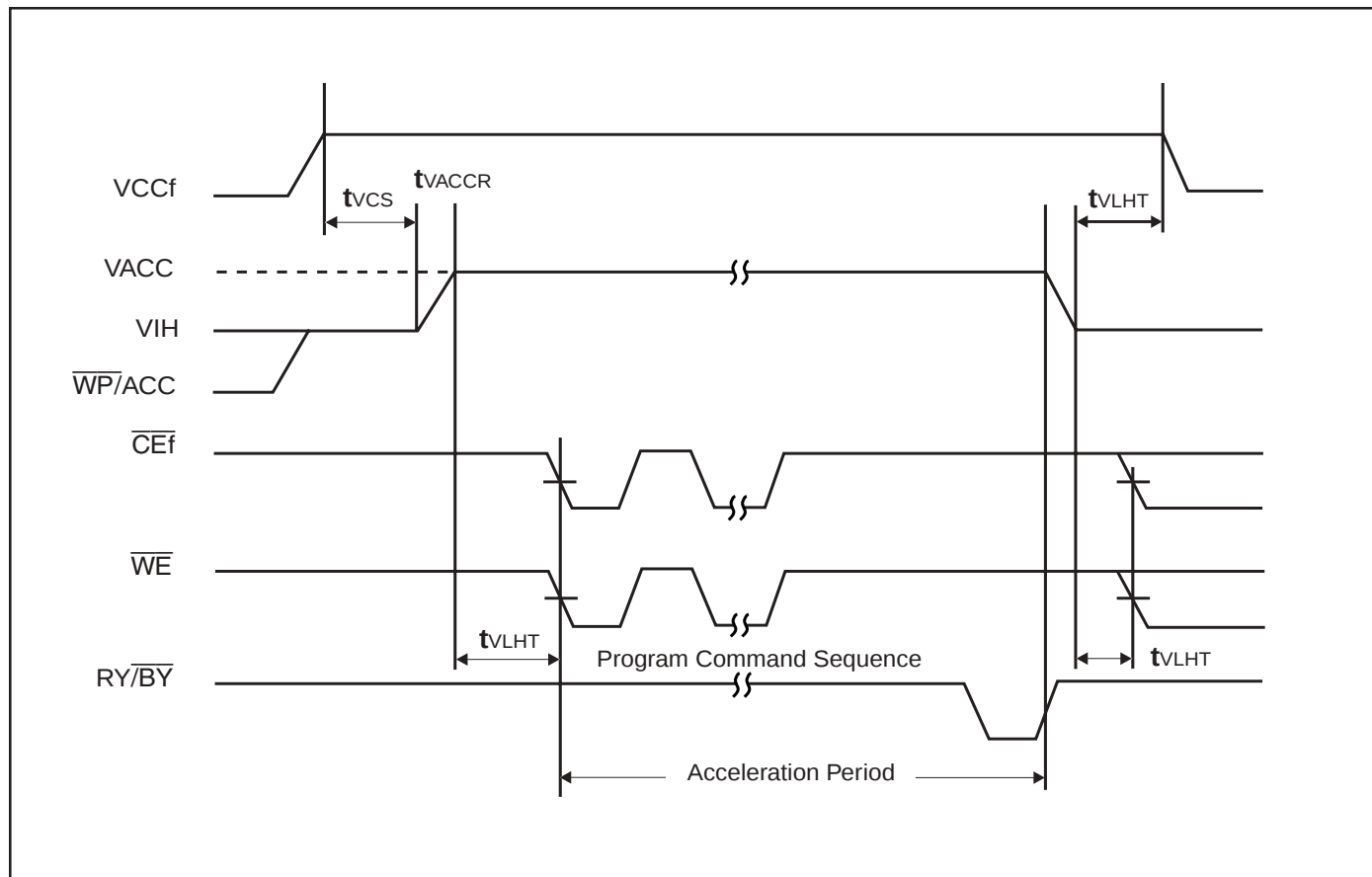
BA2: Address of Bank 2.

FLASH  $\overline{\text{RY}}/\overline{\text{BY}}$  TIMING DIAGRAM DURING WRITE/ERASE OPERATIONSFLASH  $\overline{\text{RESET}}$   $\overline{\text{RY}}/\overline{\text{BY}}$  TIMING DIAGRAM

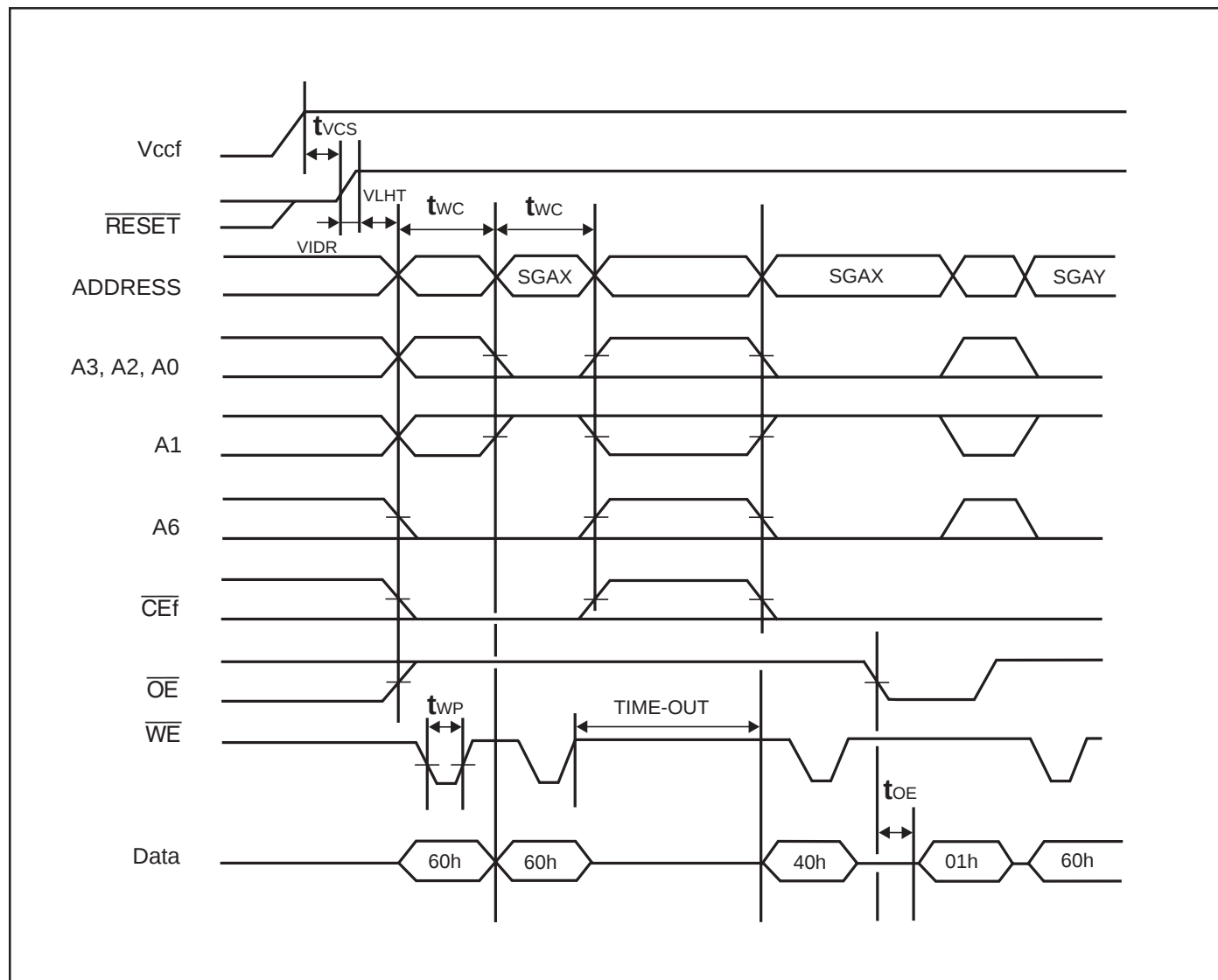
## FLASH TEMPORARY SECTOR GROUP UNPROTECTION



## FLASH ACCELERATED PROGRAM



## FLASH EXTENDED SECTOR GROUP PROTECTION



SGAx: Sector Group Address to be protected. SGAY: Next Group Sector Address to be protected

UNPROTECTION: Implement with A6 = 1, A1 = 1, A0 = 0. Time-out approximately 15 ms.

TIME-OUT : Time-Out window = 250  $\mu$ s (Min.)

**SRAM POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

| Symbol           | Parameter                                        | Test Conditions                                                                                                                                                                  | Min. | Max. | Unit |
|------------------|--------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|
| I <sub>CC</sub>  | V <sub>CC</sub> Dynamic Operating Supply Current | V <sub>CCS</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>                                                                                                        | —    | 25   | mA   |
| I <sub>CC1</sub> | Operating Supply Current                         | V <sub>CCS</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA, f = 0                                                                                                                       | —    | 5    | mA   |
| I <sub>SB1</sub> | TTL Standby Current (TTL Inputs)                 | V <sub>CCS</sub> = Max.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>$\overline{CE1}_s = V_{IH}$ , $CE2_s = V_{IL}$ ,<br>f = 1 MHz                                | —    | 0.3  | mA   |
|                  | <b>OR</b>                                        |                                                                                                                                                                                  |      |      |      |
|                  | ULB Control                                      | V <sub>CCS</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>$\overline{CE1}_s = V_{IL}$ , f = 0, $\overline{UB}_s = V_{IH}$ , $\overline{LB}_s = V_{IH}$    |      |      |      |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>CCS</sub> = Max.,<br>$\overline{CE1}_s \geq V_{CCS} - 0.2V$ ,<br>$CE2_s \leq 0.2V$ ,<br>V <sub>IN</sub> $\geq V_{CCS} - 0.2V$ , or<br>V <sub>IN</sub> $\leq 0.2V$ , f = 0 | —    | 25   | μA   |
|                  | <b>OR</b>                                        |                                                                                                                                                                                  |      |      |      |
|                  | ULB Control                                      | V <sub>CCS</sub> = Max., $\overline{CE1}_s = V_{IL}$<br>V <sub>IN</sub> $\leq 0.2V$ , f = 0; $\overline{UB}_s / \overline{LB}_s = V_{CCS} - 0.2V$                                |      |      |      |

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**SRAM READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

| Symbol            | Parameter                                           | 70 ns |      | Unit |
|-------------------|-----------------------------------------------------|-------|------|------|
|                   |                                                     | Min.  | Max. |      |
| $t_{RC}$          | Read Cycle Time                                     | 70    | —    | ns   |
| $t_{AA}$          | Address Access Time                                 | —     | 70   | ns   |
| $t_{OHA}$         | Output Hold Time                                    | 10    | —    | ns   |
| $t_{ACE1}$        | $\overline{CE1}_s$ Access Time                      | —     | 70   | ns   |
| $t_{DOE}$         | $\overline{OE}$ Access Time                         | —     | 35   | ns   |
| $t_{HZOE}^{(2)}$  | $\overline{OE}$ to High-Z Output                    | —     | 25   | ns   |
| $t_{LZOE}^{(2)}$  | $\overline{OE}$ to Low-Z Output                     | 5     | —    | ns   |
| $t_{HZCE1}^{(2)}$ | $\overline{CE1}_s$ to High-Z Output                 | 0     | 25   | ns   |
| $t_{LZCE1}^{(2)}$ | $\overline{CE1}_s$ to Low-Z Output                  | 10    | —    | ns   |
| $t_{BA}$          | $\overline{LB}_s, \overline{UB}_s$ Access Time      | —     | 70   | ns   |
| $t_{HZB}$         | $\overline{LB}_s, \overline{UB}_s$ to High-Z Output | 0     | 25   | ns   |
| $t_{LZB}$         | $\overline{LB}_s, \overline{UB}_s$ to Low-Z Output  | 0     | —    | ns   |

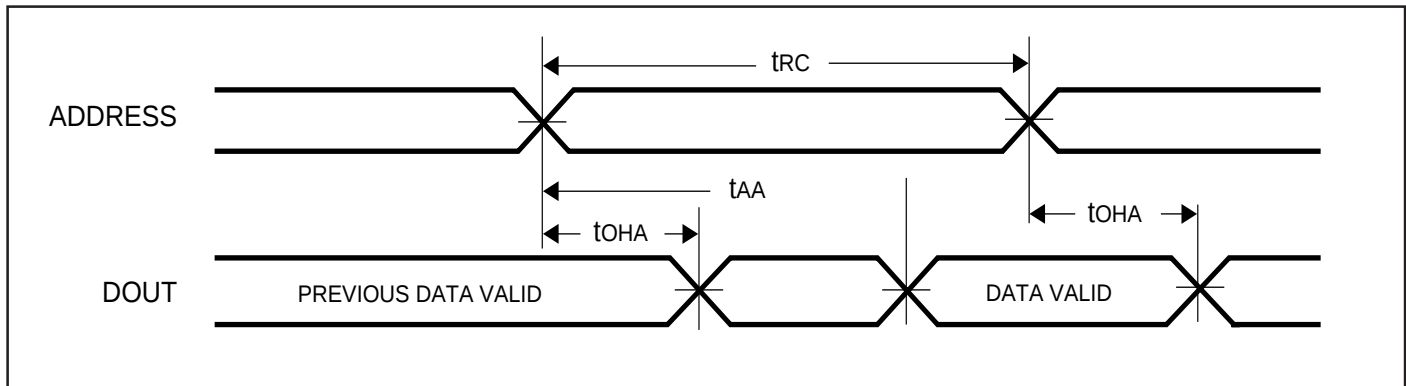
**Notes:**

1. See SRAM AC TEST CONDITIONS.
2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

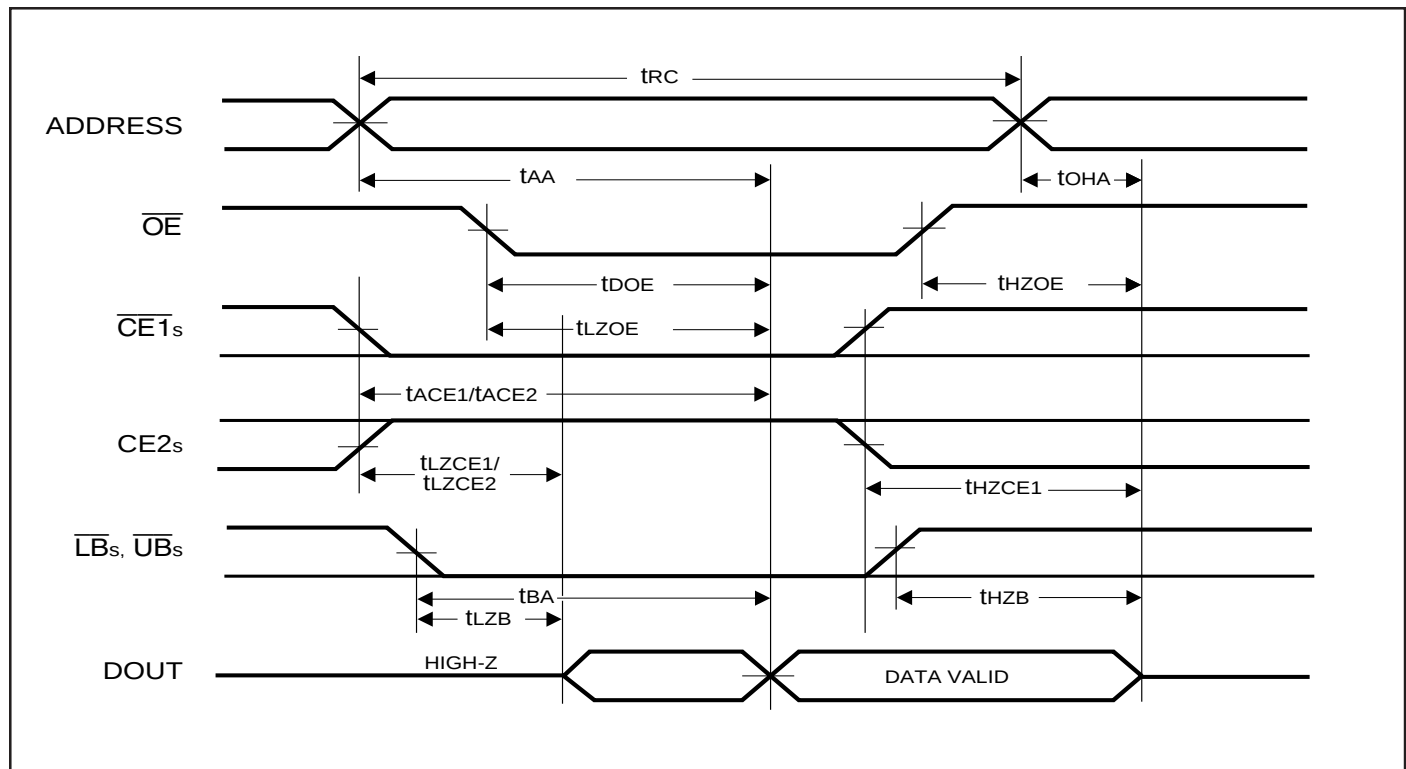
**SRAM AC TEST CONDITIONS**

| Parameter                                   | Unit                    |
|---------------------------------------------|-------------------------|
| Input Pulse Level                           | 0.4V to $V_{CC} - 0.3V$ |
| Input Rise and Fall Times                   | 5 ns                    |
| Input and Output Timing and Reference Level | 1.5V                    |
| Output Load                                 | 1 TTL gate and 30pF     |

## AC WAVEFORMS

SRAM READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) ( $\overline{CE1}_s = \overline{OE} = V_{IL}$ ,  $\overline{UB}_s$  or  $\overline{LB}_s = V_{IL}$ )

## AC WAVEFORMS

SRAM READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{CE1}_s$ ,  $\overline{OE}$ , AND  $\overline{UB}_s / \overline{LB}_s$  Controlled)

## Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE1}_s$ ,  $\overline{UB}_s$ , or  $\overline{LB}_s = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE1}_s$  LOW transition.

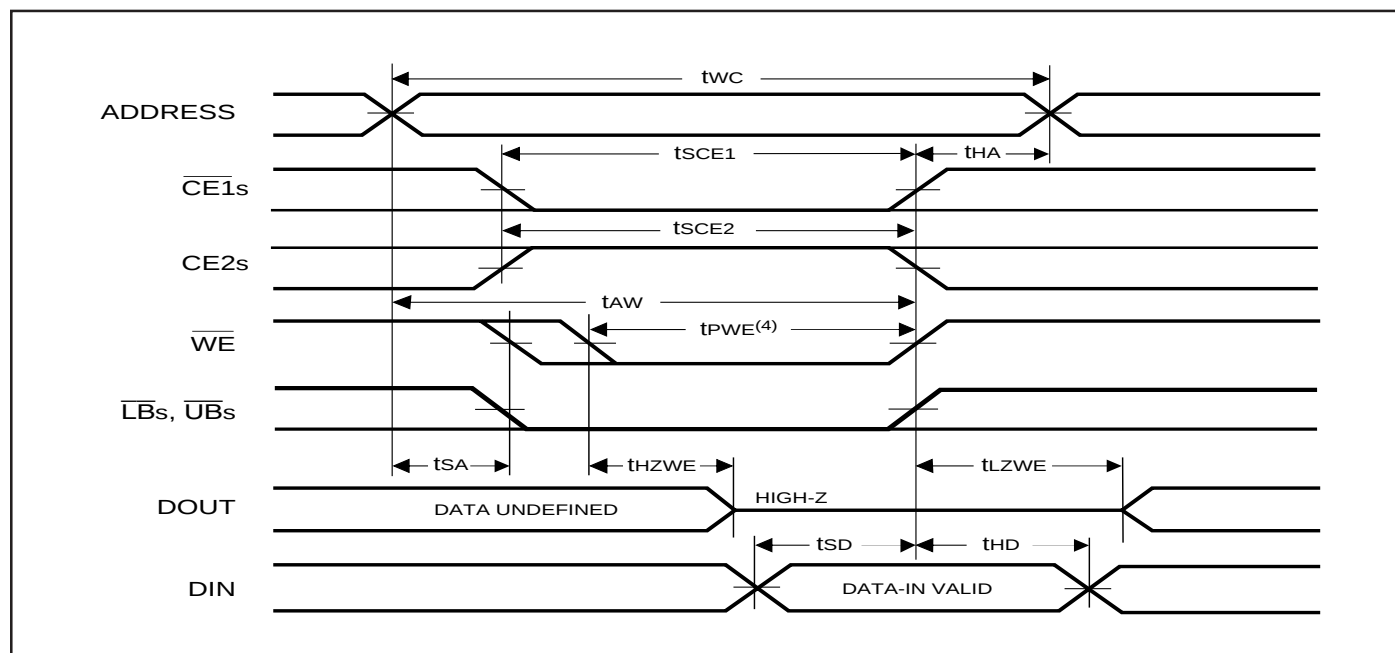
WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Symbol                           | Parameter                                                | 70 ns |      | Unit |
|----------------------------------|----------------------------------------------------------|-------|------|------|
|                                  |                                                          | Min.  | Max. |      |
| t <sub>wc</sub>                  | Write Cycle Time                                         | 70    | —    | ns   |
| t <sub>SCE1</sub>                | $\overline{CE1}_s$ to Write End                          | 60    | —    | ns   |
| t <sub>AW</sub>                  | Address Setup Time to Write End                          | 60    | —    | ns   |
| t <sub>HA</sub>                  | Address Hold from Write End                              | 0     | —    | ns   |
| t <sub>SA</sub>                  | Address Setup Time                                       | 0     | —    | ns   |
| t <sub>PWB</sub>                 | $\overline{LB}_s, \overline{UB}_s$ Valid to End of Write | 60    | —    | ns   |
| t <sub>PWE</sub>                 | $\overline{WE}$ Pulse Width                              | 50    | —    | ns   |
| t <sub>SD</sub>                  | Data Setup to Write End                                  | 30    | —    | ns   |
| t <sub>HD</sub>                  | Data Hold from Write End                                 | 0     | —    | ns   |
| t <sub>HZWE</sub> <sup>(2)</sup> | $\overline{WE}$ LOW to High-Z Output                     | —     | 20   | ns   |
| t <sub>LZWE</sub> <sup>(2)</sup> | $\overline{WE}$ HIGH to Low-Z Output                     | 5     | —    | ns   |

## Notes:

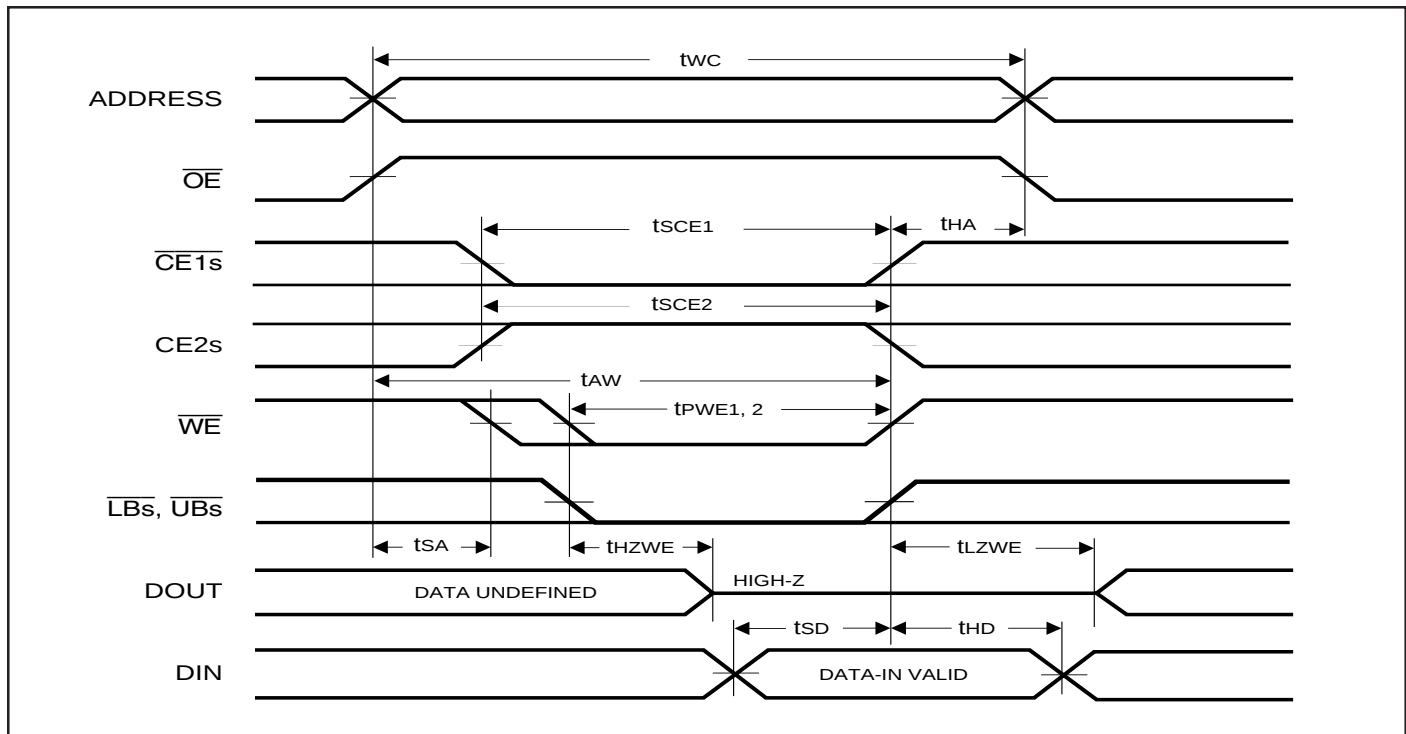
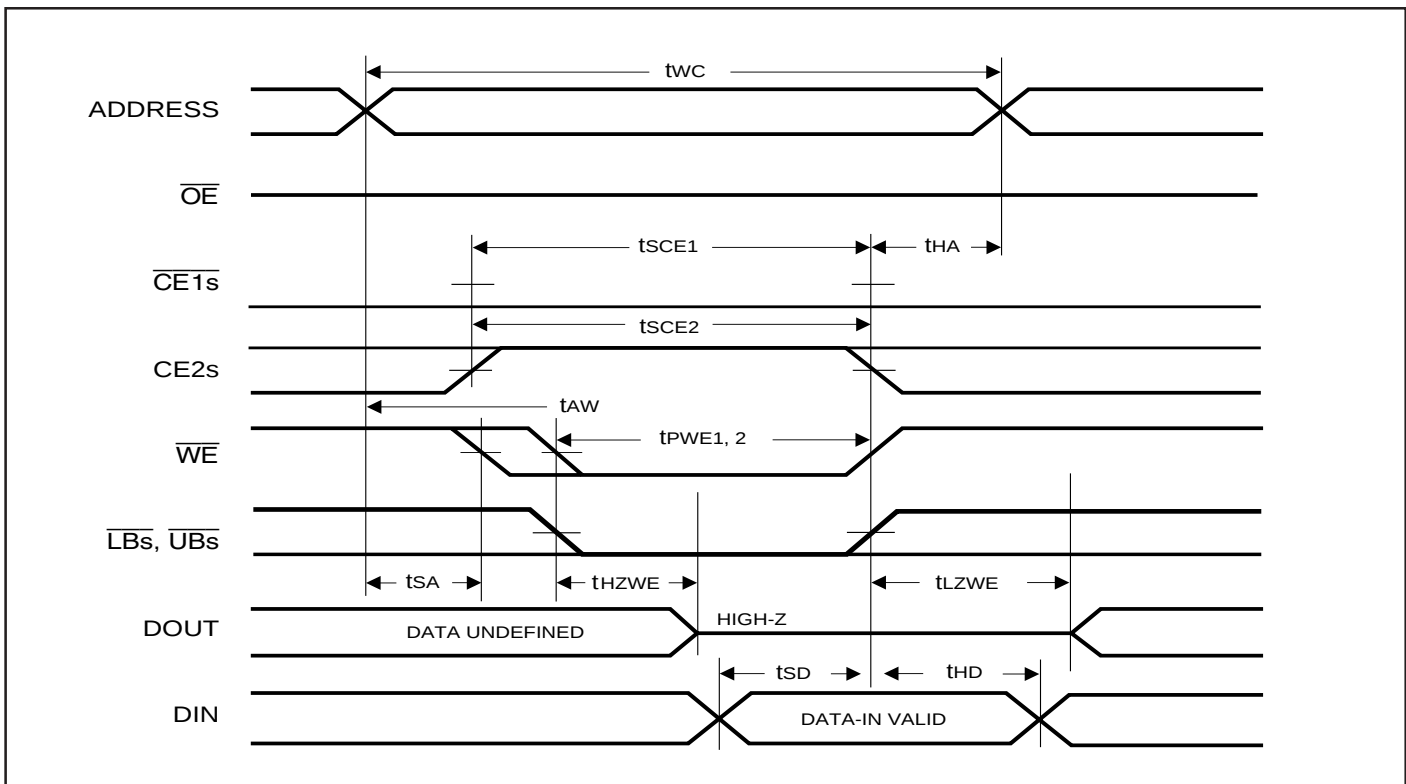
1. See SRAM AC TEST CONDITIONS.
2. Transition is measured  $\pm 500$  mV from steady-state voltage.

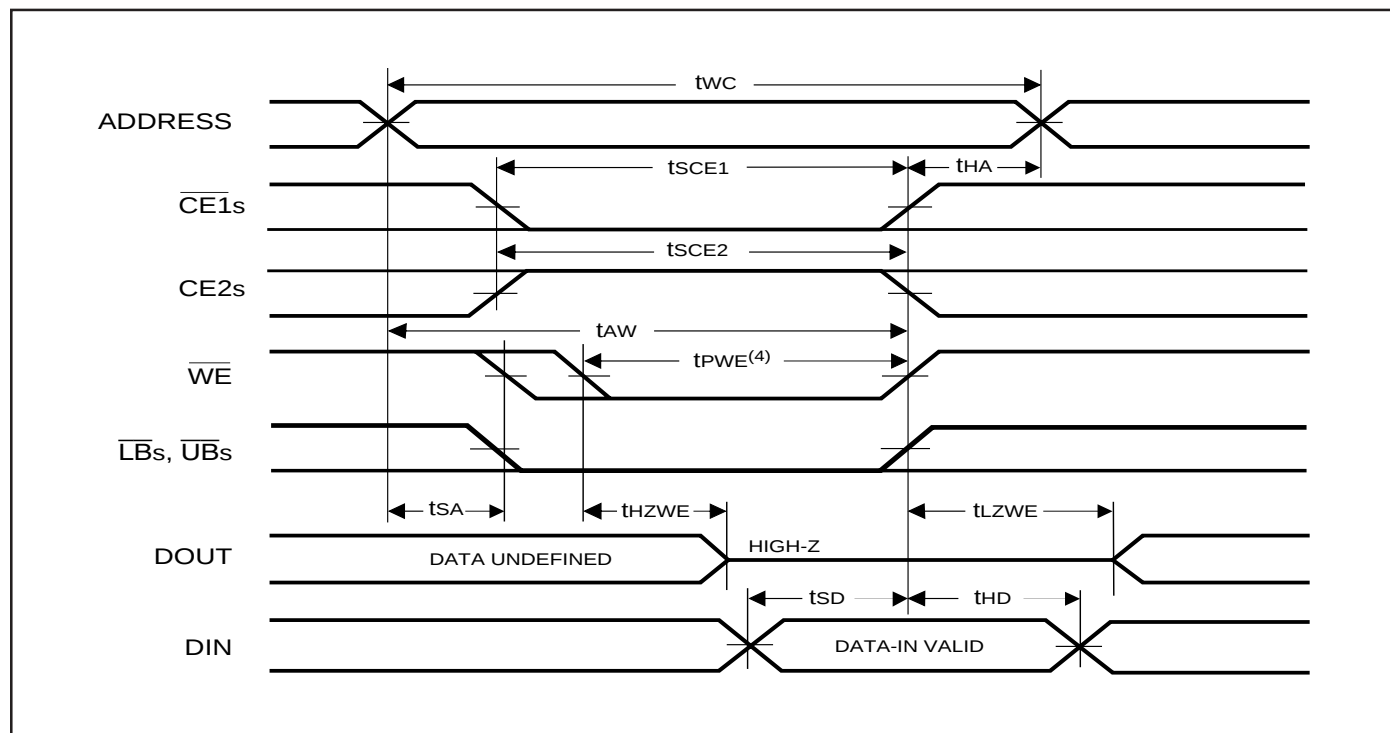
## AC WAVEFORMS

SRAM WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CE1}_s$  Controlled,  $\overline{OE}$  = HIGH or LOW)

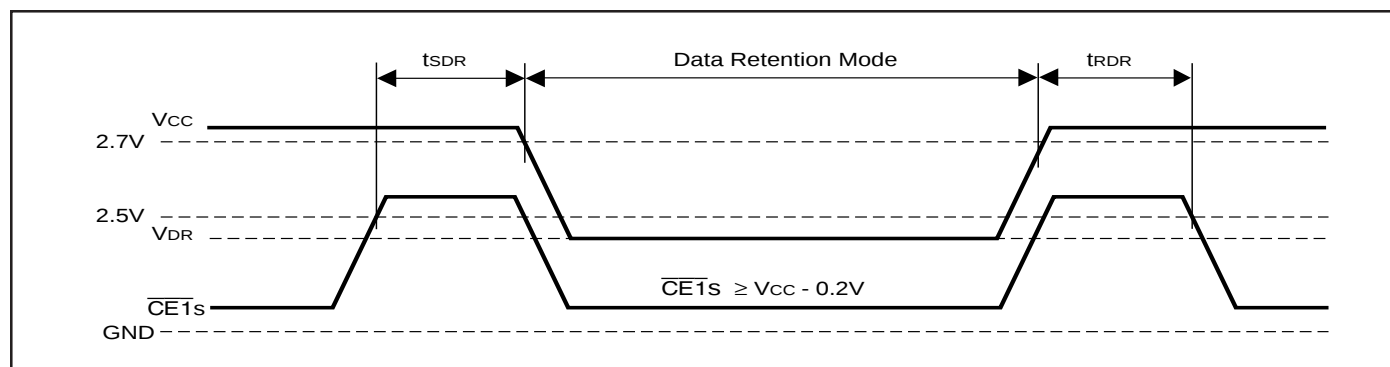
## Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{CE1}_s$  and  $\overline{WE}$  inputs and at least one of the  $\overline{LB}_s$  and  $\overline{UB}_s$  inputs being in the LOW state.
2.  $WRITE = (\overline{CE1}_s) [ (\overline{LB}_s) = (\overline{UB}_s) ] (\overline{WE})$ .

SRAM WRITE CYCLE NO. 2 ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)SRAM WRITE CYCLE NO. 3 ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)

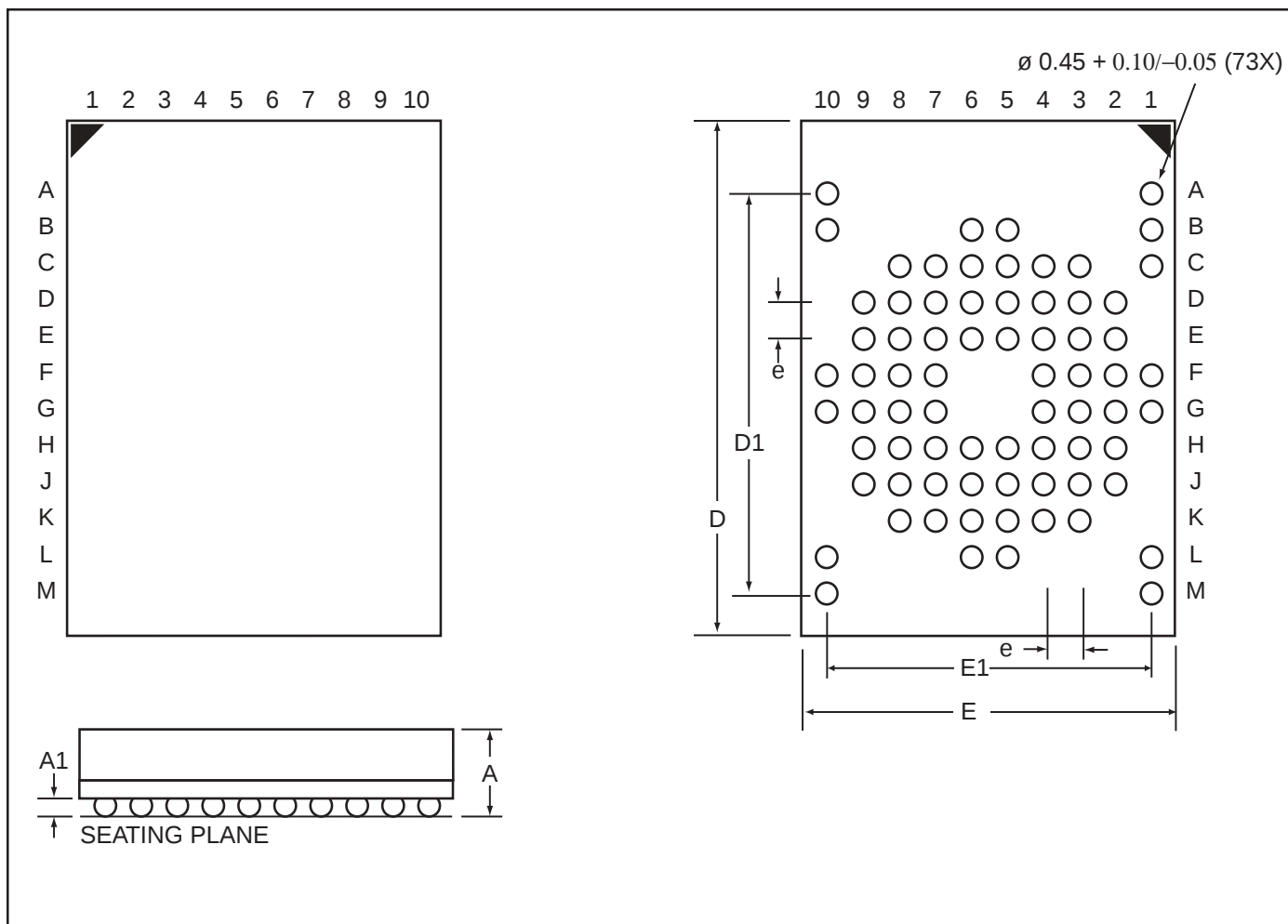
**WRITE CYCLE NO. 4** ( $\overline{UB}_s/\overline{LB}_s$  Controlled,  $\overline{CE1}_s$  is LOW,  $CE2_s$  is HIGH)**SRAM DATA RETENTION SWITCHING CHARACTERISTICS**

| Symbol    | Parameter                   | Test Condition                                        | Min.     | Max. | Unit    |
|-----------|-----------------------------|-------------------------------------------------------|----------|------|---------|
| $V_{DR}$  | $V_{CC}$ for Data Retention | See Data Retention Waveform                           | 1.0      | 3.3  | V       |
| $I_{DR}$  | Data Retention Current      | $V_{CC} = 1.0V$ , $\overline{CS1} \geq V_{CC} - 0.2V$ | —        | 15   | $\mu A$ |
| $t_{SDR}$ | Data Retention Setup Time   | See Data Retention Waveform                           | 0        | —    | ns      |
| $t_{RDR}$ | Recovery Time               | See Data Retention Waveform                           | $t_{rc}$ | —    | ns      |

**SRAM DATA RETENTION WAVEFORM** ( $\overline{CE1}$  Controlled)

## MINI BALL GRID ARRAY – 73-Ball BGA

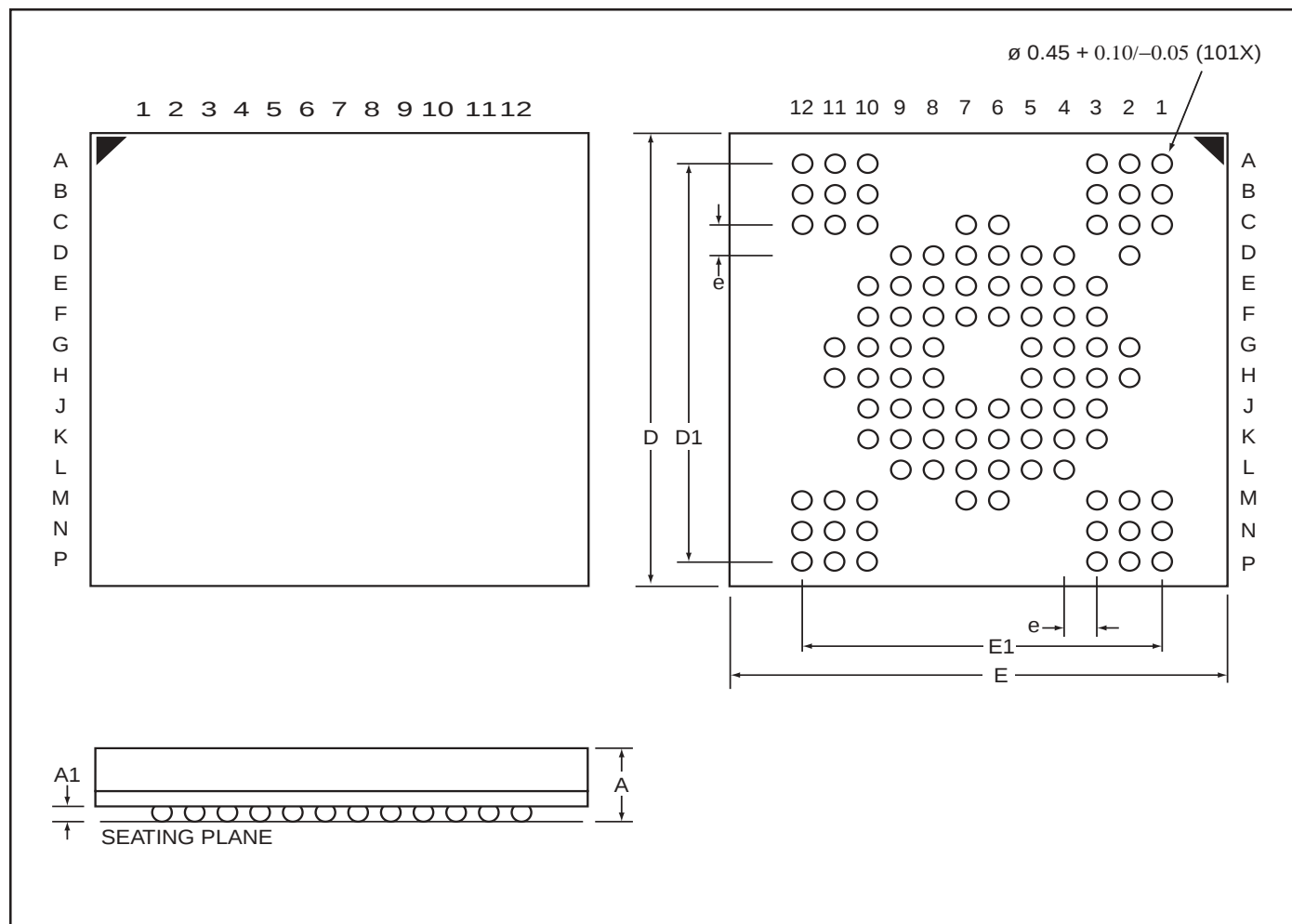
PACKAGE CODE: B (8.00 mm x 11.60 mm Body, 0.8 mm Ball Pitch)



| Symbol | Min.  | Typ.  | Max.  | Units |
|--------|-------|-------|-------|-------|
| A      | —     | —     | 1.40  | mm    |
| A1     | 0.28  | 0.38  | 0.48  | mm    |
| D      | 11.50 | 11.60 | 11.70 | mm    |
| D1     | —     | 8.80  | —     | mm    |
| E      | 7.90  | 8.00  | 8.10  | mm    |
| E1     | —     | 7.20  | —     | mm    |
| e      | —     | 0.80  | —     | mm    |

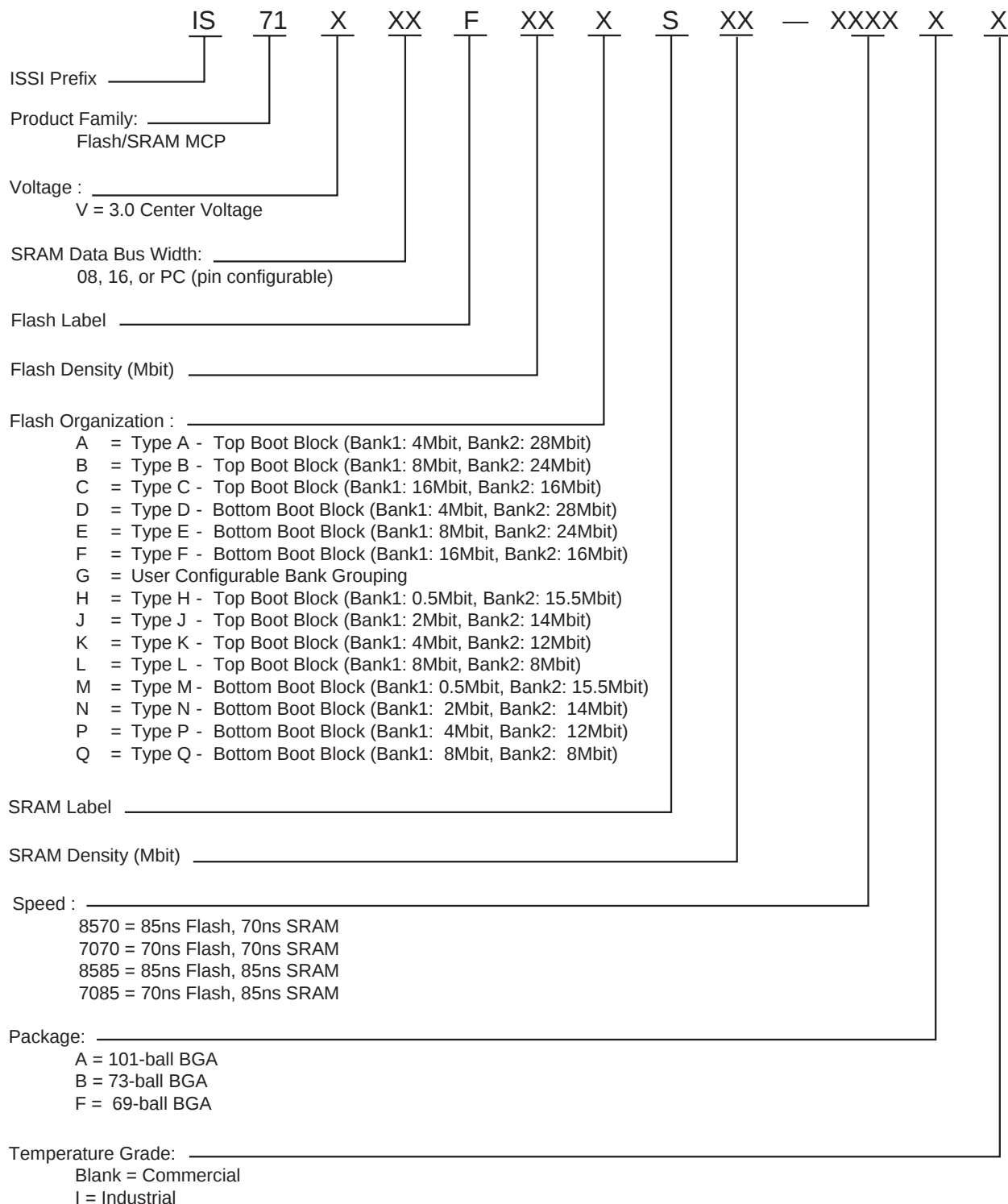
## MINI BALL GRID ARRAY – 101-Ball BGA (64 Mb Flash and 8 Mb SRAM)

PACKAGE CODE: A (11 mm x 12 mm Body, 0.8 mm Ball Pitch)



| Symbol | Min.  | Typ.  | Max.  | Units |
|--------|-------|-------|-------|-------|
| A      | —     | —     | 1.40  | mm    |
| A1     | 0.28  | 0.38  | 0.48  | mm    |
| D      | 11.90 | 12.00 | 12.10 | mm    |
| D1     | —     | 10.40 | —     | mm    |
| E      | 10.90 | 11.00 | 11.10 | mm    |
| E1     | —     | 8.80  | —     | mm    |
| e      | —     | 0.80  | —     | mm    |

## PART NUMBER LOGIC



**IS71V08F64GS08, IS71V16F64GS08****ORDERING INFORMATION****Industrial Range: -40°C to +85°C**

| <b>Order Part No.</b> | <b>SRAM<br/>Data Bus</b> | <b>Flash Bank<br/>Organization</b> | <b>Flash<br/>Speed(ns)</b> | <b>SRAM<br/>Speed(ns)</b> | <b>Package</b> |
|-----------------------|--------------------------|------------------------------------|----------------------------|---------------------------|----------------|
| IS71V08F64GS08-7070BI | 8                        | User Configurable                  | 70                         | 70                        | 73-ball BGA    |
| IS71V08F64GS08-7085BI | 8                        | User Configurable                  | 70                         | 85                        | 73-ball BGA    |
| IS71V08F64GS08-8570BI | 8                        | User Configurable                  | 85                         | 70                        | 73-ball BGA    |
| IS71V08F64GS08-8585BI | 8                        | User Configurable                  | 85                         | 85                        | 73-ball BGA    |
| IS71V16F64GS08-7070BI | 16                       | User Configurable                  | 70                         | 70                        | 73-ball BGA    |
| IS71V16F64GS08-7085BI | 16                       | User Configurable                  | 70                         | 85                        | 73-ball BGA    |
| IS71V16F64GS08-8570BI | 16                       | User Configurable                  | 85                         | 70                        | 73-ball BGA    |
| IS71V16F64GS08-8585BI | 16                       | User Configurable                  | 85                         | 85                        | 73-ball BGA    |
|                       |                          |                                    |                            |                           |                |
| IS71V08F64GS08-7070AI | 8                        | User Configurable                  | 70                         | 70                        | 101-ball BGA   |
| IS71V08F64GS08-7085AI | 8                        | User Configurable                  | 70                         | 85                        | 101-ball BGA   |
| IS71V08F64GS08-8570AI | 8                        | User Configurable                  | 85                         | 70                        | 101-ball BGA   |
| IS71V08F64GS08-8585AI | 8                        | User Configurable                  | 85                         | 85                        | 101-ball BGA   |
| IS71V16F64GS08-7070AI | 16                       | User Configurable                  | 70                         | 70                        | 101-ball BGA   |
| IS71V16F64GS08-7085AI | 16                       | User Configurable                  | 70                         | 85                        | 101-ball BGA   |
| IS71V16F64GS08-8570AI | 16                       | User Configurable                  | 85                         | 70                        | 101-ball BGA   |
| IS71V16F64GS08-8585AI | 16                       | User Configurable                  | 85                         | 85                        | 101-ball BGA   |