IS32WV16100A/B
IS32WV16200A/B

1M x 16 (16-MBIT) , 2M x16 (32-MBIT) PSEUDO STATIC RAM

ADVANCED INFORMATION
JANUARY 2003

FEATURES

- Access time: 70ns
- TTL compatible inputs and outsputs;tri-state I/O
- Wide Power supply voltage: 1.65V to 2.2V (A)
  2.2V to 3.6V (B)
- CMOS Standby 60µA (16-MBIT)
  70µA (32-MBIT)
- Deep Power Down Standby
  5µA (16-MBIT)
  5µA (32-MBIT)
- Deep Power-Down Mode: Data Invalid
- Page Operation Mode: Four Word Access
- Logic compatible with SRAM R/W ($\overline{WE}$) pin.
- Industrial Temperature Range: -40°C to 85°C
- Page 48 pin FBGA (6mm x 8mm)

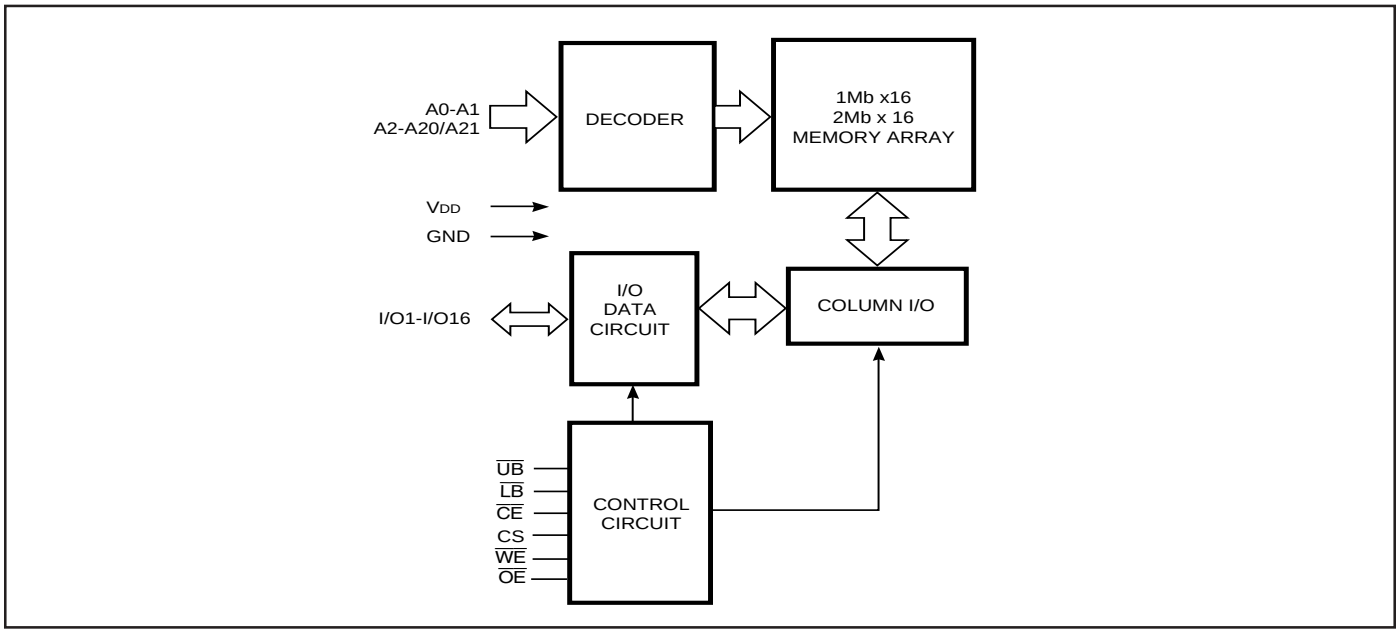
DESCRIPTION

The *ISSI* IS32WV16100A/B and IS32WV16200A/B are high-performance CMOS Pseudo Static RAM organized as a 1Meg x16, 2Meg x16, bits respectively.

ISSI CMOS technology provides high density, high speed low power devices that features SRAM-like write timing. Data is written to memory cells on the rising edge of the WE signal. With a page size of 4 words, the device has a page access operation. The device also supports deep power-down mode providing low-power standby.

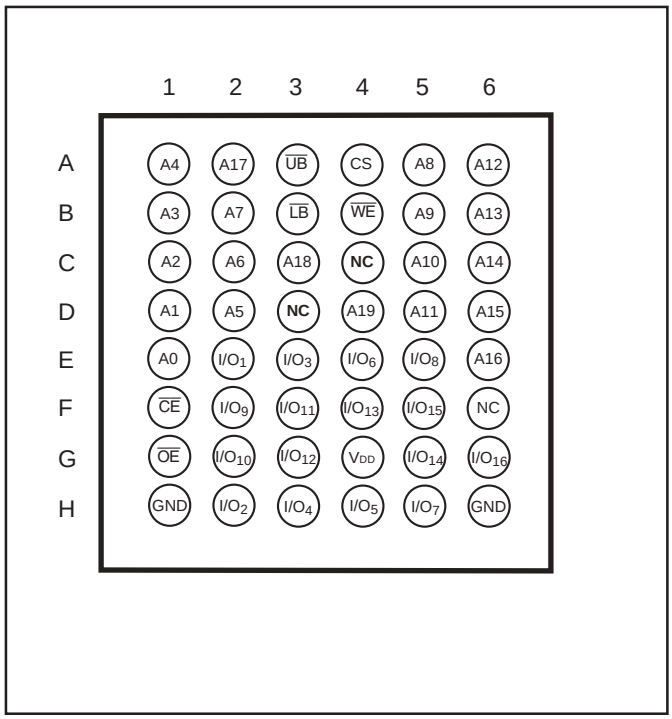
The IS32WV16100A/B and IS32WV16200A/B are packaged in a 48 pin FBGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM

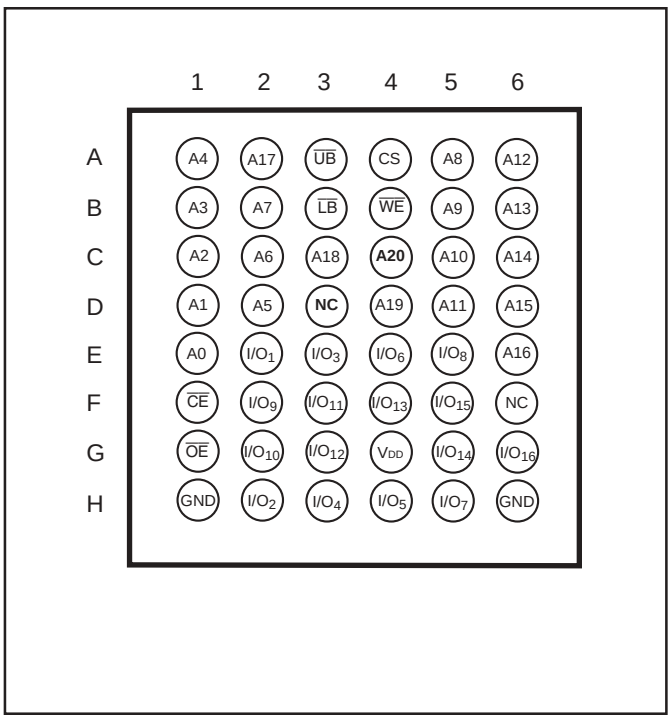


PIN CONFIGURATIONS

IS32WV16100A/B (48-pin BGA)



IS32WV16200A/B (48-pin BGA)



PIN DESCRIPTIONS

A0-A21	Address Inputs
A0-A1	Page Address Inputs
I/O1 to I/O16	Data Input/Outputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable Input
CS	Chip Select Input
$\overline{LB}$, $\overline{UB}$	Lower & Upper Data Byte Control Input
V_{DD}	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Function	$\overline{CE}$	CS	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	ADD	I/O1 to I/O8	I/O9 to I/O16	Power
Read: Word	L	H	L	H	L	L	XX	I/O_{OUT}	I/O_{OUT}	I_{CC1}
Read: Lower Byte	L	H	L	H	L	H	XX	I/O_{OUT}	HIGH-Z	I_{CC1}
Read: Upper Byte	L	H	L	H	H	L	XX	HIGH-Z	I/O_{OUT}	I_{CC1}
Write: Word	L	H	X	L	L	L	XX	D_{IN}	D_{IN}	I_{CC1}
Write: Lower	L	H	X	L	L	H	XX	D_{IN}	INVALID	I_{CC1}
Write: Upper	L	H	X	L	H	L	XX	INVALID	D_{IN}	I_{CC1}
Outputs Disabled	L	H	H	H	X	X	XX	HIGH-Z	HIGH-Z	I_{SB}
Standby	H	H	X	X	X	X	X	HIGH-Z	HIGH-Z	I_{SB}
Deep Power-Down Standby	H	L	X	X	X	X	X	HIGH-Z	HIGH-Z	I_{SB3}

L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, High-Z = High-impedence. XX = At $\overline{CE}$ falling edge, all addresses (A2 to A20) are valid "IN". Page address signals (A0 and A1) must be V_{IH} or V_{IL}, during entire cycle.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
V_T	Voltage on Any Pin Relative to GND	–0.2 to V_{DD}+3.6	V
V_{DD}	Supply Voltage	–0.2 to V_{DD}+3.6	V
I_{OUT}	Output Current	50	mA
P_D	Power Dissipation	0.6	W
T_A	Commercial Operation Temperature	0 to +70	°C
	Industrial Temperature	–40 to +85	°C
T_{STG}	Storage Temperature	–55 to +150	°C

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

IS32WV16100A/IS32WV16200A

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.65		2.2	V
V_{IH}	Input High Voltage	1.4	—	V_{DD} + 03	V
V_{IL}	Input Low Voltage	–0.2	—	0.4	V
V_{DH}	Data Retention Supply Voltage	1.5	—	2.0	V

IS32WV16100B/IS32WV16200B

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	2.2		3.6	V
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 03	V
V_{IL}	Input Low Voltage	–0.2	—	0.4	V
V_{DH}	Data Retention Supply Voltage	2.0	—	3.0	V

ELECTRICAL CHARACTERISTICS[1]

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Cond.	Min.	Max.	Unit
I_{IL}	Input Leakage Current	Any input 0V ≤ V_{IN} ≤ V_{DD} Other inputs not under test = 0V		–1.0	1.0	µA
I_{IO}	Output Leakage Current	Output is disabled (Hi-Z) 0V ≤ V_{OUT} ≤ V_{DD}		–1.0	1.0	µA
V_{OH}	Output High Voltage Level	I_{OH} = –0.5 mA		1.4	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = 1.0 mA		—	0.2	V
$I_{CC}1$	Operating Current	$\overline{CS}$ =V_{IH}, I_{OUT} = 0mA $\overline{CE}$ Cycling, t_{RC} = t_{RC} (min.)	32WV16100A/B 32WV16200A/B	— —	20 30	mA mA
$I_{CC}2$	Page Access Operating Currentt	$\overline{CE}$=V_{IL}, CS=V_{IH}, I_{OUT} = 0mA Page Add.Cycling, t_{PC} (min.) t_{PC} >1µA	32WV16100A/B 32WV16200A/B	— —	40 5	mA mA
$I_{SB}1$	Standby Current: TTL Commerical Temp	$\overline{CE}$=V_{IH}, CS=V_{IH}	32WV16100A/B 32WV16200A/B	— —	1.5 3	mA mA
	Industrial Temp	$\overline{CE}$=V_{IH}, CS= V_{IH}	32WV16100A/B 32WV16200A/B	— —	3 6	mA mA
$I_{SB}2$	Standby Current: CMOS Commercial Temp	$\overline{CE}$=Vss-0.2V, CS=V_{DD}-0.2V	32WV16100A/B 32WV16200A/B	— —	60 70	µA µA
	Industrial Temp	$\overline{CE}$=Vss-0.2V, CS=V_{DD}-0.2V	32WV16100A/B 32WV16200A/B	— —	70 90	µA µA
$I_{SB}3$	Standby Current: Deep Power-down Commercial Temp	$\overline{CS}$=0.2V	32WV16100A/B 32WV16200A/B	— —	5 5	µA µA
	Industrial Temp	$\overline{CS}$=0.2V	32WV16100A/B 32WV16200A/B	— —	10 10	µA µA

CAPACITANCE[1,2]

Symbol	Parameter	Max.	Unit
$C_{IN}1$	Input Capacitance: A0-A21	10	pF
$C_{IN}2$	Input Capacitance: $\overline{CE}$, CS, $\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$	10	pF
C_{IO}	Data Input/Output Capacitance: I/O0-I/O16	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Random Read or Write Cycle Time	100	—	ns
t_{CE}	$\overline{CE}$ Pulse Width	80	10K	ns
t_{P}	Pre-charge Time	20	—	ns
t_{CEA}	$\overline{CE}$ Access Time	—	70	ns
t_{OEA}	$\overline{OE}$ Access Time	—	70	ns
t_{OEP}	$\overline{OE}$ Pulse Width	70	10K	ns
t_{BEA}	$\overline{LB}$,$\overline{UB}$ AccessTime	—	25	ns
t_{APH}	Address (A0 and A1) Hold Time	70	—	ns
t_{ASC}	Address Setup Time	-25	—	ns
t_{AHC}	Address Hold Time	45	—	ns
t_{ASO}, t_{ASW}	Address Setup Time	0	—	ns
t_{AHO}, t_{AHW}	Address Hold Time	45	—	ns
t_{WHC}	$\overline{WE}$ Hold Time	8	—	ns
t_{RCS}	Read Command Setup Time	8	—	ns
t_{WOS}	Write Command Setup Time	18	—	ns
t_{RCH}	Read Command Hold Time	8	—	ns
t_{WP}	$\overline{WE}$ Pulse Width	70	10K	ns
t_{WCH}	$\overline{CE}$ to End of Write	55	—	ns
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	70	—	ns
t_{WBH}	$\overline{LB}$,$\overline{UB}$ to End of Write	45	—	ns
t_{BWL}	Write Command to $\overline{LB}$, $\overline{UB}$ Lead time	50	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DSW}	Data Set-up Time from $\overline{WE}$	25	—	ns
t_{DSC}	Data Set-up Time from $\overline{CE}$	25	—	ns
t_{DSB}	Data Set-up Time from $\overline{LB}$, $\overline{UB}$	25	—	ns
t_{DHW}	Data Hold Time from $\overline{WE}$	0	—	ns
t_{DHC}	Data Hold Time from $\overline{CE}$	0	—	ns
t_{DHB}	Data HoldTime from $\overline{LB}$, $\overline{UB}$	0	—	ns

Continued

AC CHARACTERISTICS Continued

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Min.	Max.	Units
t_{CLZ}	$\overline{CE}$ Low to Output Active	10	—	ns
t_{OLZ}	$\overline{OE}$ Low to Output Active	0	—	ns
t_{BLZ}	$\overline{LB}$, $\overline{UB}$ Low to Output Active	0	—	ns
t_{WLZ}	$\overline{WE}$ Low to Output Active	0	—	ns
t_{CHZ}	$\overline{CE}$ High to Output High-Z	—	20	ns
t_{OHZ}	$\overline{OE}$ High to Output High-Z	—	20	ns
t_{BHZ}	$\overline{LB}$, $\overline{UB}$ High to Output High-Z	—	20	ns
t_{WHZ}	$\overline{OE}$ High to Output High-Z	—	20	ns
t_{PC}	Page Mode Cycle Time	22	—	ns
t_{AA}	Page Mode Address Access Time	—	25	ns
t_{AOH}	Page Mode Output Data Hold Time	5(1)	—	ns
t_{CS}	$\overline{CS}$ Set-up Time	0	—	ns
t_{CH}	$\overline{CS}$ Hold Time	200	—	ns
t_{DPD}	$\overline{CS}$ Pulse Width (Deep Power Down)	10	—	ns

AC Notes:

1. Guarantee minimum 10ns of datavalid time under any specific operting condition.
2. After power-up, an initial pause of 200 us with CS high is required with the output open condition.
3. Parameters tCHZ, tOHZ, tBHZ and TWHZ define the time at which the output goes the into the open condition and are not output voltage reference levels.
4. During write cycles, input data is latched on the earliest of $\overline{WE}$, $\overline{LB/UB}$, or $\overline{CE}$ rising edge. Therefore, input data must be valid during the set-up time (tDSC, tDSB or tDSW) and hold time (tDHC, tDHB or tDHW).
5. Address (A2 to A20) inputs are latched on the falling edge of $\overline{OE}$ or $\overline{WE}$. Address (A2 to A20) input must be valide during the set-up time (tASO or tASW) and hold time (tAHO or tAHW).
6. Data can not be retained at deep power-down stand-by mode.
7. If $\overline{OE}$ is high during the write cycle, the outputs will remain at high impedance.
8. During the output state of I/O signals, input signals of reverse polarity must not be applied.
9. $t_{rising} = t_{falling} = 5ns$ for inputs.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	V_{DD}-0.2V to V_{DD}+0.2V
Input Rise and Fall Time	5 ns
Input and Output Timing and Reference Level	V_{REF}
Output Load	See Figures 1 and 2 (1)

Note 1. All AC test to output Load Fgiure 1, excpt High-Z use output load Figure 2.

	1.65V to 2.2V	2.2V to 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

AC TEST LOADS

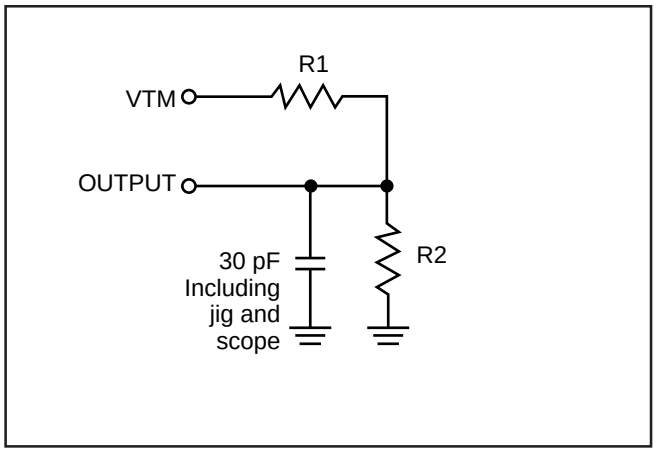


Figure 1

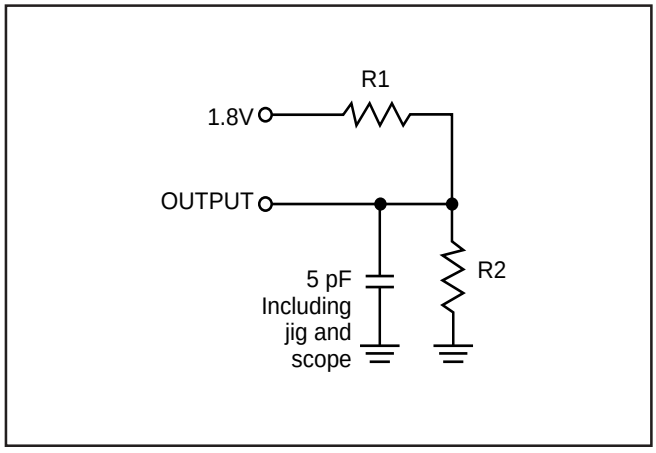
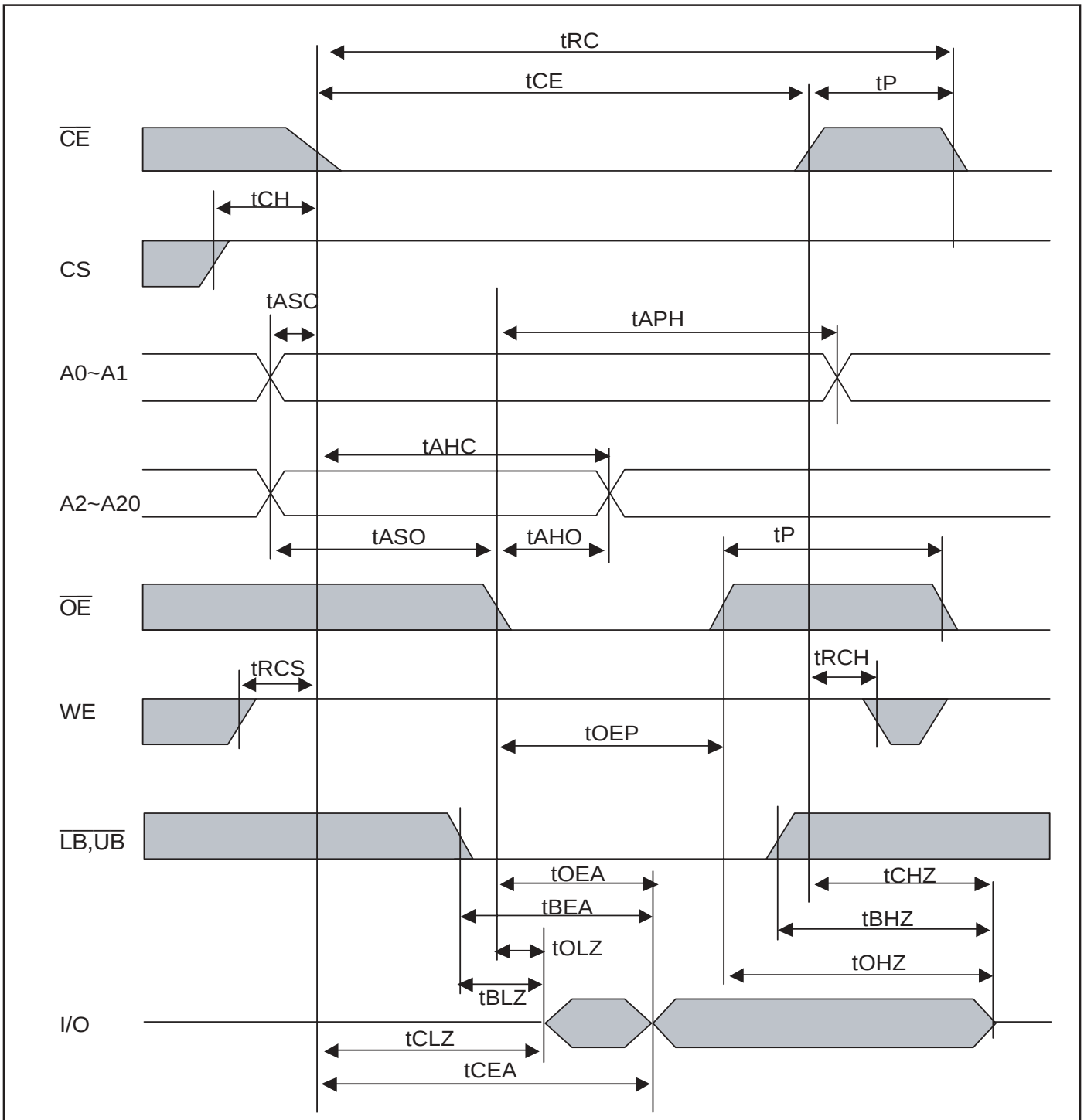


Figure 2

AC WAVEFORMS

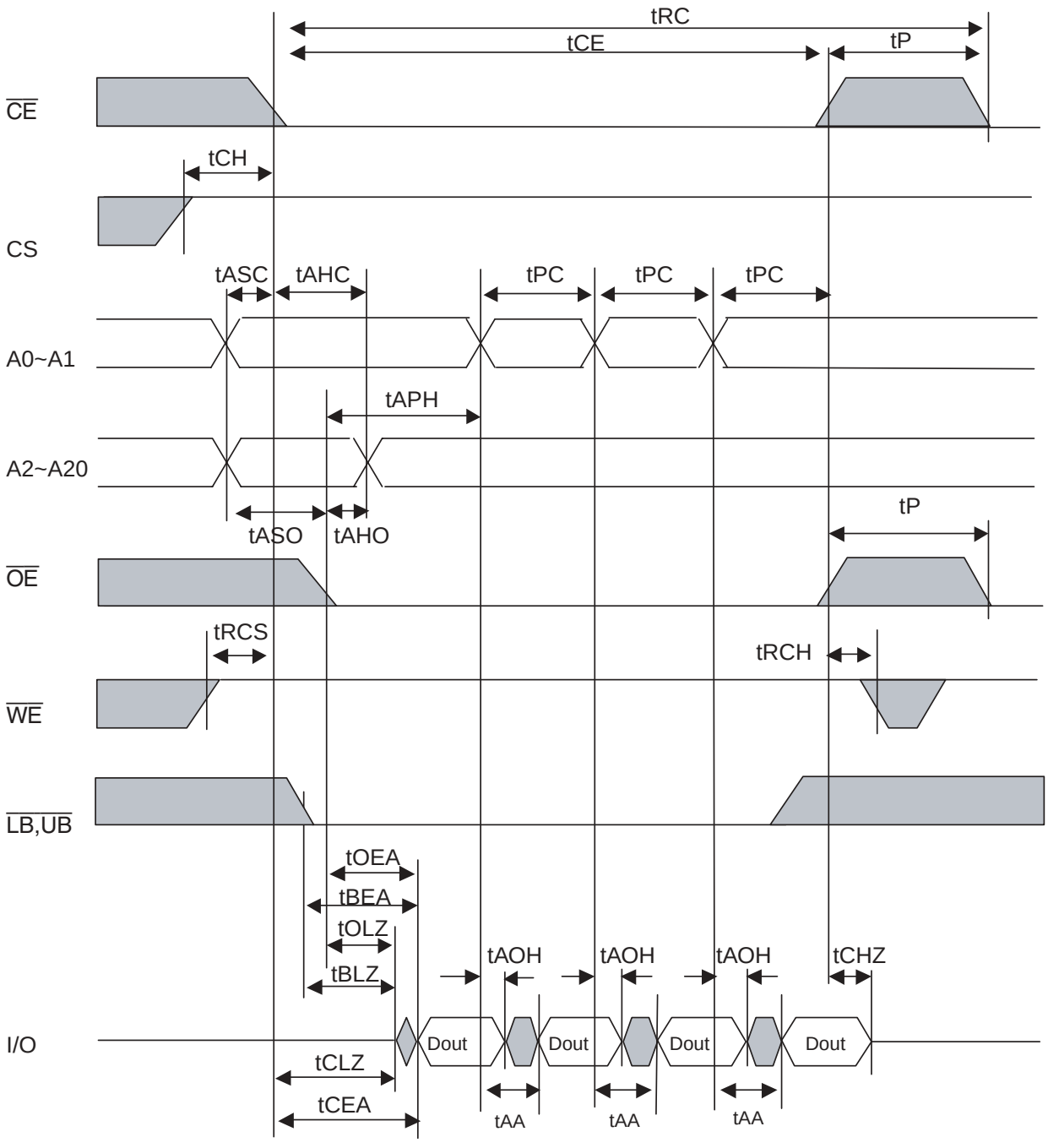
Read Timing



For shaded areas either $\overline{OE}$ or $\overline{CE}$ = High.

AC WAVEFORMS

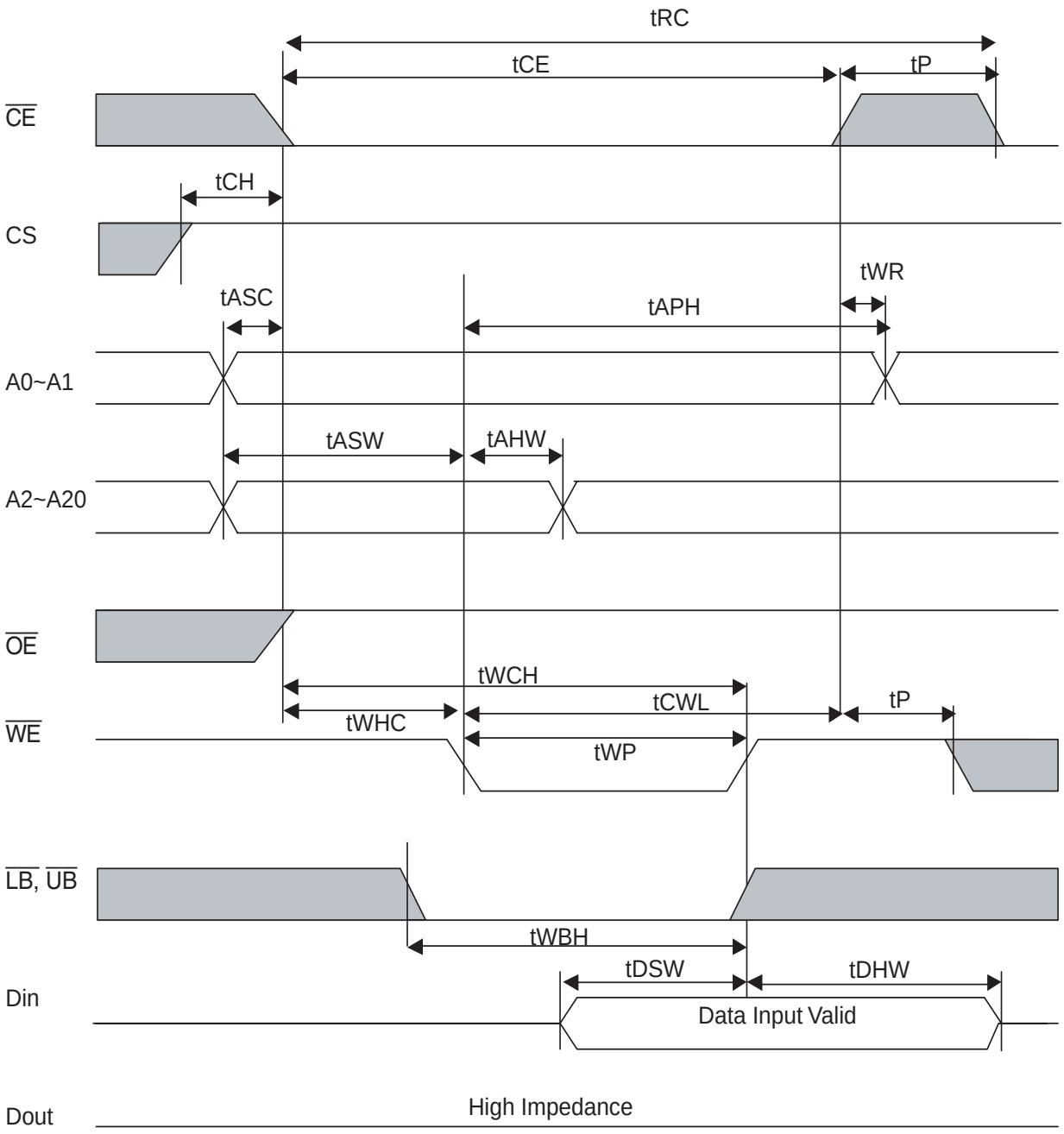
Page Read timing (four word access)



For shaded areas either $\overline{OE}$ or $\overline{CE}$ = High.

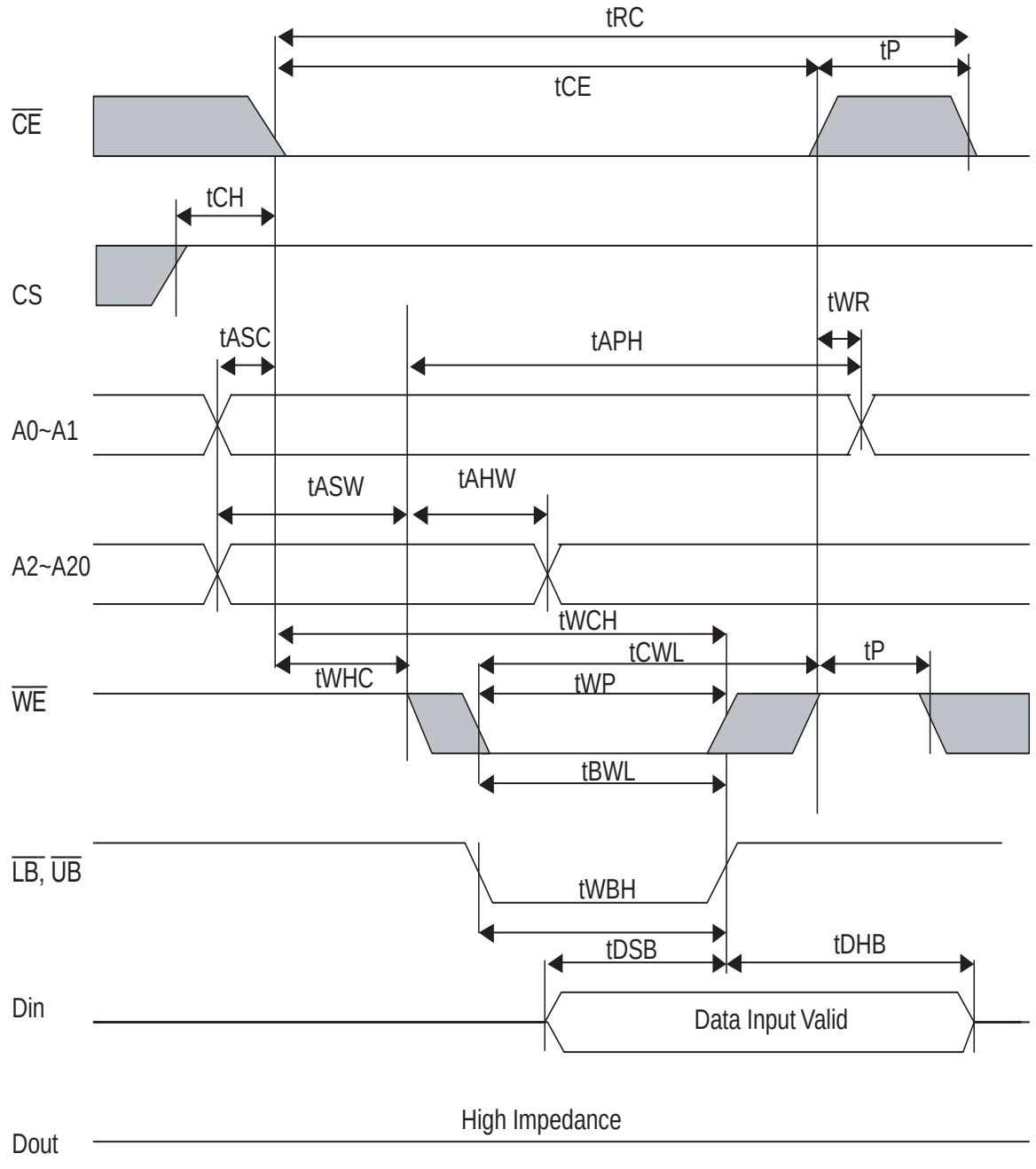
AC WAVEFORMS

Write Timing ($\overline{WE}$ Control Write)



AC Wave Forms

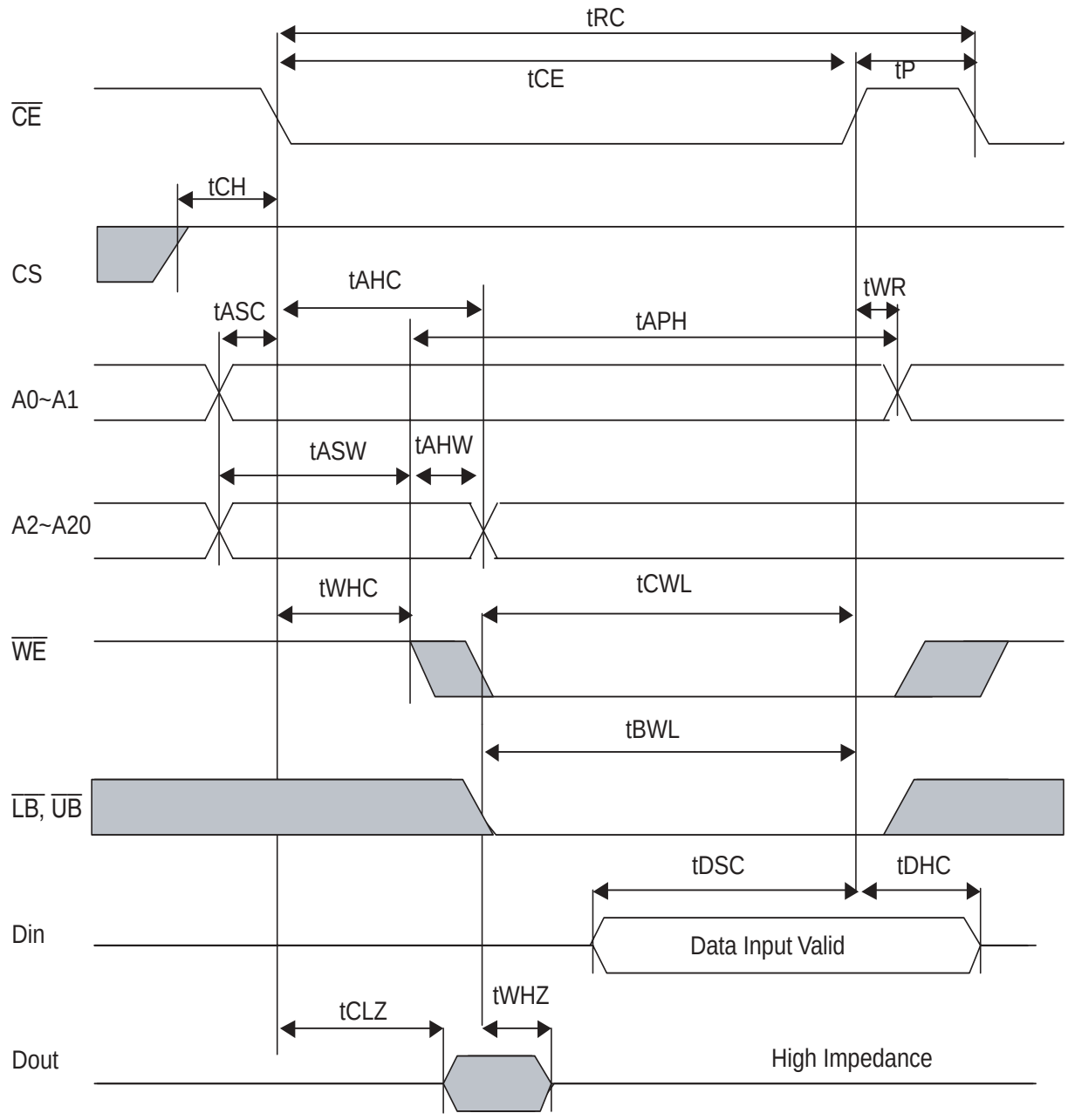
Write Timing ($\overline{LB}$/$\overline{UB}$ Control Write)



$\overline{CE}$ = High.

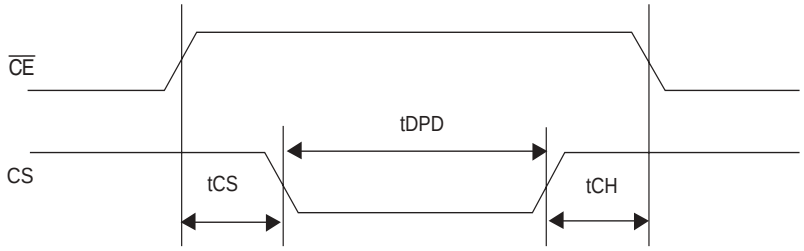
AC Wave Forms

Write Timing ($\overline{CE}$ Control Write)



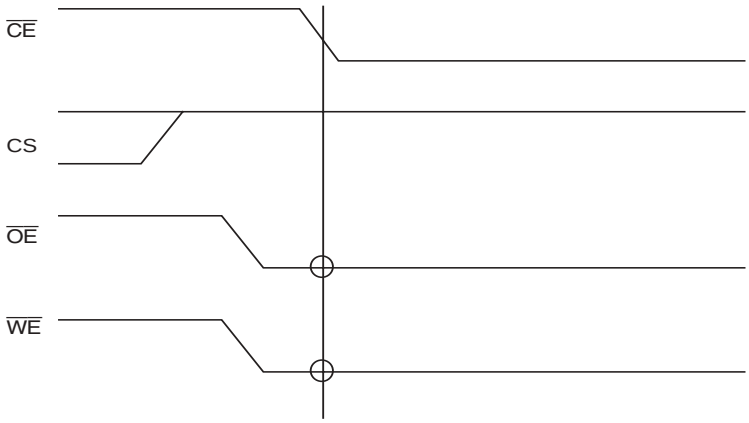
$\overline{OE}$ = High.

Deep Power-Down Timing



Note: During deep power-down stand-by mode, data can not be retained.

Prohibition Timing (Timing shown is prohibited.)



Note: A malfunction may occur, since devices go into test modes for internal use, if both $\overline{OE}$ and $\overline{WE}$ go Low coincident with or before falling edge of CE.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS31WV16100A-70M	Mini BGA (6mm x8mm)
	IS31WV16100B-70M	Mini BGA (6mm x8mm)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS31WV16100A-70MI	Mini BGA (6mm x 8mm)
	IS31WV16100B-70MI	Mini BGA (6mm x 8mm)

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS31WV16200A-70M	Mini BGA (6mm x 8mm)
	IS31WV16200B-70M	Mini BGA (6mm x 8mm)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS31WV16200A-70MI	Mini BGA (6mm x 8mm)
	IS31WV16200B-70MI	Mini BGA (6mm x 8mm)