128K x 8 HIGH-SPEED CMOS STATIC RAM

ADVANCED INFORMATION
JANUARY 2003

FEATURES

- High-speed access time: 15 ns
- Low active and standby power
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V (±10%) power supply
- Temperature offerings:
  Option A1: -40°C to +85°C
  Option A2: -40°C to +105°C
  Option A3: -40°C to +125°C

DESCRIPTION

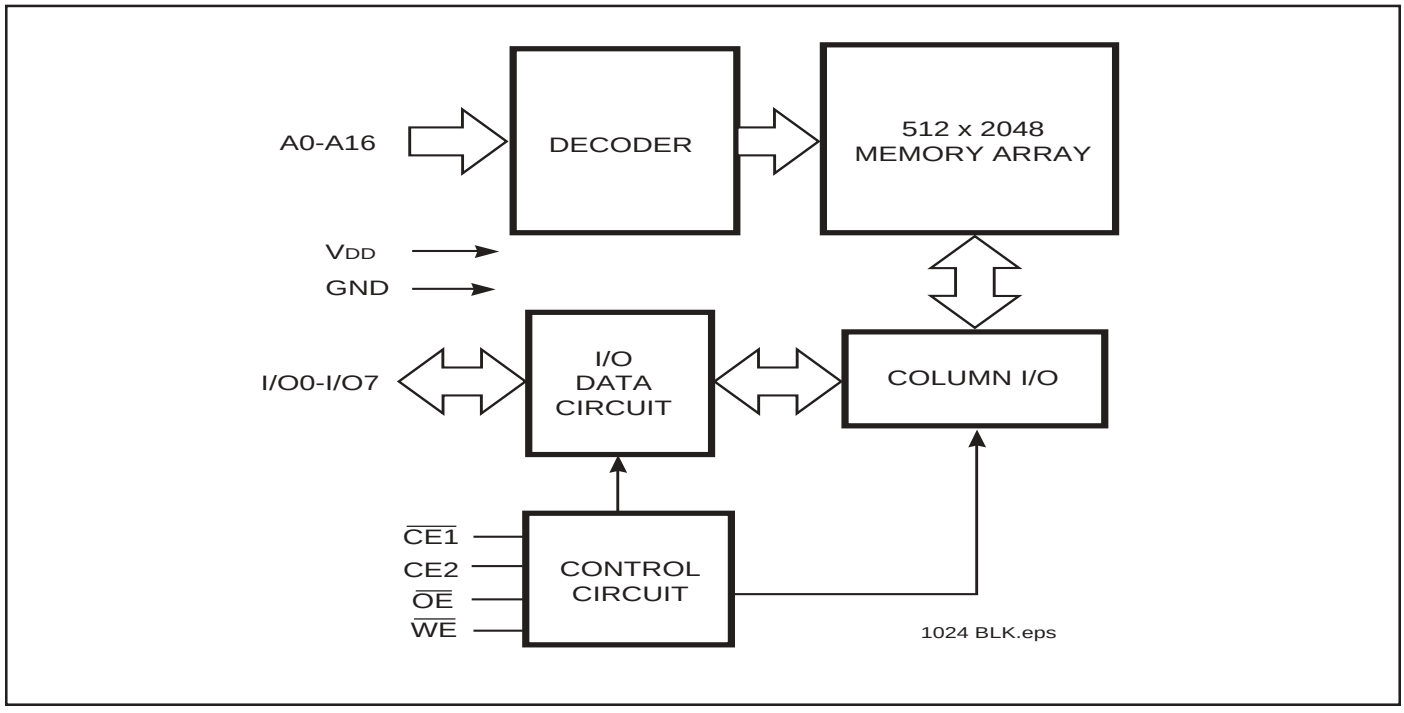
The *ISSI* IS64C1024L is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAMs. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

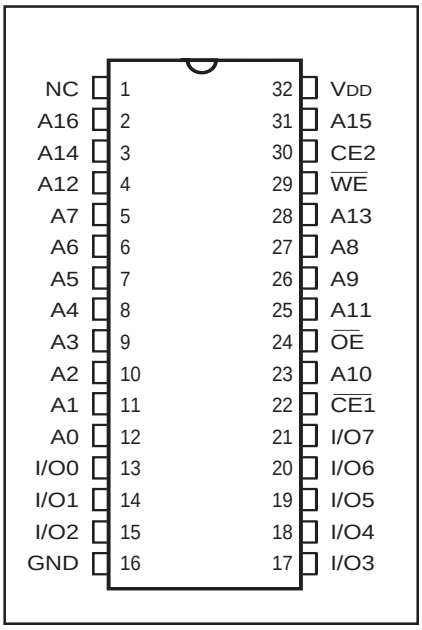
Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS64C1024L is available in the following 32-pin packages: 300-mil and 400-mil SOJ, and TSOP (Type I, 8x20).

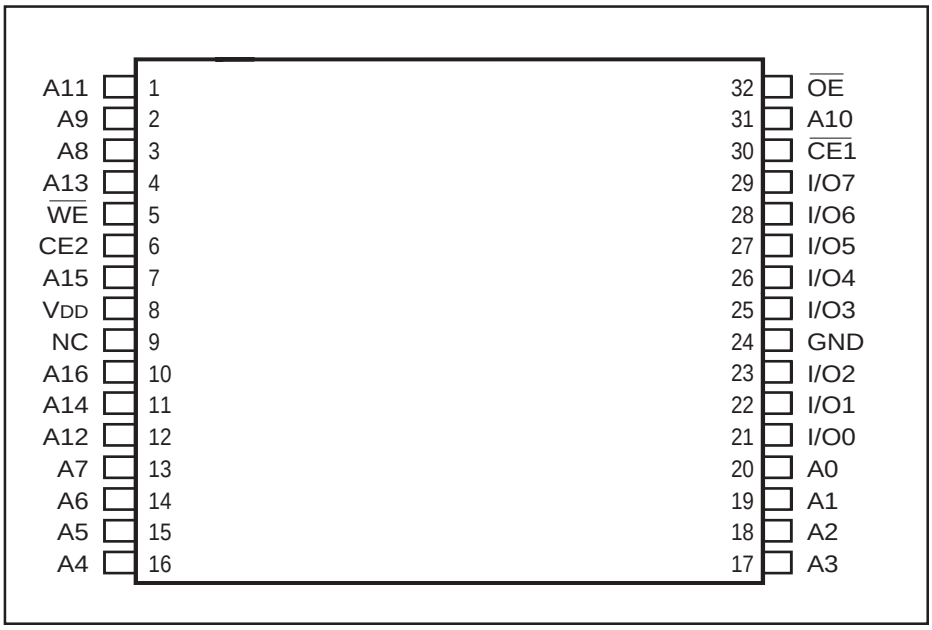
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
32-Pin SOJ



PIN CONFIGURATION
32-Pin TSOP (Type 1) (T)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	H	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	H	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Options	Ambient Temperature	IS64C1024L
A1	–40°C to +85°C	4.5V - 5.5V
A2	–40°C to +105°C	4.5V - 5.5V
A3	–40°C to +125°C	4.5V - 5.5V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	— –5	— 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD} Outputs Disabled	— –5	— 5	µA

Note:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	Options	-15 ns Min.	-15 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ I_{OUT} = 0 mA, f = 0	A1 A2 A3	— — —	90 95 100	mA
I_{CC2}	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ I_{OUT} = 0 mA, f = f_{MAX}	A1 A2 A3	— — —	150 155 160	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	$V_{DD} = V_{DD\ MAX}$, $V_{IN} = V_{IH}$ or V_{IL} $\overline{CE1} \geq V_{IH}$, f = 0 or CE2 $\leq V_{IL}$, f = 0	A1 A2 A3	— — —	30 40 45	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE1} \leq V_{DD} - 0.2V$, CE2 $\leq$ 0.2V $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq$ 0.2V, f = 0	A1 A2 A3	— — —	1.0 2 3	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

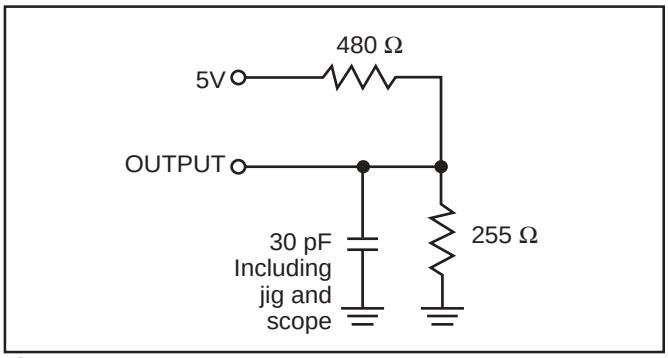


Figure 1

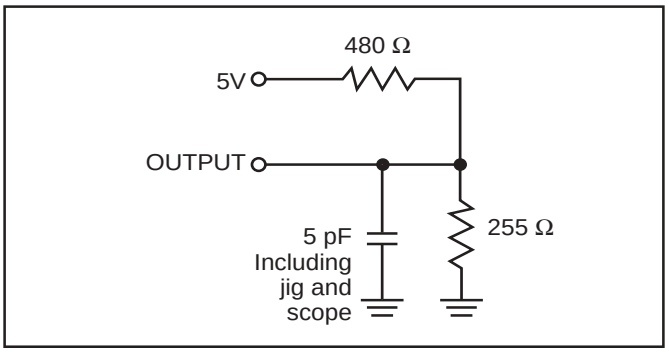


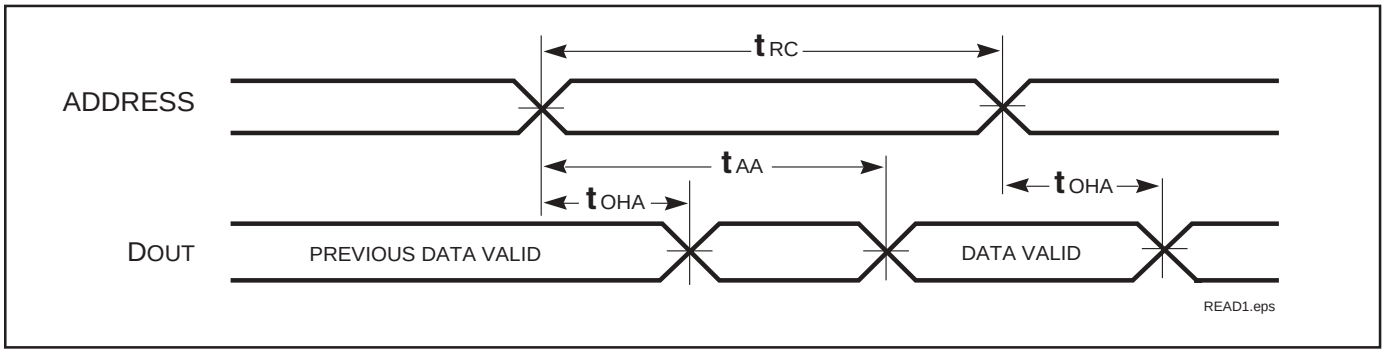
Figure 2

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

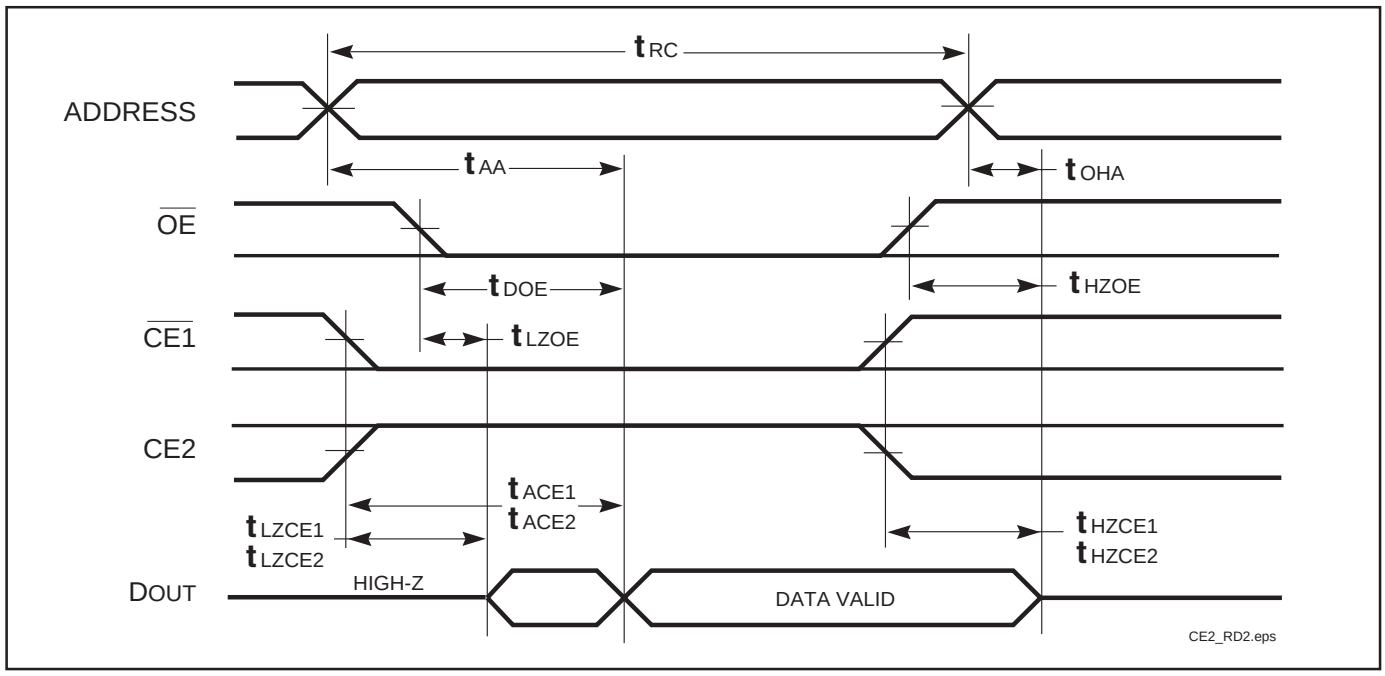
		-15 ns		
Symbol	Parameter	Min.	Max.	Unit
t_{RC}	Read Cycle Time	15	—	ns
t_{AA}	Address Access Time	—	15	ns
t_{OHA}	Output Hold Time	2	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	15	ns
t_{ACE2}	CE2 Access Time	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	7	ns
t_{LZOE}[3]	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZOE}[3]	$\overline{OE}$ to High-Z Output	0	6	ns
t_{LZCE1}[3]	$\overline{CE1}$ to Low-Z Output	2	—	ns
t_{LZCE2}[3]	CE2 to Low-Z Output	2	—	ns
t_{HZCE}[3]	$\overline{CE1}$ or CE2 to High-Z Output	0	8	ns
t_{PU}[4]	$\overline{CE1}$ or CE2 to Power-Up	0	—	ns
t_{PD}[4]	$\overline{CE1}$ or CE2 to Power-Down	—	12	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS
READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range, Standard and Low Power)

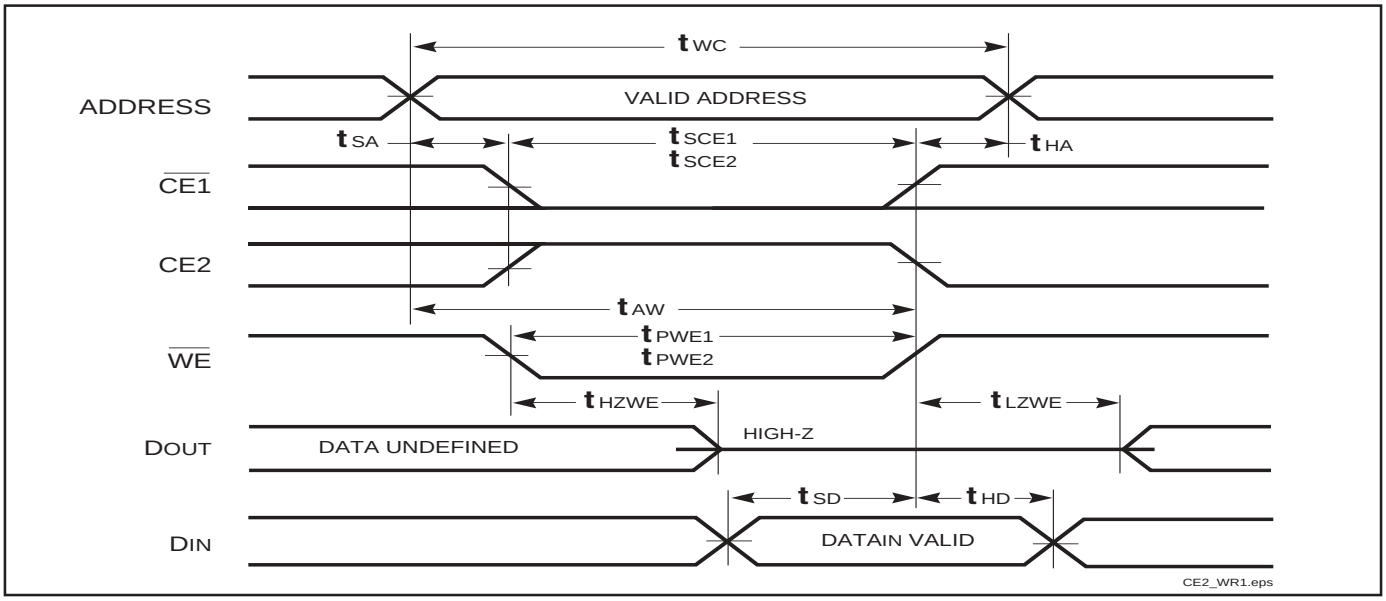
Symbol	Parameter	-15 ns Min.	Max.	Unit
t_{WC}	Write Cycle Time	15	—	ns
t_{SCE1}	$\overline{CE1}$ to Write End	12	—	ns
t_{SCE2}	CE2 to Write End	12	—	ns
t_{AW}	Address Setup Time to Write End	12	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	12	—	ns
t_{SD}	Data Setup to Write End	10	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[5]	$\overline{WE}$ LOW to High-Z Output	—	7	ns
t_{LZWE}[5]	$\overline{WE}$ HIGH to Low-Z Output	2	—	ns

Notes:

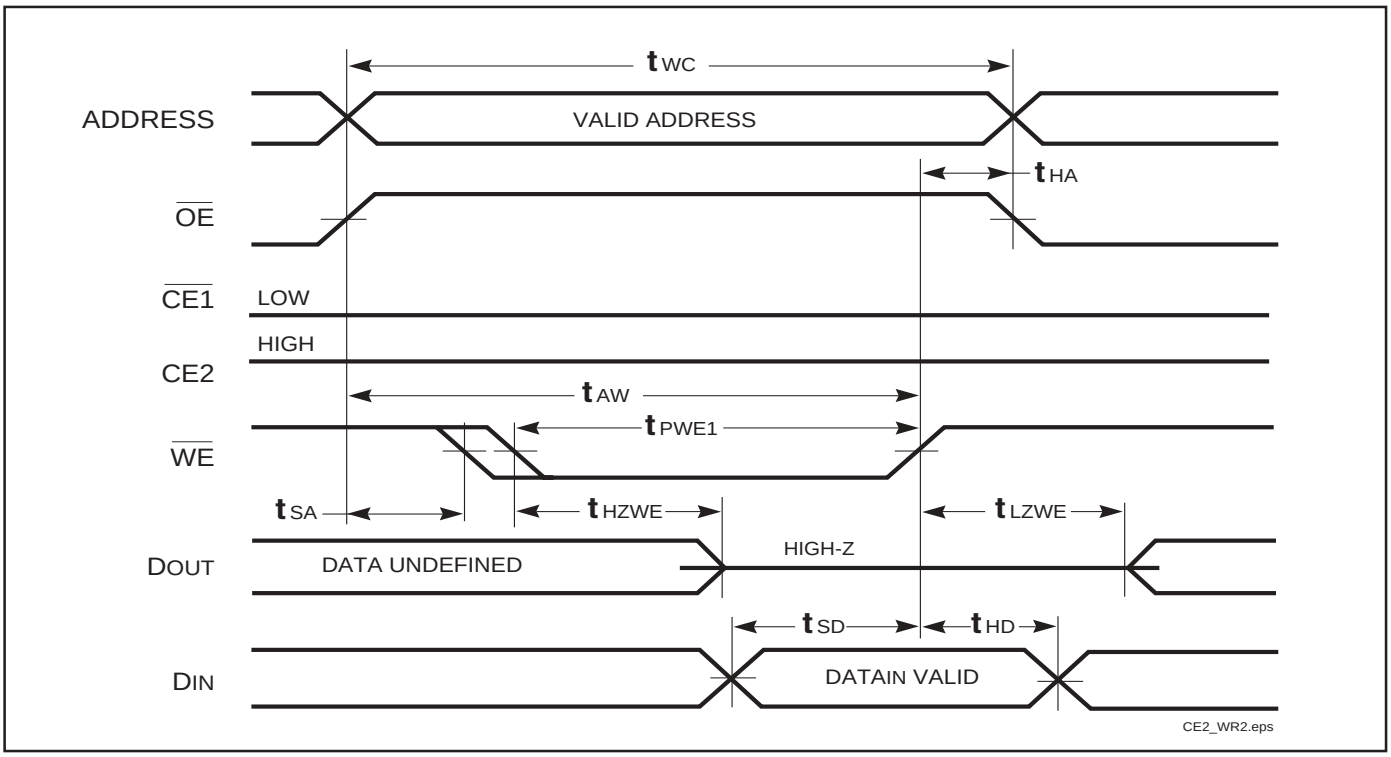
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with $\overline{OE}$ HIGH.
4. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

WRITE CYCLE NO. 1 (CE CONTROLLED, OE IS HIGH OR LOW) (1)



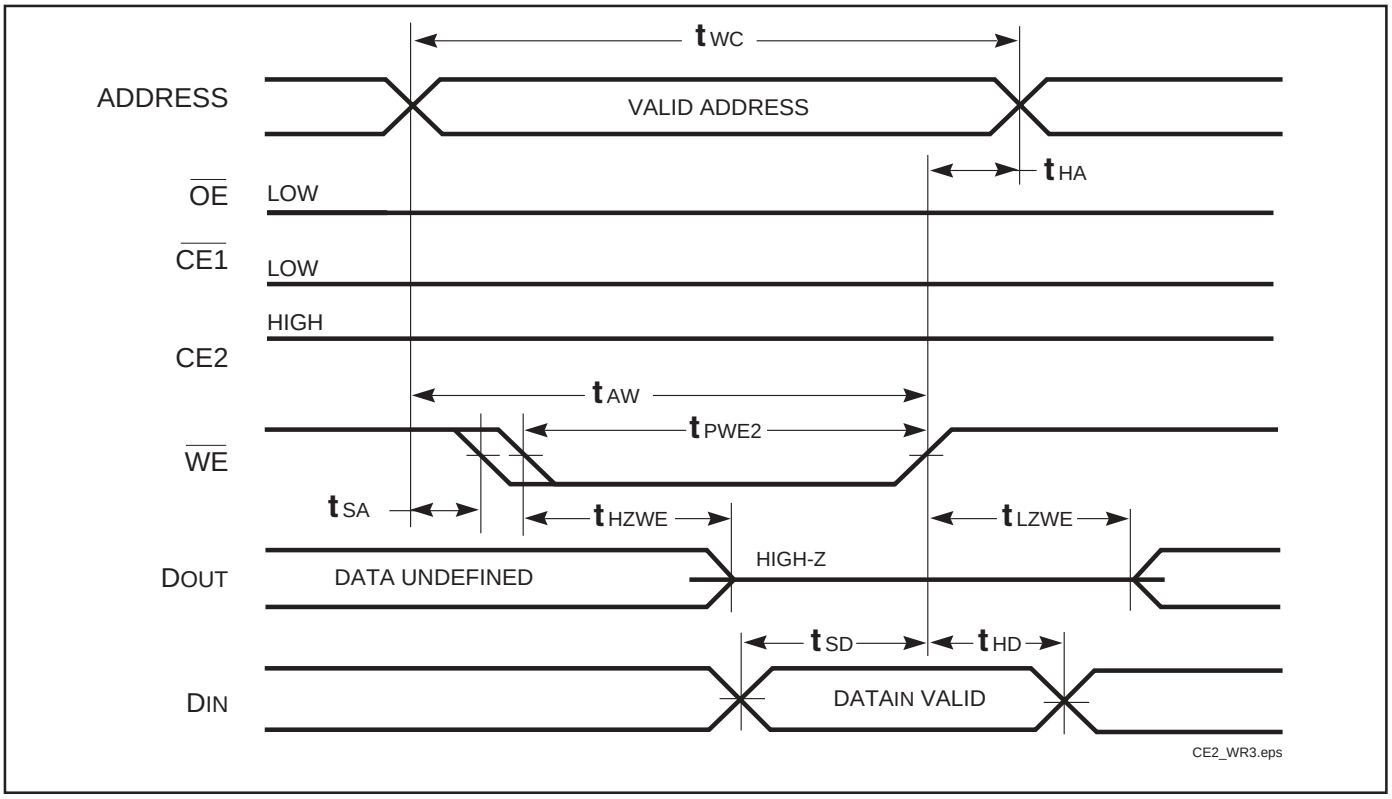
WRITE CYCLE NO. 2 ($\overline{OE}$ IS HIGH DURING WRITE CYCLE) (1,2)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

WRITE CYCLE NO. 3 ($\overline{OE}$ IS LOW DURING WRITE CYCLE) [1]



IS64C1024L LOW POWER VERSION ORDERING INFORMATION

Temperature Range (A1): –40°C to +85°C

Speed (ns)	Order Part No.	Package
15	IS64C1024L-15JA1	300-mil Plastic SOJ
	IS64C1024L-15KA1	400-mil Plastic SOJ
	IS64C1024L-15TA1	TSOP (Type I)

Temperature Range (A2): –40°C to +105°C

Speed (ns)	Order Part No.	Package
15	IS64C1024L-15JA2	300-mil Plastic SOJ
	IS64C1024L-15KA2	400-mil Plastic SOJ
	IS64C1024L-15TA2	TSOP (Type I)

Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
15	IS64C1024L-15JA3	300-mil Plastic SOJ
	IS64C1024L-15KA3	400-mil Plastic SOJ
	IS64C1024L-15TA3	TSOP (Type I)