IS61C6416

64K x 16 HIGH-SPEED CMOS STATIC RAM

ISSI®

MAY 1999

FEATURES

- High-speed access time: 10, 12, 15, and 20 ns
- CMOS low power operation
  - 1650 mW (max) @ -10ns Cycle
  - 55 μW (max) CMOS Standby
- TTL compatible interface levels
- Single 5V ± 10% power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Available in 44-pin SOJ package and 44-pin TSOP (Type II)
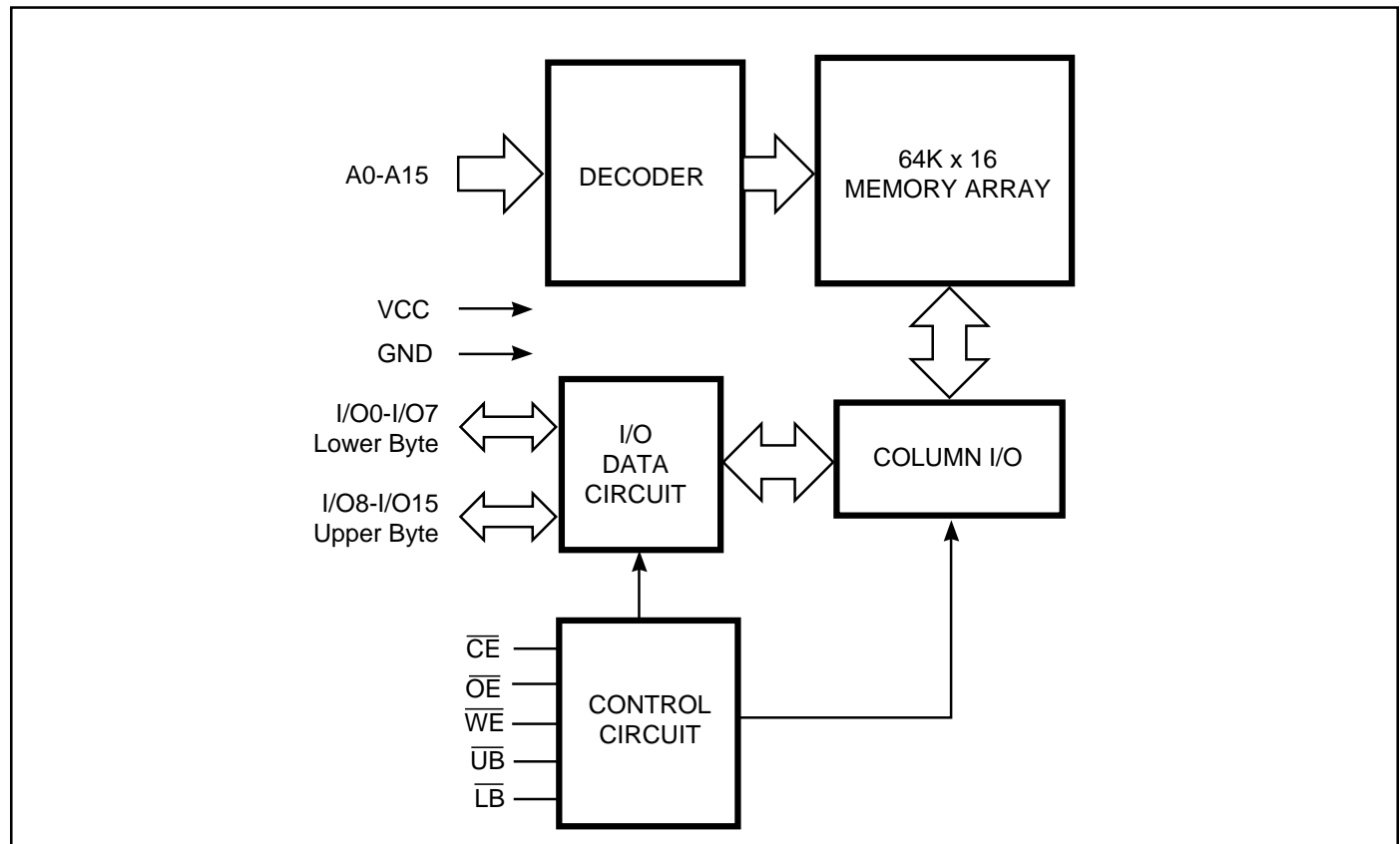
DESCRIPTION

The *ISSI* IS61C6416 is a high-speed, 1,048,576-bit static RAM organized as 65,536 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

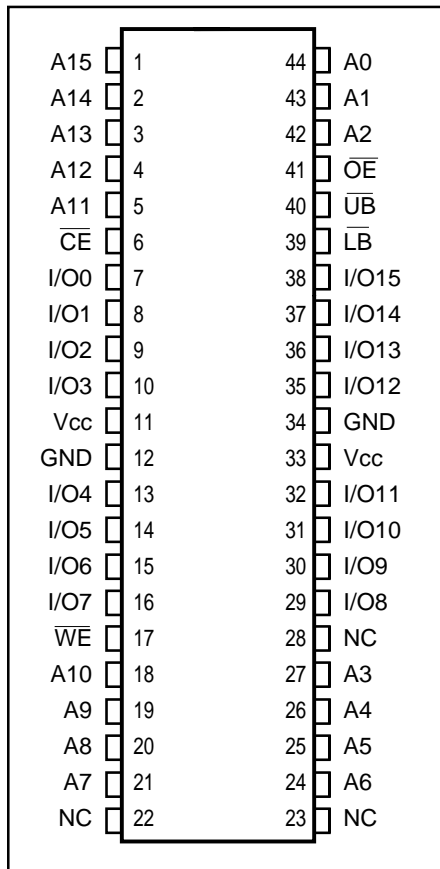The IS61C6416 is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type II).
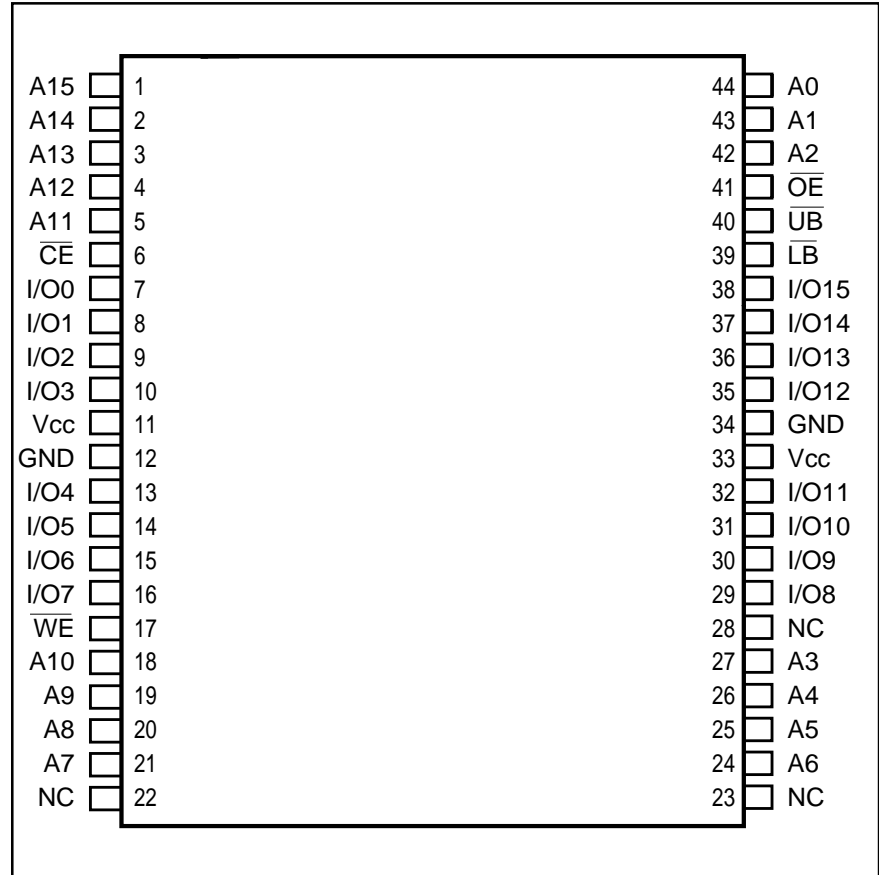
FUNCTIONAL BLOCK DIAGRAM

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PIN CONFIGURATIONS
44-Pin SOJ

A15	1	44	A0
A14	2	43	A1
A13	3	42	A2
A12	4	41	$\overline{OE}$
A11	5	40	$\overline{UB}$
$\overline{CE}$	6	39	$\overline{LB}$
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
Vcc	11	34	GND
GND	12	33	Vcc
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
$\overline{WE}$	17	28	NC
A10	18	27	A3
A9	19	26	A4
A8	20	25	A5
A7	21	24	A6
NC	22	23	NC

44-Pin TSOP (Type II)

A15	1	44	A0
A14	2	43	A1
A13	3	42	A2
A12	4	41	$\overline{OE}$
A11	5	40	$\overline{UB}$
$\overline{CE}$	6	39	$\overline{LB}$
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
Vcc	11	34	GND
GND	12	33	Vcc
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
$\overline{WE}$	17	28	NC
A10	18	27	A3
A9	19	26	A4
A8	20	25	A5
A7	21	24	A6
NC	22	23	NC

PIN DESCRIPTIONS

A0-A15	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input

$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

						I/O PIN		
Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0-I/O7	I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC1}, I_{CC2}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC1}, I_{CC2}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC1}, I_{CC2}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:
1. Stress greater than those listed under ABSO-LUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	Vcc
Commercial	0°C to +70°C	-10, -12	5V ± 5%
		-15, -20	5V ± 10%
Industrial	−40°C to +85°C	-12	5V ± 5%
		-15, -20	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	Vcc = Min., I_{OH} = −4.0 mA	2.4	—	V
		I_{OH} = −100 µA	—	3.95	
V_{OL}	Output LOW Voltage	Vcc = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	Vcc + 0.5	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ Vcc	−2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ Vcc, Outputs Disabled	−2	2	µA

Notes:
1. V_{IL} (min.) = −3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
Icc	Vcc Dynamic Operating Supply Current	Vcc = Max., I_{OUT} = 0 mA, f = MAX	Com.	—	300	—	280	—	260	—	235	mA
			Ind.	—	—	—	300	—	290	—	255	
I_{SB1}	TTL Standby Current (TTL Inputs)	Vcc = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH} , f = max	Com.	—	50	—	50	—	50	—	50	mA
			Ind.	—	—	—	55	—	55	—	55	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	Vcc = Max., $\overline{CE}$ ≥ Vcc − 0.2V, V_{IN} ≥ Vcc − 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	—	10	—	10	—	10	—	10	mA
			Ind.	—	—	—	15	—	15	—	15	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

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CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C_{OUT}	Input/Output Capacitance	$V_{OUT} = 0V$	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	4	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	15	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	6	—	7	—	9	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	6	0	6	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZCE}[2	$\overline{CE}$ to High-Z Output	0	5	0	6	0	6	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	5	—	6	—	7	—	9	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	5	0	6	0	6	0	8	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

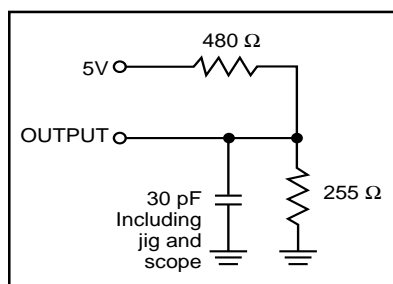| Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

Figure 1

Figure 2
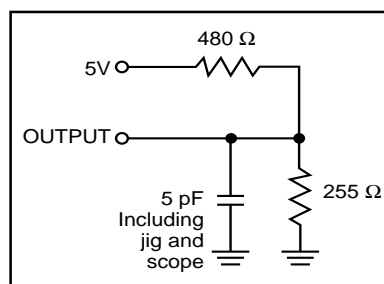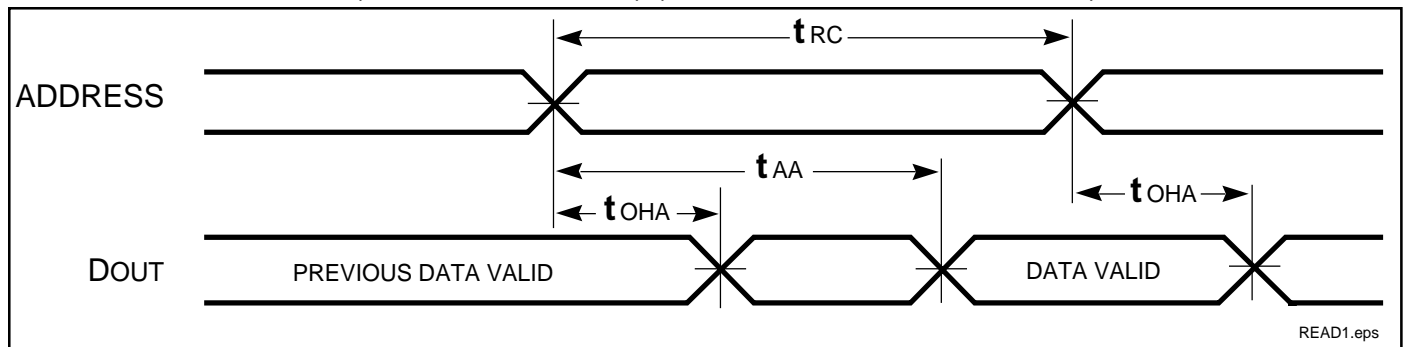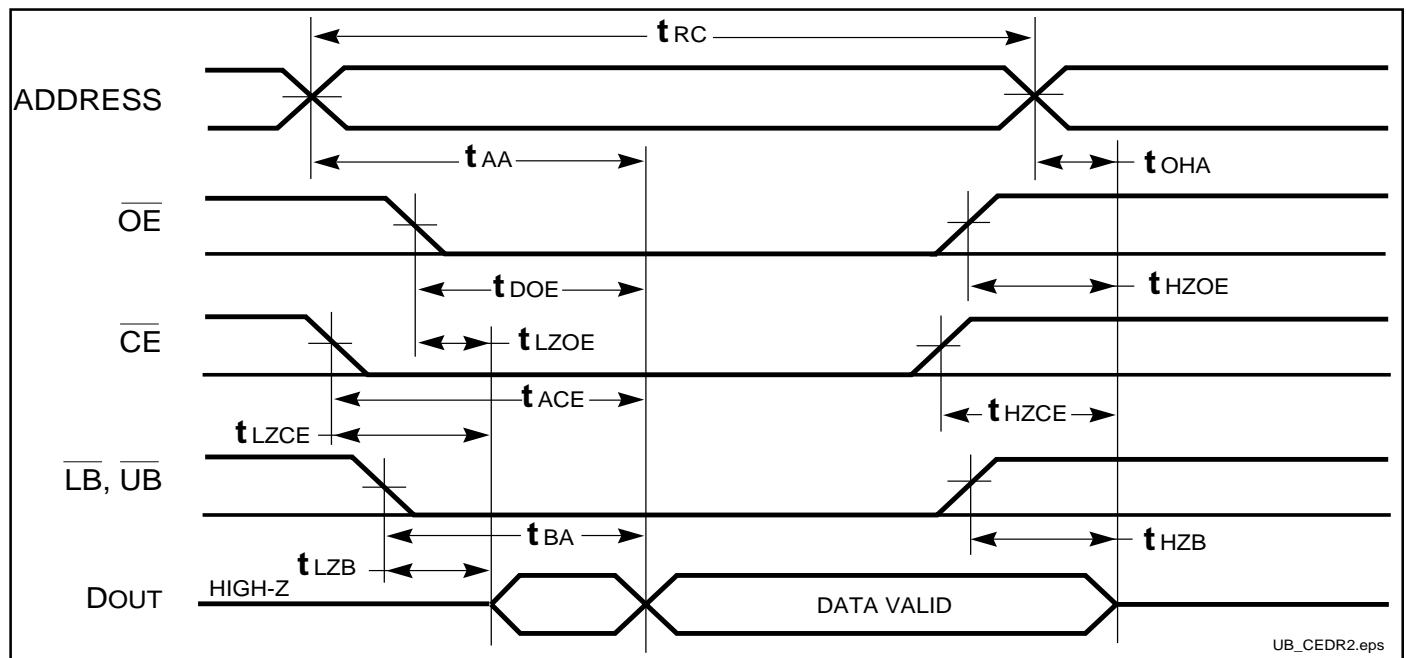
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AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)

READ1.eps

READ CYCLE NO. 2[1,3]

UB_CEDR2.eps

Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$.
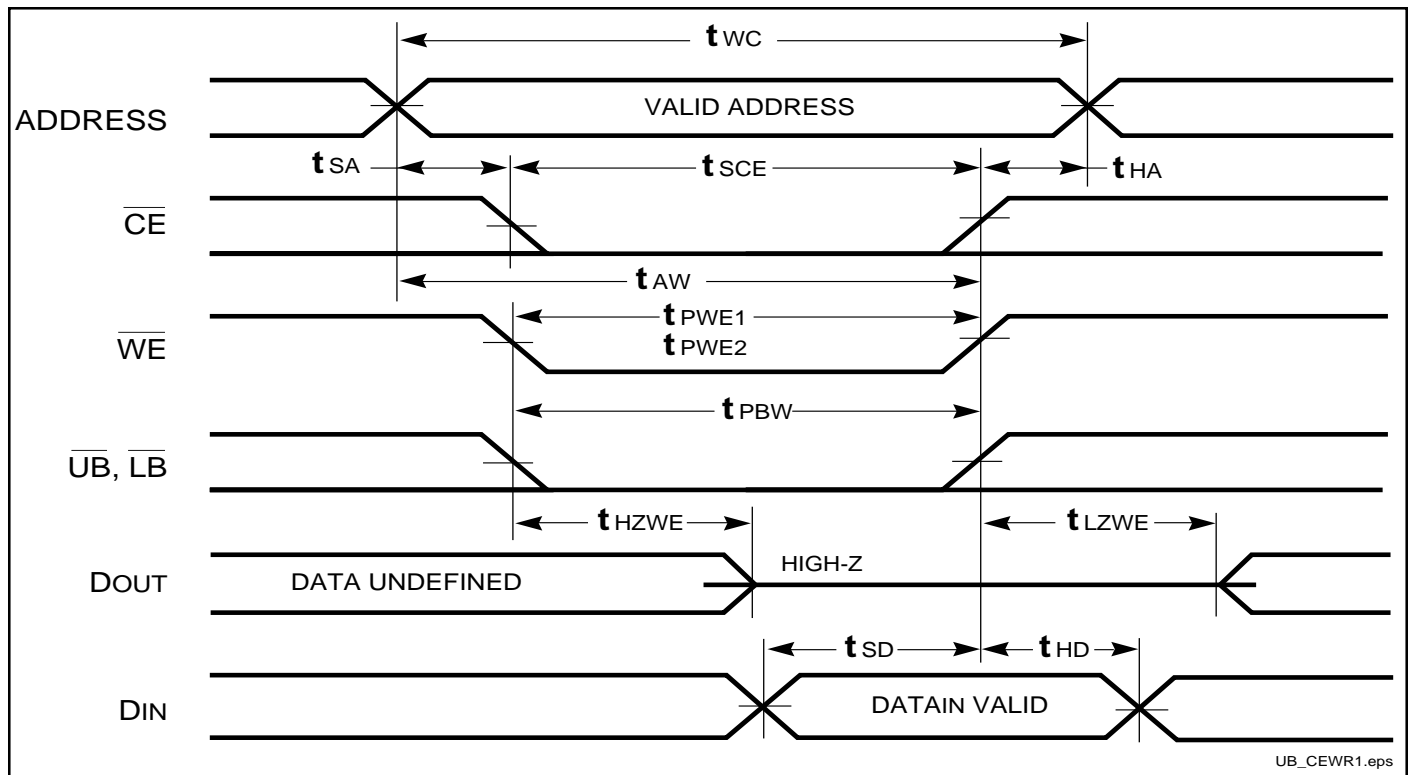3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

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WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

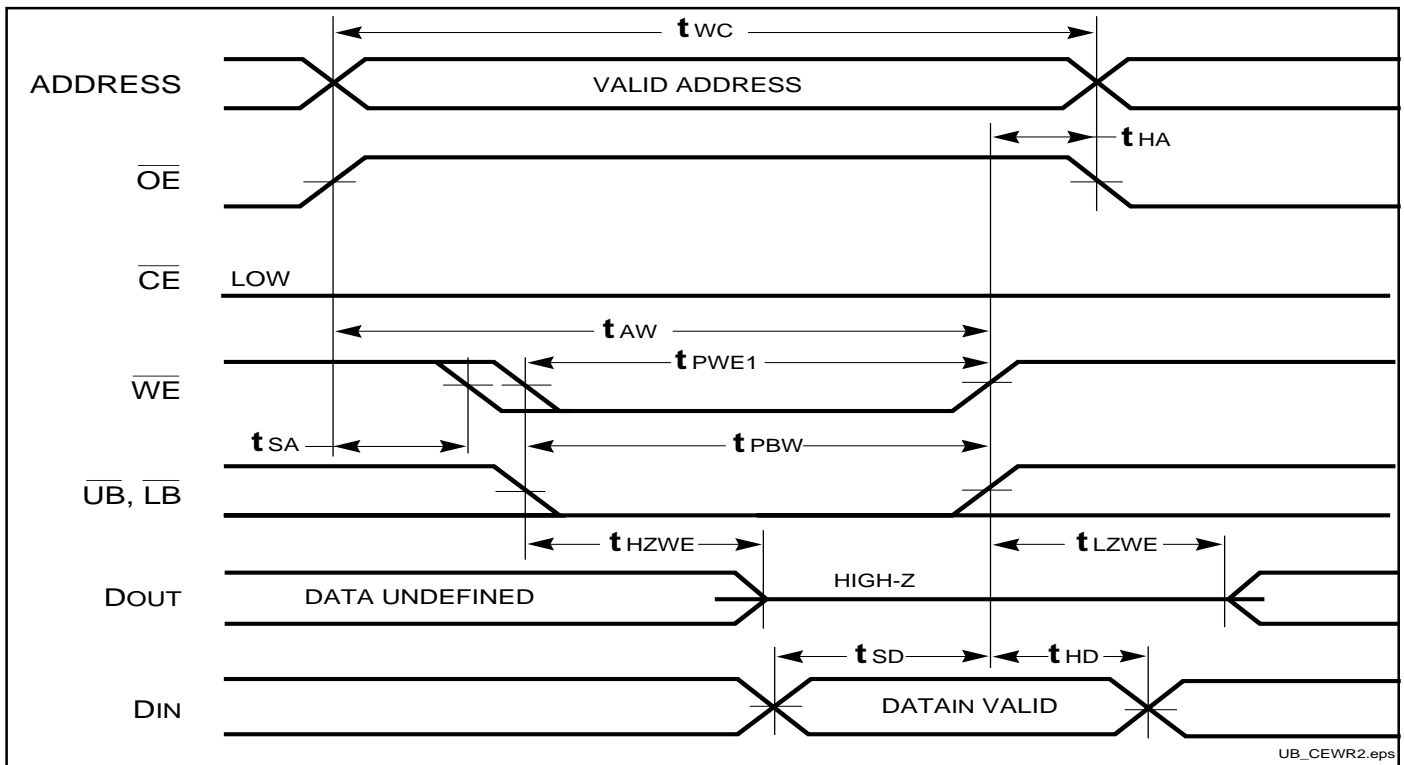| Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	8	—	9	—	10	—	12	—	ns
t_{AW}	Address Setup Time to Write End	8	—	9	—	10	—	12	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	8	—	9	—	10	—	12	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	8	—	9	—	10	—	12	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$=Low)	8	—	9	—	10	—	12	—	ns
t_{SD}	Data Setup to Write End	6	—	6	—	7	—	9	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	5	—	6	—	7	—	9	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	3	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
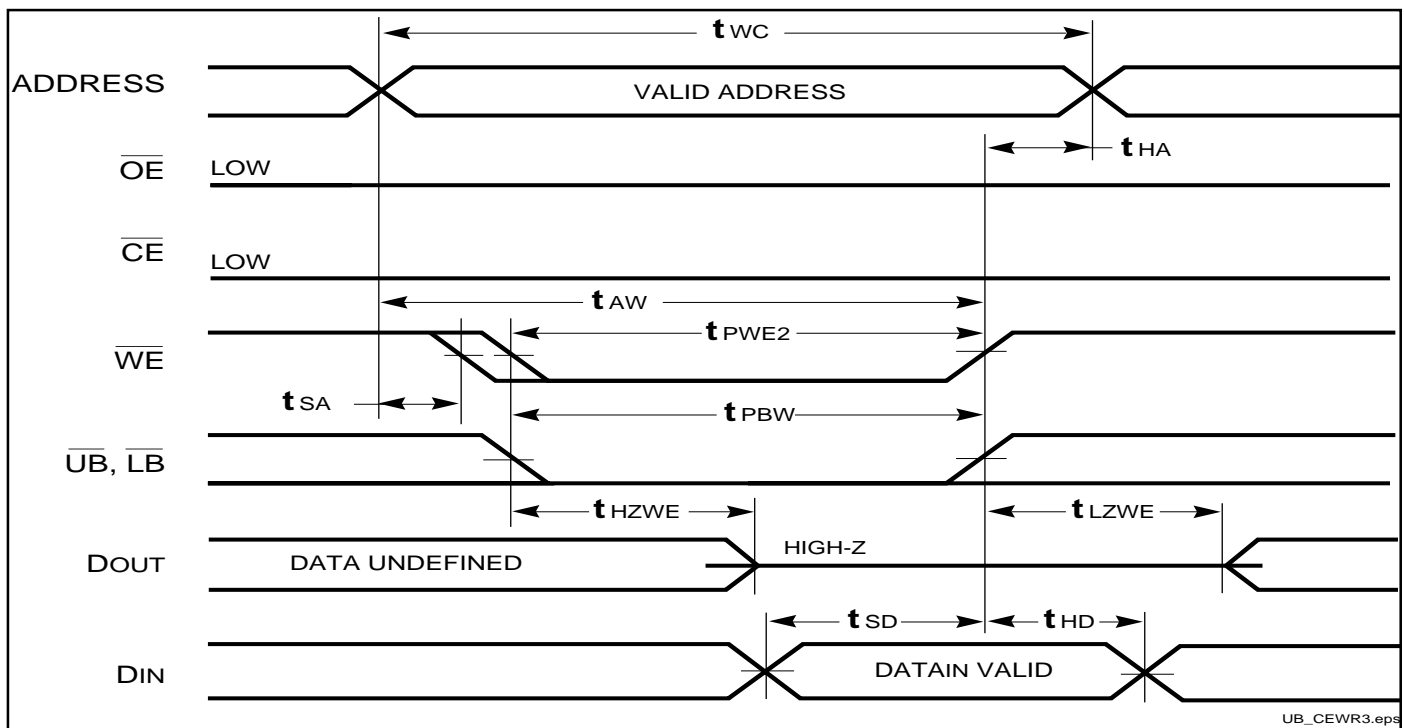
AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]

UB_CEWR1.eps

Notes:
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE}$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CE}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

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WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]

UB_CEWR2.eps

WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]

UB_CEWR3.eps

Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 4 ($\overline{\text{UB}}/\overline{\text{LB}}$ Back to Back Write)

UB_CEWR4.eps

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IS61C6416-10T	Plastic TSOP(II)
10	IS61C6416-10K	400-mil Plastic SOJ
12	IS61C6416-12T	Plastic TSOP(II)
12	IS61C6416-12K	400-mil Plastic SOJ
15	IS61C6416-15T	Plastic TSOP(II)
15	IS61C6416-15K	400-mil Plastic SOJ
20	IS61C6416-20T	Plastic TSOP(II)
20	IS61C6416-20K	400-mil Plastic SOJ

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61C6416-12TI	Plastic TSOP(II)
12	IS61C6416-12KI	400-mil Plastic SOJ
15	IS61C6416-15TI	Plastic TSOP(II)
15	IS61C6416-15KI	400-mil Plastic SOJ
20	IS61C6416-20TI	Plastic TSOP(II)
20	IS61C6416-20KI	400-mil Plastic SOJ