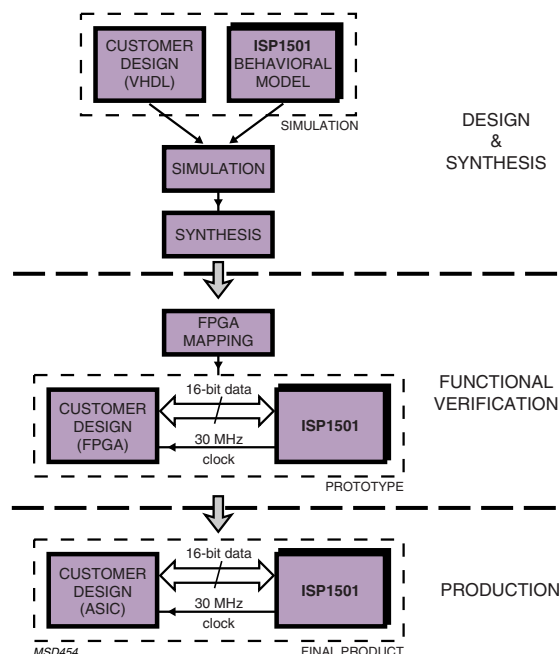


Simplify your ASIC implementation with the ISP1501 Universal Serial Bus (USB) transceiver. This generic USB 2.0 transceiver improves the chance of successful ASIC implementation by allowing FPGA verification through its 16-bit bidirectional data bus. The ISP1501 from Philips Semiconductors is ideal for current and future high-performance scanners, digital cameras, printers, and external storage devices.



Key Features

- **Greatly reduced risk of errors during ASIC implementation:** 16-bit bidirectional data bus allows FPGA verification to be performed
- **Minimal crosstalk:** separate 3.3-V supplies for analog transceiver and digital I/Os
- **Flexibility:** complies with Universal Serial Bus Specification Rev. 2.0 and legacy USB 1.1 transceiver interfaces
- **Use in all power conditions:** supports bus-powered (with low suspend current), self-powered, or hybrid-powered applications
- **Lower costs:** can be run with widely available external 12-MHz crystal
- **Test mode:** loopback test mode enables the SIE to perform a self-test on the data bus and the analog D+/D- lines
- **Exceptional capability:** for high-performance scanners, cameras, printers, and external storage devices, including portable hard disks, Zip®, MO, and DVD drives

ISP1501 USB 2.0 Peripheral Transceiver

Today's USB for Advanced Peripherals

The ISP1501 USB 2.0 peripheral transceiver can reduce the risks of application specific integrated circuit (ASIC) implementation and help USB core designers leverage their previous development efforts. This versatile transceiver is optimal for use as a USB 2.0 analog front end for ASICs and Field-Programmable Gate Arrays (FPGAs) with built-in USB Serial Interface Engine (SIE) cores. The 16-bit bidirectional data bus interface to the SIE runs at 30 MHz, enabling effective FPGA verification. Integrating a USB full-speed transceiver and a USB high-speed transceiver, the ISP1501 provides connectivity that complies with USB Specification Rev. 2.0 for peripherals.

Add performance, keep legacy interfaces. The transceiver switches to a USB 1.1 legacy interface when it is used to drive full-speed signaling, which means few or no changes to existing USB 1.1 core interfaces. Designed for bus-powered applications with low suspend currents, the ISP1501 can be used in self-, hybrid-, or bus-powered conditions. High-speed data transmission capability, integrated bit stuffing and unstuffing, and NRZI encoding and decoding are included on the ISP1501. When the transceiver is running at full speed, the bit-stuffing logic and NRZI logic are implemented on the external SIE.

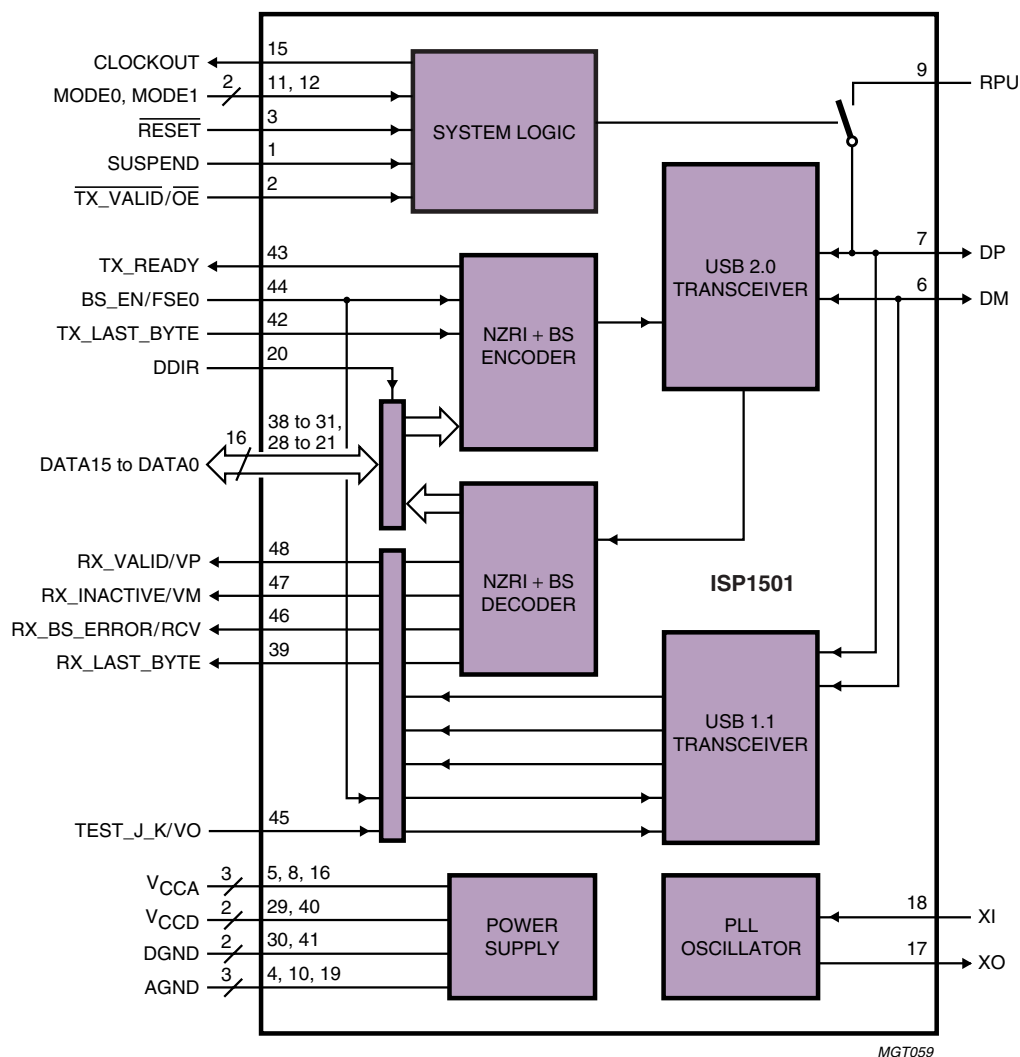
Convenient and cost-saving. The ISP1501 can use an external 12-MHz crystal running on the fundamental frequency or an external 12-MHz clock input. No passive resistor or inductor is required. Because the 12-MHz crystal is widely available and frequently used, this solution keeps costs low. The ISP1501's loopback test mode enables the SIE to perform a self-test on the data bus and the analog D+/D- lines. The SIE can use the 30-MHz clock as a heartbeat clock. In suspend condition, the clock is held at logic high and then, upon resume, runs again.

Additional features of the ISP1501 include USB data recovery upon receiving and data synchronization upon transmitting and internal power-on reset. The transceiver is available in the LQFP48 package.

Let's make things better.



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