

DDR Phase Lock Loop Clock Driver

Recommended Application:

DDR Memory Modules

Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution
- Feedback pins for input to output synchronization
- Active high OE to enable outputs
- Spread Spectrum tolerant inputs

Specifications:

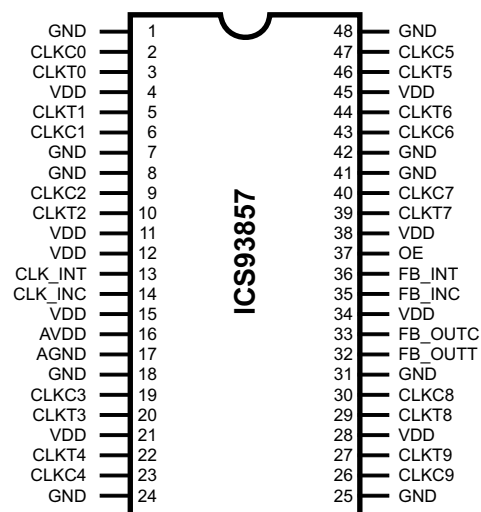
Input/Output Level

- Inputs and outputs are compatible to JEDEC SSTL-2 standard.

Switching Characteristics:

- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz): <120ps
- CYCLE - CYCLE jitter (>100MHz): <65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

Pin Configuration

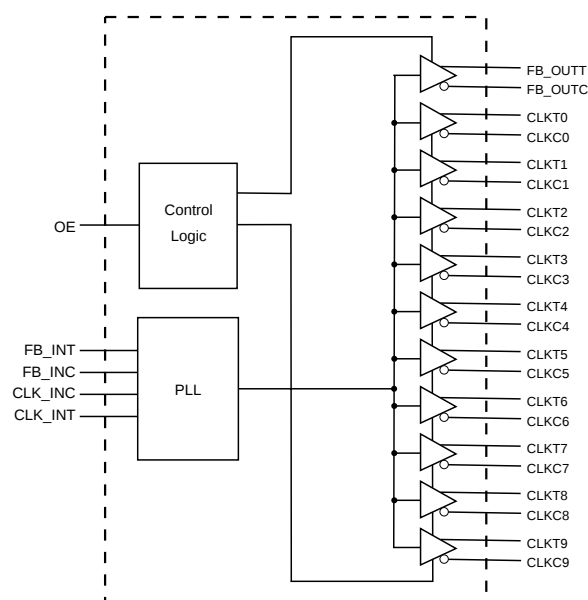


48-Pin TSSOP

Functionality

INPUTS				OUTPUTS				PLL State
AVDD	OE	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	L	H	Z	Z	Z	Z	off
2.5V (nom)	L	H	L	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20MHz ⁽¹⁾		Z	Z	Z	Z	off

Block Diagram





Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 11, 12, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs.
14	CLK_INC	IN	"Complementary" reference clock input
13	CLK_INT	IN	"True" reference clock input
33	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
32	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
36	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
35	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
37	OE	IN	Active High output enable pin



Absolute Maximum Ratings

Supply Voltage (VDD & AVDD)	-0.5V to 4.6V
Logic Inputs	GND–0.5 V to V _{DD} +0.5 V
Ambient Operating Temperature	0°C to +85°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	I _{IH}	VI = VDD or GND			±10	μA
Input Low Current	I _{IL}	VI = VDD or GND			±10	μA
Operating Supply Current	I _{DD2.5}	CL = 0pf		250		mA
	I _{DDPD}	CL = 0pf		50	100	μA
Output High Current	I _{OH}	VDD = 2.3V, V _{OUT} = 1V	-18	-32		mA
Output Low Current	I _{OL}	VDD = 2.3V, V _{OUT} = 1.2V	26	30		mA
High Impedance Output Current	I _{OZ}	VDD=2.7V, V _{out} =VDD or GND			±10	μA
High-level output voltage	V _{OH}	VDD = min to max, IOH = -1 mA	VDD -0.1			V
		VDD = 2.3V, IOH = -12 mA	1.7			V
Low-level output voltage	V _{OL}	VDD = min to max I _{OL} =1 mA			0.1	
		VDD = 2.3V IOH=12 mA			0.6	V
Input Capacitance ¹	C _{IN}	VI = GND or VDD			9	pF
Output differential-pair crossing voltage	V _{OC}		(V _{DD} /2) -0.2	V _{DD} /2	(V _{DD} /2) +0.2	V

¹Guaranteed by design, not 100% tested in production.

Recommended Operating Condition

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog/core supply voltage	A _{VDD}		2.3	2.5	2.7	V
Input High Voltage	V _{IH}	OE input	0.7 x V _{DD}			V
Input Low Voltage	V _{IL}	OE input			0.3 x V _{DD}	V
Input voltage level	V _{IN}		-0.3		V _{DD} +0.3	V

¹Guaranteed by design, not 100% tested in production.



Preliminary Product Preview

Timing Requirements

$T_A = 0 - 85^\circ\text{C}$; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

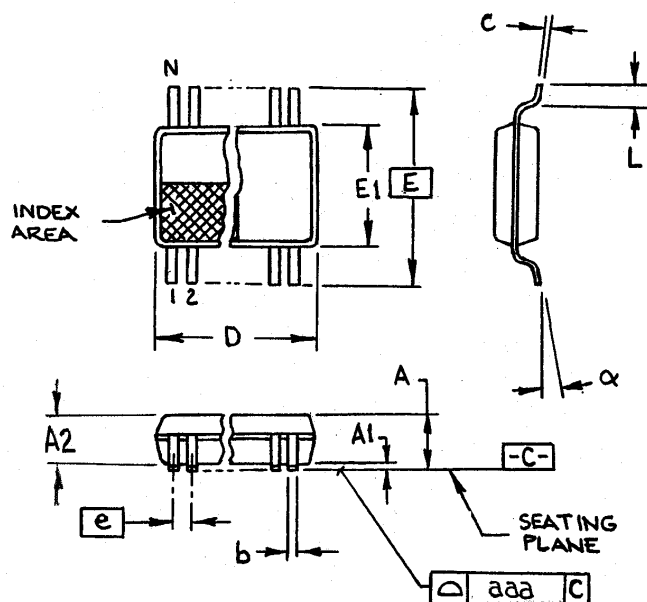
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating clock frequency	freq_{op}		66	170	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}	from VDD = 3.3V to 1% target freq.		100	μs

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time, bypass mode	t_{PLH}^1	CLK_IN to any output	1.5	3.5	6	ns
High-to low level propagation delay time	t_{PLL}^1	CLK_IN to any output	1.5	3.5	6	ns
Output enable time	t_{EN}	OE to any output		3		ns
Output disable time	t_{dis}	OE to any output		3		ns
Jitter; peak to peak jitter	T_{jitter}	100/125/133/167MHz			75	ps
Cycle to Cycle Jitter1	$T_{\text{cyc}} - T_{\text{cyc}}$	100/125/133/167MHz			75	ps
Phase error, static	$t_{\text{(phase error)}}$		-150		150	ps
Output to Output Skew	T_{skew}				100	ps
Duty cycle	D_C^2	100MHz to 167MHz	49		51	%
Rise Time, Fall Time	t_r, t_f	Load = 120 Ω /16pF		800	950	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.30
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

MO-153 JEDEC
Doc.# 10-0039 7/6/00 Rev B

Ordering Information

ICS93857yGT

Example:

ICS XXXX y G - PPP - T

Designation for tape and reel packaging

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
G=TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device