iC-NV

6-BIT Sin/D FLASH CONVERTER

target specification

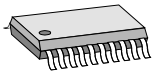
FEATURES

- Fast flash converter
- Selectable resolution of up to 64 steps per cycle and up to 16-fold interpolation
- Integrated instrumentation amplifiers with adjustable gain
- Direct connection of sensor bridges, no external components required
- 200kHz input frequency with the highest resolution
- Incremental A QUAD B output of up to 3.2MHz
- Reversed A/B phase selectable
- Index signal processing
- Low power consumption from single 5V supply
- TTL- /CMOS-compatible outputs
- Inputs and outputs protected against destruction by ESD

APPLICATIONS

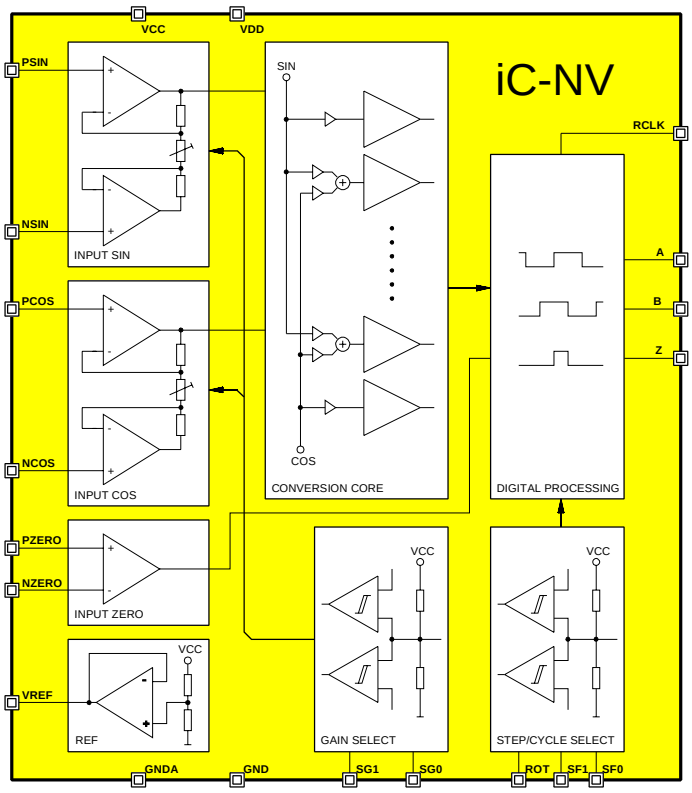
- Angle interpolation from orthogonal sinusoidal input signals
- Linear and rotary encoders
- MR sensor systems

PACKAGES



TSSOP20

BLOCK DIAGRAM



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DESCRIPTION

iC-NV is a monolithic A/D converter which produces two digital A/B incremental signals phase-shifted at 90° from two sinusoidal input signals, also phase-shifted at 90°.

The converter operates on the flash principle with fast single comparators. For static input signals hysteresis prevents the switching of the outputs.

By programming the pins the interpolator can be set to nine different resolutions between 4 and 64 angle steps per cycle; multiplication values of between 1 and 16 are possible for the frequency. The phase relation between the sine/cosine input signals and the A/B incremental signals generated can be selected here.

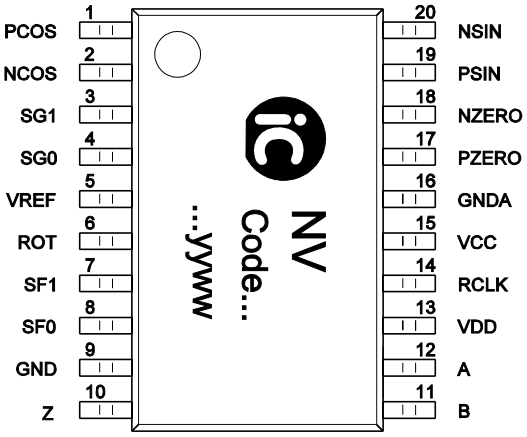
The device also incorporates an index signal processing circuit which generates a digital zero pulse at Z dependent on the analog sine/cosine input signals and the enable input ZERO. Alternatively, the converter MSB can also be output at Z for synchronization purposes in an absolute measuring system.

The input amplifiers are configured as instrumentation amplifiers and permit sensor bridges to be directly connected without the need for external resistors. The input amplification has nine selectable settings which have been graded to suit standard sensor signals of between ca. 10mVpk and 1Vpk.

PACKAGES TSSOP20 to JEDEC Standard

PIN CONFIGURATION TSSOP20 4.4mm

(top view)



PIN FUNCTIONS

No.	Name	Function
1	PCOS	Input Cosine +
2	NCOS	Input Cosine −
3	SG1	Gain Select
4	SG0	Gain Select
5	VREF	Reference Voltage
6	ROT	A/B Phase Select
7	SF1	Resolution Select
8	SF0	Resolution Select
9	GND	Ground (digital)
10	Z	Output Index Z / MSB
11	B	Incremental Output B
12	A	Incremental Output A
13	VDD	+5V Supply Voltage (digital)
14	RCLK	Setup Resistor (use is optional; can be wired to VCC or requires resistor to GNDA)
15	VCC	+5V Supply Voltage (analog)
16	GNDA	Ground (analog)
17	PZERO	Input Zero Signal +
18	NZERO	Input Zero Signal −
19	PSIN	Input Sine +
20	NSIN	Input Sine −

External connections linking VCC to VDD and GND to GNDA are required.

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VCC	Supply Voltage analog			-0.3	6	V
G002	VDD	Supply Voltage digital			-0.3	6	V
G003	V()	Voltage at NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, RCLK SF1, SF0, ROT, A, B, Z	V() < VCC+0.3V V() < VDD+0.3V		-0.3	6	V
G004	Imx(VCC)	Current in VCC			-50	50	mA
G005	Imx(GNDA)	Current in GNDA			-50	50	mA
G006	Imx(VDD)	Current in VDD			-50	50	mA
G007	Imx(GND)	Current in GND			-50	50	mA
G008	Imx()	Current in NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, VREF, RCLK, SF1, SF0, ROT, A, B, Z			-10	10	mA
G009	Ilu()	Pulse Current in all pins (Latch-up strength)	pulse duration < 10µs		-100	100	mA
EG1	Vd()	ESD Susceptibility at all pins	MIL-STD-883, Method 3015, HBM 100pF discharged through 1.5kΩ			2	kV
TG1	Tj	Operating Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature Range			-40	165	°C

THERMAL DATA

Operating Conditions: VCC= VDD= 5V ±10%

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range (extended range on request)			-25		85	°C

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VDD= 5V ±10%, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VCC, VDD	Permissible Supply Voltage				4.5		5.5	V
002	I(VCC)	Supply Current in VCC	fin()= 200kHz; A, B, Z open					15	mA
003	I(VDD)	Supply Current in VDD	fin()= 200kHz; A, B, Z open					5	mA
004	Vc()hi	Clamp Voltage hi at NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, ROT, SF1, SF0, VREF, RCLK	Vc()hi= V() -VCC; I()= 1mA, other pins open			0.3		1.6	V
005	Vc()lo	Clamp Voltage lo at NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, ROT, SF1, SF0, VREF, RCLK, A, B, Z	I()= -1mA, other pins open			-1.5		-0.3	V
006	Vc()hi	Clamp Voltage hi at A, B, Z	Vc()hi= V()-VDD; I()= 1mA, other pins open			0.3		1.6	V
Input Amplifiers NSIN, PSIN, NCOS, PCOS									
101	Vos()	Input Offset Voltage	Vin() see table gain select			-10		10	mV
102	Iin()	Input Current	V()= 0V.. VCC			-50		50	nA
103	G()	Gain	GAIN following table gain select			95		101	%
104	Grel	Gain Ration SIN/COS	GAIN following table gain select			98		102	%
105	fhc	Cut-off Frequency	GAIN= 66.667 GAIN= 3.03			500 2.3			kHz MHz
106	SR	Slew Rate	GAIN= 66.667 GAIN= 3.03			10 15			V/µs V/µs
Signal Processing: Converter Accuracy									
201	AAabs	Absolute Angular Accuracy	referred to 360° input signal, GAIN= 3.03			-1		1	DEG
202	AArel	Relative Angular Accuracy	referred to period of AX, GAIN= 3.03			-10		10	%
VREF									
401	V(VREF)	Reference Voltage at VREF	I(VREF)= -1mA..+1mA			48		52	%VCC
Zero Comparator									
701	Vos()	Input Offset Voltage	V()= Vcm()			-20		20	mV
702	Iin()	Input Current	V()= 0V.. VCC			-50		50	nA
703	Vcm()	Common-Mode Input Voltage Range				1.4		VCC-1.5	V
704	Vdm()	Differential Input Voltage Range				0		VCC	V
Signal Processing: Inputs SG1, SG0, ROT, SF1, SF0									
801	Vt()hi	Input Threshold Voltage hi				60		78	%VCC
802	Vt()lo	Input Threshold Voltage lo				25		40	%VCC
803	V0()	Mid Level Voltage				43		57	%VCC
804	Ri()	Input Resistance				45	150	220	kΩ

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VDD= 5V ±10%, Tj= -40..125°C, unless otherwise noted

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Signal Processing: Outputs A, B, Z									
D01	Vs()hi	Saturation Voltage hi	Vs()hi= VDD-V(); I()= -4mA					0.4	V
D02	Vs()lo	Saturation Voltage lo	I()= 4mA					0.4	V
D05	tr()	Rise Time	CL()= 50pF					60	ns
D06	tf()	Fall Time	CL()= 50pF					60	ns

DESCRIPTION OF FUNCTIONS

Input Amplifiers

Input stages SIN and COS are configured as instrumentation amplifiers. The gain is dependent on the amplitude of the input signal and set via pins SG0 and SG1 according to the following table. So that the DC level to be adjusted half of the supply voltage is available at VREF.

GAIN SELECT

SG1	SG0	Gain	Sine/Cosine Input Signal Levels Vin()			
			Amplitude		Average value (DC)	
			differential	single ended	differential	single ended
hi	hi	66.667	up to 60mVpp	up to 120mVpp	0.7V .. VCC-1.2V	0.7V .. VCC-1.2V
hi	open	50.000	up to 80mVpp	up to 160mVpp	0.7V .. VCC-1.2V	0.7V .. VCC-1.2V
hi	lo	33.333	up to 120mVpp	up to 240mVpp	1.2V .. VCC-1.2V	1.2V .. VCC-1.3V
open	hi	20.000	up to 0.2Vpp	up to 0.4Vpp	1.2V .. VCC-1.2V	1.2V .. VCC-1.3V
open	open	14.300	up to 0.28Vpp	up to 0.56Vpp	0.7V .. VCC-1.3V	0.8V .. VCC-1.4V
open	lo	10.000	up to 0.4Vpp	up to 0.8Vpp	1.2V .. VCC-1.3V	1.3V .. VCC-1.5V
lo	hi	7.125	up to 0.56Vpp	up to 1.1Vpp	1.2V .. VCC-1.4V	1.4V .. VCC-1.7V
lo	open	4.000	up to 1Vpp	up to 2Vpp	1.2V .. VCC-1.6V	1.6V .. VCC-2.1V
lo	lo	3.030	up to 1.3Vpp	up to 2.6Vpp	1.2V .. VCC-1.7V	1.8V .. VCC-2.4V

Converter Core

For each of the 64 comparator levels the sine/cosine input signals are calculated according to the theorem of addition and are fed into single comparators. This procedure guarantees a very high converter frequency yet also means that consecutive comparators can switch in a very short space of time in the event of input signal disturbances.

Digital Processing Unit

By this unit the transition events are converted into a pulse sequence for the incremental outputs A and B. The square-wave signals generated have a phase shift of +90° or -90°, depending on the direction of rotation. The phase relation between the sine/cosine input signals and the A/B output signals can be set using programming pin ROT.

A/B PHASE SELECT

ROT	Input signals	Output signals
lo / open	positive; COS leading SIN	B leading A
lo / open	negative; SIN leading COS	A leading B
hi	positive; COS leading SIN	A leading B
hi	negative; SIN leading COS	B leading A

Resolution, frequency ranges

Nine different resolutions or interpolation factors (IPF) can be programmed via inputs SF0 and SF1. Resolutions 16, 12 and 10 are generated at the core of the converter itself. Resolutions of less than 10 are produced by division DIV in the digital processing unit. The following table gives possible settings.

RESOLUTION SELECT

SF1	SF0	IPF	DIV factor	fin_{MAX}
hi	hi	16	1	200kHz
hi	open	12	1	260kHz
hi	lo	10	1	320kHz
open	hi	8	2	400kHz
open	open	5	2	640kHz
open	lo	4	4	800kHz
lo	hi	3	4	1.04MHz
lo	open	2	8	1.6MHz
lo	lo	1	16	(3.2MHz)

Hysteresis

iC-NV has an angular hysteresis which is independent of the input amplitude and phase. It prevents the outputs from switching when the inputs are static. The following diagram shows the effect this has with an interpolation factor of 8.

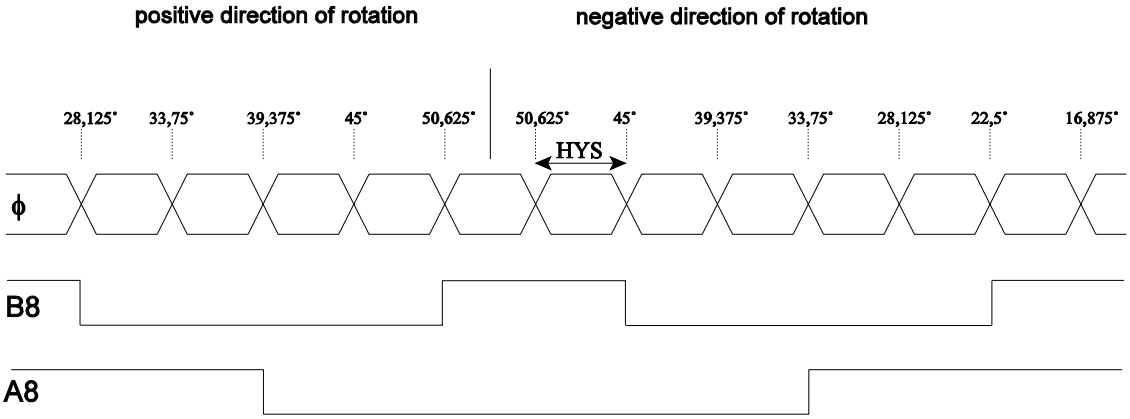


Fig. 1: Effect of angle hysteresis

When the direction of rotation is reversed the integrated hysteresis circuit prompts the change in direction to be signaled at the outputs; the hysteresis causes a delay here. According to the resolution the hysteresis is set to one of the following fixed values.

ANGLE HYSTERESIS									
Interpolation factor	1	2	3	4	5	8	10	12	16
Hysteresis DEG	5,625°	5,625°	7,5°	5,625°	9°	5,625°	9°	7,5°	5,625°
referred to A/B period	1/64	1/32	1/16	1/16	1/8	1/8	1/4	1/4	1/4

Zero pulse

One zero pulse (index) is generated per cycle from the sine/cosine inputs. To be output to Z it must be enabled by the comparator at differential inputs PZERO and NZERO. The width of the zero pulse is a quarter of the length of the A and/or B signal output cycle. When Z is high, simultaneously A&B are high. The position of the zero pulse dependent on the interpolation factor and the direction of rotation is given in the following table.

INDEX POSITION		
IPF	**positive direction of rotation**	**negative direction of rotation**
16	45°.. 50,625°	39,375° .. 45°
12	45°.. 52,5°	37,5° .. 45°
10	45°.. 54°	36° .. 45°
8	39,375°.. 50,625°	33,75° .. 45°
5	36° .. 54°	27° .. 45°
4	33,75° .. 56,25°	28,125° .. 50,625°
3	30°.. 60°	22,5° .. 52,5°
2	22,5 .. 67,5°	16,875° .. 61,875°
1	0° .. 90°	354,375° .. 84,625°

Alternatively, the MSB of the converter can be output to Z when ROT is high. With the zero signal this changes to high and has the pulse length of half a cycle. This signal can be used to synchronize the high-order tracks of an absolute-value encoder device.

Oscilloscope diagrams

The following diagrams give the input and output signals for various directions of rotation and ROT settings for interpolation factors 1, 2 and 16.

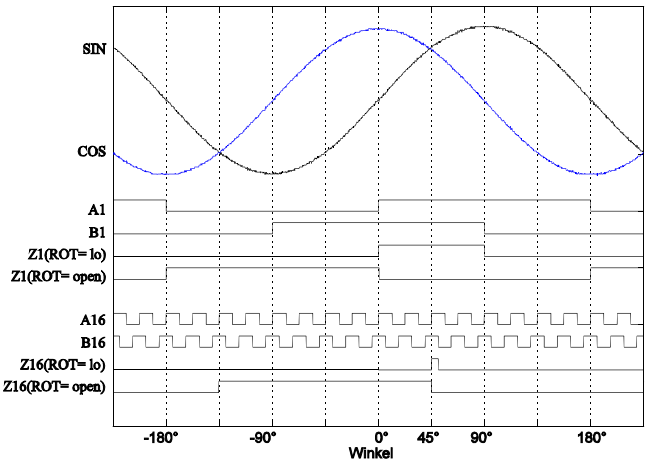


Fig. 2: ROT= lo/open, COS leading SIN

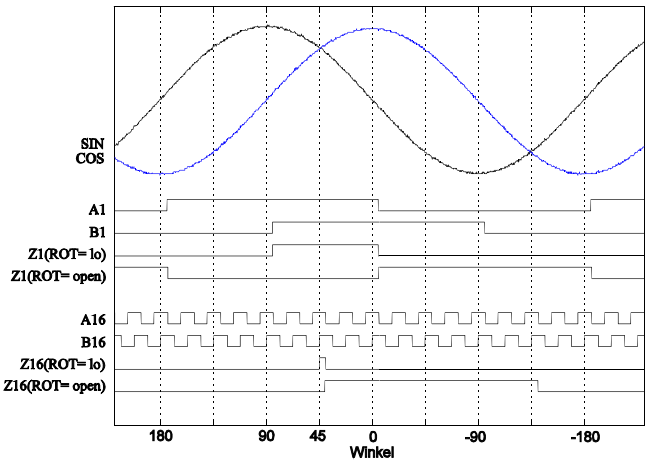


Fig. 3: ROT= lo/open, SIN leading COS

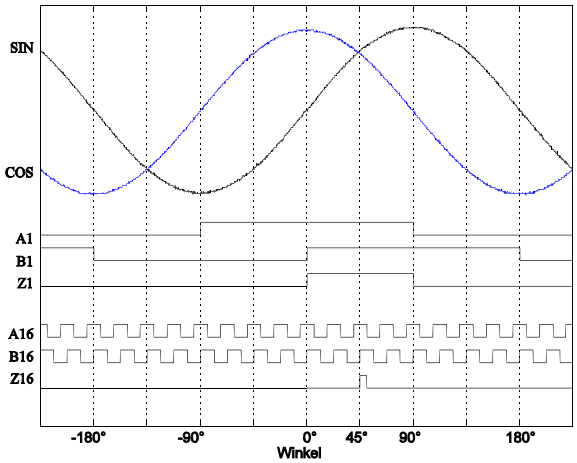


Fig. 4: ROT= hi, COS leading SIN

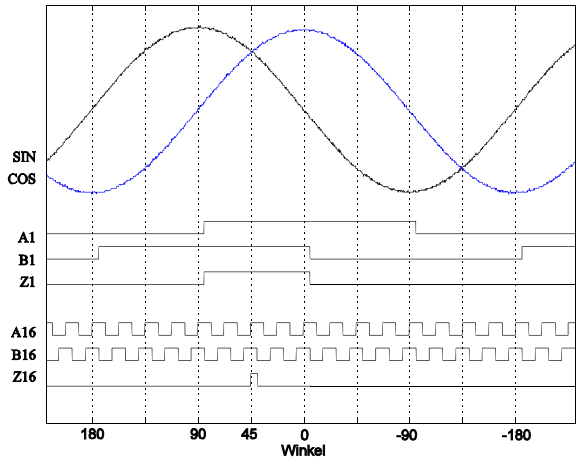


Fig. 5: ROT= hi, SIN leading COS

APPLICATIONS INFORMATION

Basic circuit

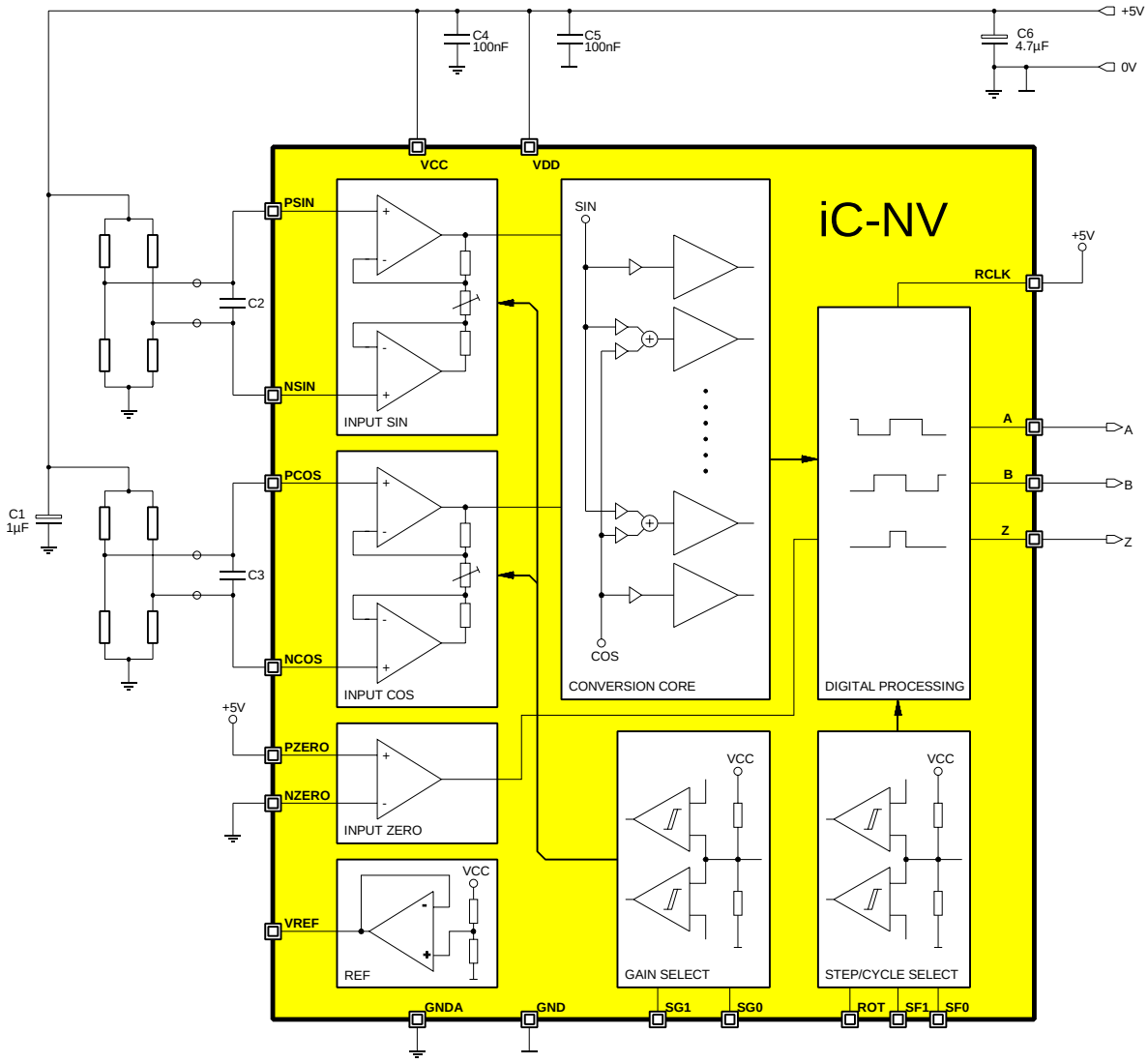


Fig. 6: Basic circuitry for complementary input signals (open setup pins can also be switched to VREF to increase noise immunity).

Possible input circuits

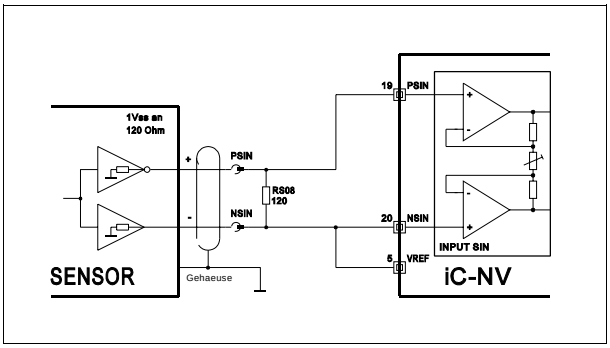


Fig. 7: Input circuit for voltage signals with 1Vpp (separated grounds)

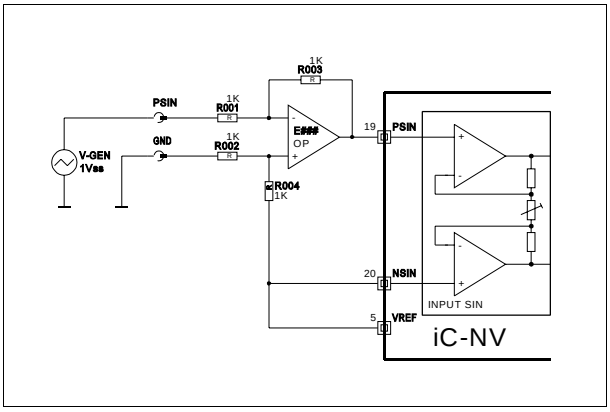


Fig. 8: Input circuit for single ended voltage signals

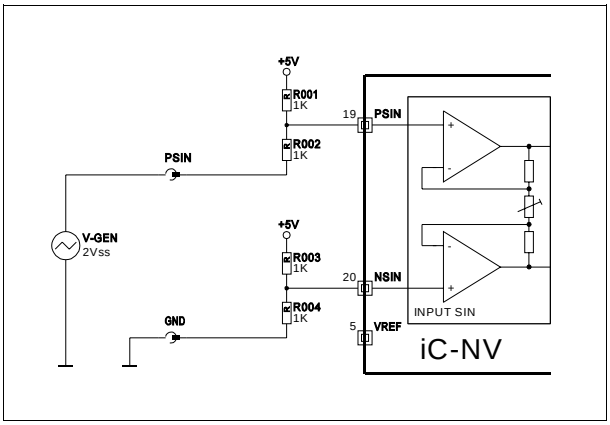


Fig. 9: Input circuit for single ended voltage signals

DEMO BOARD

The iC-NV device is equipped with a Demo Board for test purposes. Figures 10 to 12 show the wiring as well as the top and bottom layout of the test PCB.

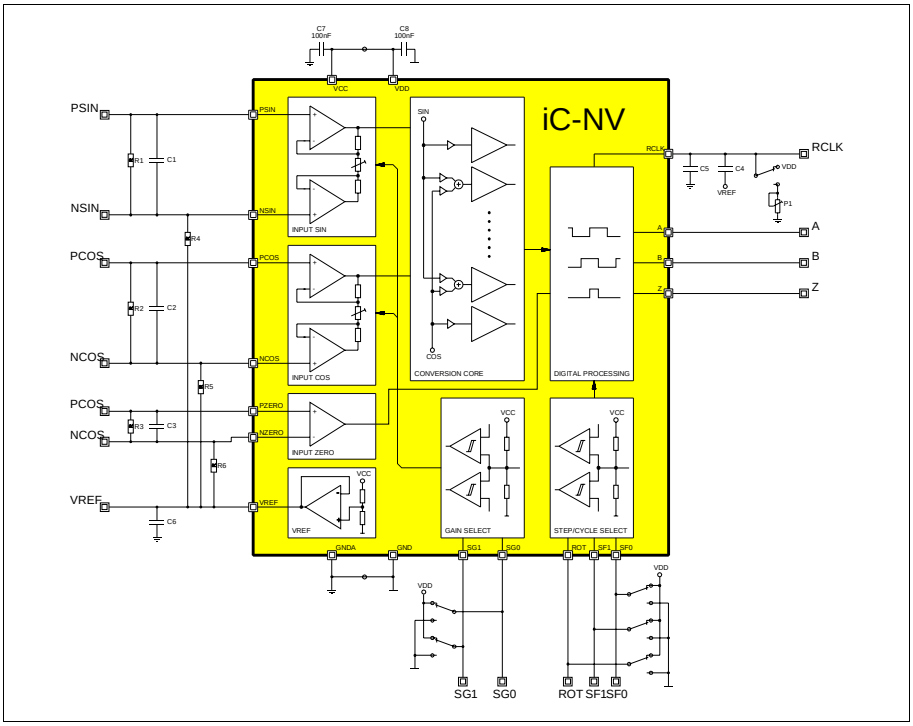


Fig. 10: Circuit diagram of the demo board (delivery comes without pot assembly; the corresponding switch must remain set to high).

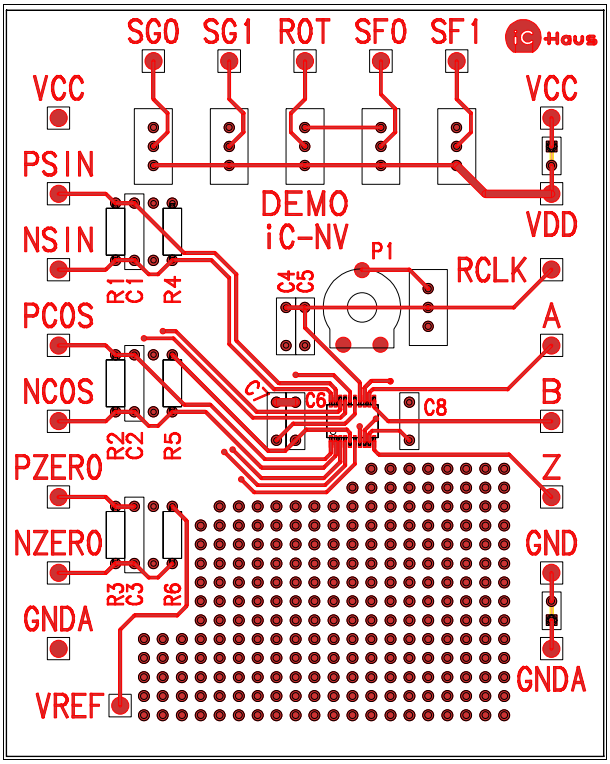


Fig. 11: Demo Board (components side)

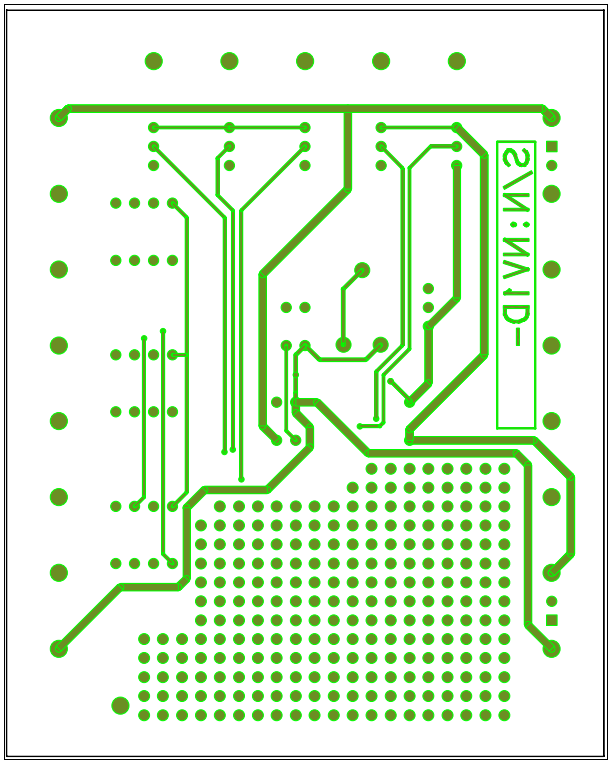


Fig. 12: Demo Board (bottom side)

ORDERING INFORMATION

Type	Package	Order designation
iC-NV	TSSOP20 4.4mm	iC-NV TSSOP20
Demo Board		NV DEMO

For information about prices, terms of delivery, options for other case types, etc., please contact:

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