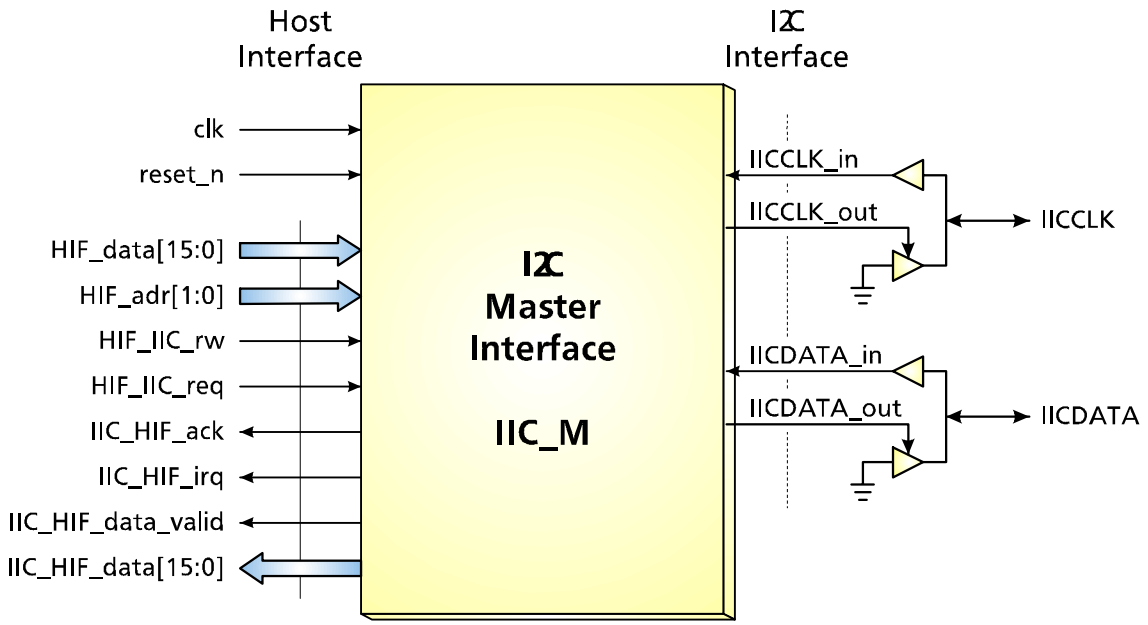
I²C Master Interface



DesignObjects®

Features

- Support of I²C fast-mode up to 400 kHz
- System clock up to 50 MHz
- Reading and writing of data bursts
- Special mode for I²C read and write access to a slave device internal register address
- Wait state generation supported
- Spike filtering

Purpose of the I²C Master Interface

The I²C Master Interface IIC_M provides an interface between a host CPU and an I²C bus. The external components at the I²C bus can be controlled by the host CPU over I²C Master Interface. Basically, the I²C Master Interface is a parallel to serial and serial to parallel converter. The parallel data received from the host CPU has to be converted to a suitable serial form for the external components on the I²C bus. Also the serial data received from the I²C bus has to be converted to a suitable parallel form for the host CPU. The I²C Master Interface also takes care of the interface timing, data structure and error handling.

I²C Master Interface

DesignObjects®

The I²C Master Interface supports four operating modes:

- Direct Write, writing of a data burst
- Direct Read, reading of a data burst
- Random Access Write, writing of one data byte to a specified address
- Random Access Read, reading of one data byte from a specified address

The I²C Master Interface supports both data transfer modes on the I²C bus with data transfer rates up to 100 kbit/s in standard-mode and up to 400 kbit/s in fast-mode.

Interface to Host CPU

The I²C Master Interface includes three register elements for communication between the host CPU and the I²C bus. They are addressed with signal HIF_adr[1:0]:

- Writeable 32 bit data register, HIF_adr[1:0]: 0x0 and HIF_adr[1:0]: 0x1
- Writeable 16 bit configuration register, HIF_adr[1:0]: 0x2
- Readable 16 bit data register, HIF_adr[1:0]: 0x3

DATA Register 32 bit

The 32 bit writeable data register is divided into two 16 bit registers conform to the 16 bit data bus of the host CPU. These two separate parts of the register are called *data_reg_high[15:0]* and *data_reg_low[15:0]*. At the beginning of a read/write access this 32 bit register is loaded with the information from the host CPU needed for the data transfer on the I²C bus. This information consists of 7 bit device code, 8 bit address, 8 bit data and 2 bit for the read or write mode. 7 of the 32 bits are not used. If the device number doesn't change, only the lower part of the data register has to be loaded to start a new data transfer. Data transfer on the I²C bus begins always, when *data_reg_low[15:0]* has been loaded.

Configuration Register

The 16 bit writeable configuration register is needed for some special configuration information, which can be changed by the host CPU. Interrupt masking is one example of that kind of configuration.

Some bits are also used as a reference frequency for the clock signal generation on the I²C bus and programming of the spike filter.

Data Register 16 bit

The 16 bit readable data register contains the 8 bit data received from the I²C bus in Random Access Read mode and Direct Read mode. This register contains also an error bit, an interrupt bit and a write_allowed bit. The error bit is generated (set to '1') if data transfer has failed. If the interrupt bit is set to '1', the register includes new data which has to be read by the host CPU. After the data has been read, the interrupt bit is reset to '0'. When the interrupt signal is disabled (irq bit in configuration register is set to '0'), the interrupt information is request from the host CPU by polling. The interrupt bit in the data register is generated without respect to the irq bit in the configuration register.

The IICCLK signal can be stalled by any I²C device so that no data can be transmitted via the I²C bus. If a proceeding write access has not been completed, the next write access will not be acknowledged. To prevent this, the 16 bit readable data register provides a write_allowed bit. This write_allowed bit is set to '0', if the 32 bit data register is ready for a new write access. The host CPU might read the write_allowed register before a new write access.

Gate Count and RAM Requirements

I²C Master Interface Gate Count Estimation: about 2,000 Gates. No RAM required.

Related Patents

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☐ sci-worx GmbH, Garbsener Landstr. 10, 30419 Hannover, Germany
Phone +49 511 277.1491, fax .2490, web www.sci-worx.com, email info@sci-worx.com

☐ US Office : sci-worx Microelectronics Corp., 1032 Elwell Court, Suite 222, Palo Alto, CA 94303
Phone +1 650 625.1888, fax .1818, web www.sci-worx.com, email info@sci-worx.com

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