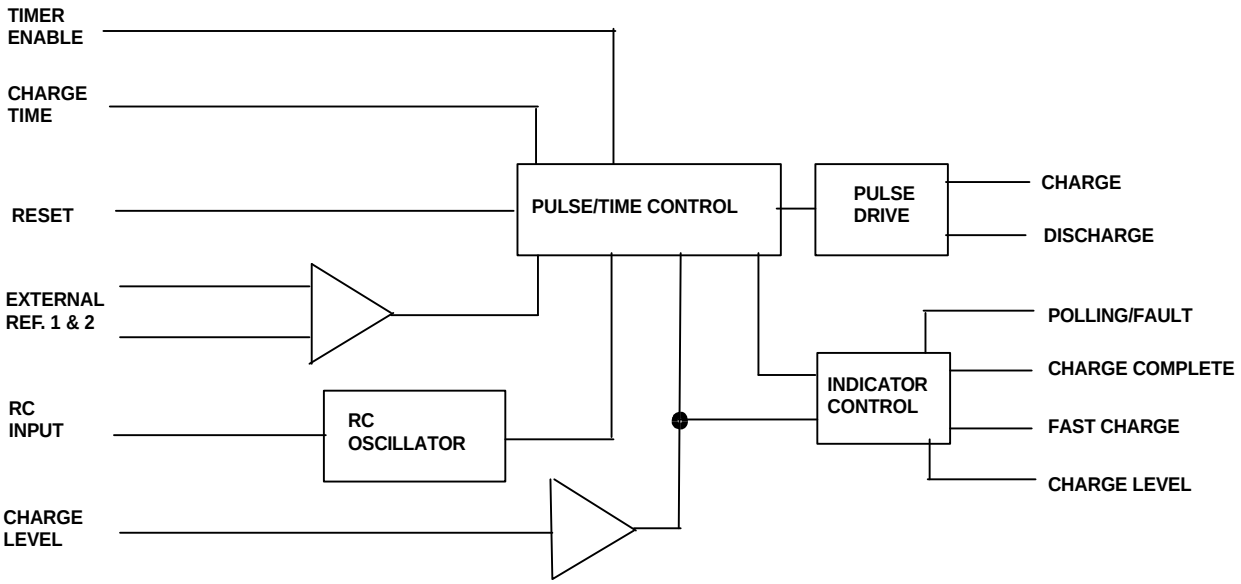
ICS1735
Preliminary/Confidential
Device Information

QuickSaver® Intelligent Conditioning/charge Solution IC for Lead Acid Batteries

General Description

The ICS1735 is a 16 pin 5V CMOS IC that provides a pulse conditioning charge technique for improved fast charge acceptance, reduced recharge time, enhanced battery performance, and extended cycle life. Pulse charge conditioning also reduces stress due to voltage sensitivity by applying a pulsed float and a pulsed maintenance charge stage after the fast charge is complete. The pulsed float and maintenance charge stages replace contemporary lead acid charge methods that maintain charge by impressing a constant float voltage on the battery. The improvements gained by pulse conditioning increase product run time and extend battery service life while providing fast charge convenience and reduced sensitivity to temperature and float voltage variations. These improvements provide greater reliability and less dependency on replacement and spare batteries.

Block Diagram



Four Stage Conditioning Charge Sequence

The normal ICS1735 charging sequence consists of four stages that enables an appropriate external current/voltage regulator to provide pulsed charge to the battery. The first stage is a *SoftStart* conditioning charge which gradually increases the on duty cycle to the current/voltage regulator in the first several minutes after the initiation of a charge. The *SoftStart* stage conditions the battery in preparation for the fast charge stage where a near full duty cycle, discharge pulse conditioning charge is applied. In both stages charge CHG pin 1 simply turns on and off an external current/voltage source. The external current/voltage regulator provides the current and voltage requirements specified by battery manufacturer. The fast charge condition stage continues until the fast conditioning charge timer expires. Fast Charge indicator (FCN) pin 10 is active and low through out the *SoftStart* and fast charge stages.

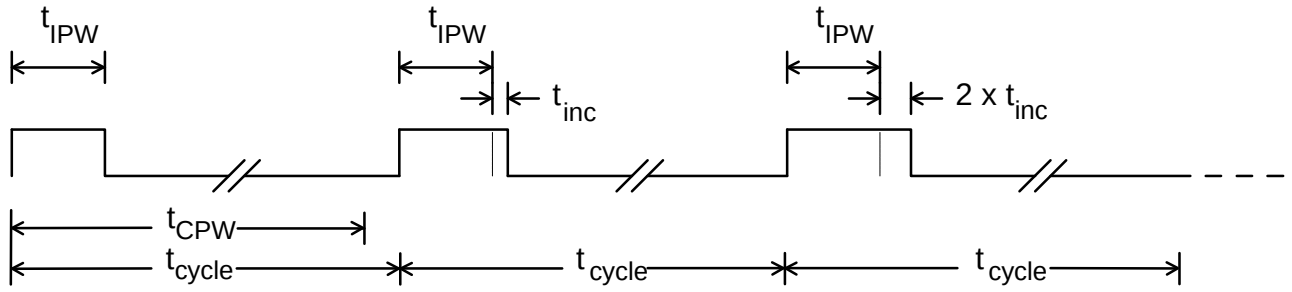
Charge Timer SELect (CTSEL) pin 7 works with external sense circuits to provide a reduced timer setting for batteries over 3/4 full upon initiation of a fast charge. Charge Level Sense (CLS) pin 12 works with external sense circuits to bypass the first two stages of the sequence, to immediately indicate that the battery is already full when charge is initiated. The immediate charge complete indication is provided by Master Charge Indicator (MCN) pin 4. Application circuits are forthcoming as to how to use these two features.

Stage 1: *SoftStart* Conditioning Charge

New unconditioned batteries or batteries that have been over-discharged do not accept charge as readily as those with cells that each have a typical minimal amount of charge. The *SoftStart* stage mitigates this effect by gradually increasing the duty cycle of the external current/voltage regulator at the beginning of charge. The pulse width increases every cycle until the duty cycle applied for the full condition charge pulse width (t_{CPW}) shown below. The *SoftStart* pulse width increases by t_{inc} over 120 cycles that is determined by:

$$t_{inc} = \frac{t_{CPW} - t_{IPW}}{120}.$$

The discharge conditioning pulse mentioned previously is not present during *SoftStart* stage.



Cycle to cycle increase of the *SoftStart* conditioning charge pulse widths.

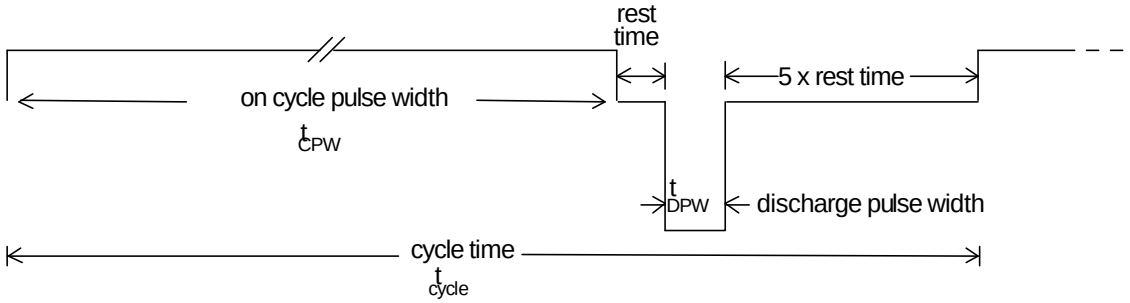
Timing Characteristics

R = 24 kΩ, C= 100 pF with typical tolerances (reduce ranges with lower tolerance R,C)

Parameter	Symbol	Range	Units
Clock Frequency		500 to 700	KHz
Master Reset Pulse Duration		1 to 1.4	Sec
Fast Reset Duration (info on later)		100 to 150	usec
Charge Pulse Width	t_{CPW}	1.3 to 1.8	Sec
Discharge Pulse Width		7.5 to 10	ms
Rest Time	Rest time	6 to 8	ms
Cycle Time	t_{cycle}	1.6 to 2.1	Sec
SoftStart Initial Pulse Width	t_{IPW}	330 to 480	ms
SoftStart Length		3 to 4.25	Min
SoftStart Incremental Pulse Width	t_{inc}	7.5 to 10	ms

Stage 2: Full Condition Charge /Discharge Pulsing

After several minutes the *SoftStart* stage completes, the ICS1735 provides a near full duty cycle output from (CHG) pin 1 in the fast charge stage. In fast charge, brief discharge conditioning pulses are produced by (DCHG) pin 2. These discharge pulses are interleaved between charge enable pulse from (DCHG) pin 2. In fast charge the pulsed technique consists of a relatively long charge pulse, which is supplied to the external voltage/current source from (CHG) pin 1. The brief discharge pulse turns on an external transistor that switches a resistor across the battery.



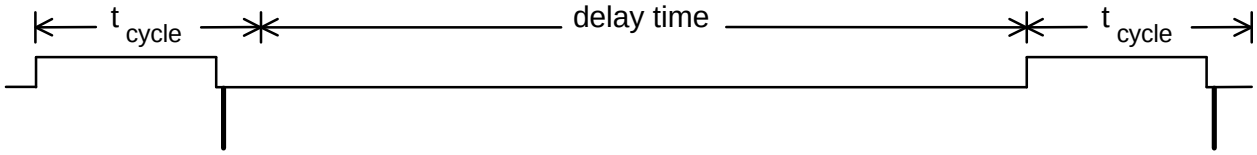
Fast charge conditioning cycle showing charge into (on cycle) and out of the battery (discharge)

The value of the discharge resistor is normally set at the ampere-hour rating of the battery. If the battery is 12 amp hour, the discharge current is set at 12Amps using the battery's nameplate voltage of the discharge resistor.

The discharge pulse is a relatively brief, fixed ratio to the cycle time. The ratio is .00465 or .465% of the cycle time. The external transistor and discharge resistor are relatively small due to the discharge function's low duty cycle. The external transistor is selected based on its pulsed ratings while the resistor is conservatively selected based on the RMS current it carries. Since the discharge current pulse is rectangular, the RMS current is equal to the peak current times the square root of the duty cycle. The RMS current is less 7% of the peak current amplitude.

Stage 3: Pulsed Conditioning Float Charge

The float conditioning charge provides additional opportunity for additional charging for cell balancing as discharge pulse conditioning continues. The ICS1735 conditioning pulsed method accomplished this without the latent stress prolonged constant float voltage charging causes. The float conditioning charge of the same pulsed technique, including the same discharge pulse conditioning used during the fast charge stage except a delay time between the charge pulses is introduced as shown in the diagram below. The duty cycle and time duration of the pulsed float voltage conditioning charge at different rates is given in the section titled *Timer Selection*. The Maintenance Charge indicator (MCN) is active during this stage and the maintenance stage that follows.



Timing diagram for topping and maintenance conditioning charges.

Stage 4: Pulsed Conditioning Maintenance Charge

The conditioning maintenance charge stage offsets the relatively small, natural self-discharge lead acid batteries. The same pulsed technique including the discharge pulse conditioning used during the topping charge stage is used, except the delay between the charge/discharge pulses is once again expanded. The maintenance charge stage maintains the battery at full charge without the added stress constant voltage unidirectional charging causes. The charge complete indicator (CCN) is active throughout this stage.

External Voltage/Current Source Considerations

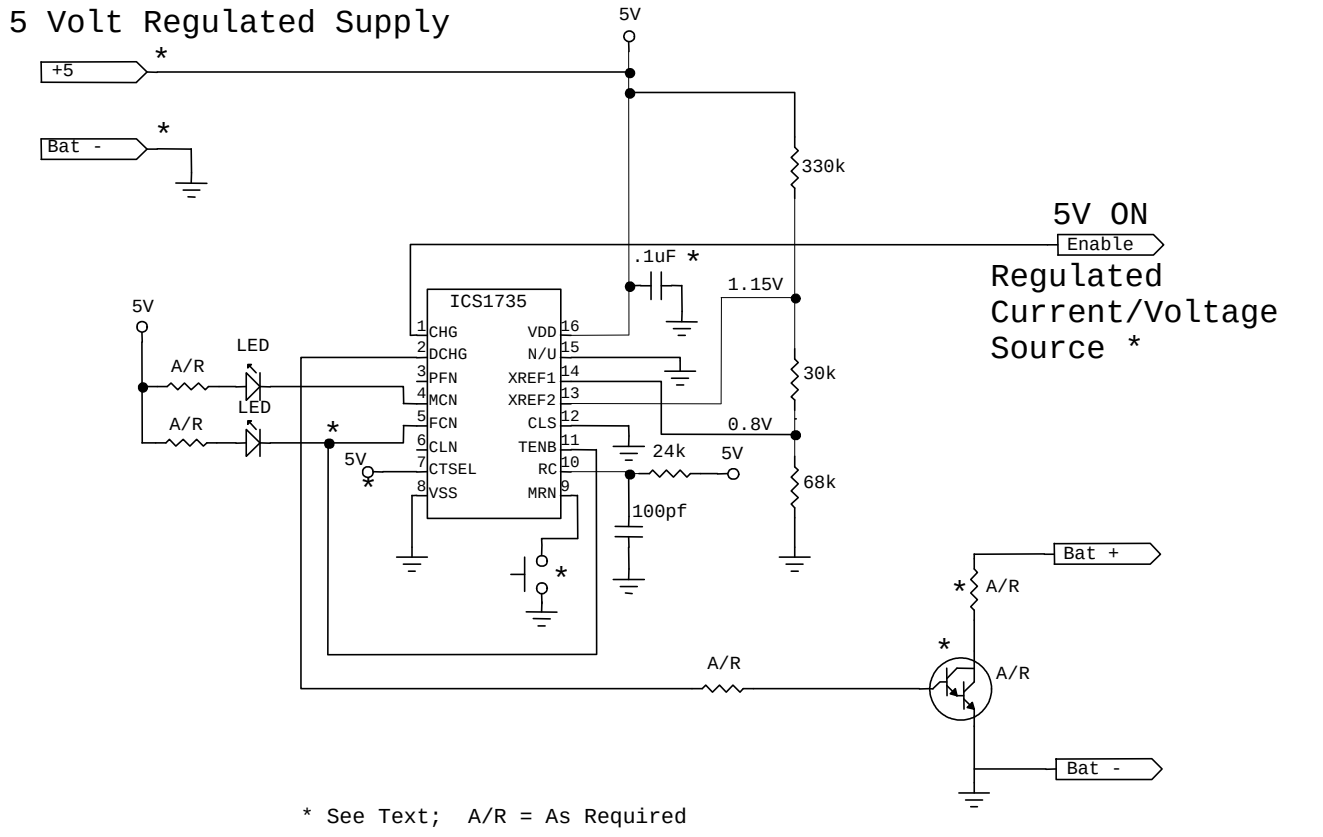
The external current/voltage regulator must provide the current and voltage amplitudes, tolerances, fault protection, etc. as required by the battery manufacturer. The external current/voltage regulator must respond reasonably well and remain stable as it is turned on and off by the ICS1735 charge enable (CHG) pin 1. A logic HIGH (+ 5V) at CHG pin 1 is used to enable ON the external current/voltage regulator. A logic LOW at CHG pin 1 is used to turn off the external current/voltage regulator. Appropriate interface circuits may be required for level shifting and logic reversal depending on the current/regulator configuration.

Battery Detection

The following options can be used to detect the presence of a battery. The simplest and often times least expensive method involves using a small push button switch to start fast charge. The push button switch holds MRN pin 9 at ground when depressed which holds the ICS1735 in reset, keeping the external current/voltage regulator off. As long as MRN pin 9 is held at ground, all ICS1735 outputs stay in their off state: pins 1 and 2 are low, pins 3 through 6 are +5V with an external pull up resistor. When the push button is released, MRN pin 9 is released and the ICS1735 starts the four stage pulse charge sequence mentioned previously. The push button approach is shown in the ICS1735 BASIC EVALUATION CIRCUIT DIAGRAM below.

ICS1735 Evaluation Information

The circuit diagram below is for evaluating the benefit of reduced capacity fade the ICS1735 provides a charging system for charging lead acid batteries. The circuit as shown will not perform any special functions such as electronic battery detection, immediate indication of an already full battery, indication that the battery is over more than 2/3rd full, etc. These functions re quire additional external sense circuits. Information will be provided at a later date. The ICS1735 in the circuit below is configured to run a full condition charge for 2 ¼ hours followed by the topping and maintenance conditioning charges previously mentioned. The 2¼ hours may be decreased approximately 20% to about 2 hours by changing the 24KΩ RC pin timing resistor to 20KΩ. Similarly, the 2 ¼ hours may be increased by 25% to about 2.75 hours by changing the 24KΩ 30KΩ.



ICS1735 BASIC EVALUATION CIRCUIT

Pin Identification, Type and Description

Pin	ID	*Type	Description
1	CHG	OUTPUT	Logic HIGH (PFET from +5V) and LOW (BFET to battery -) 16Ω, 25mA max. drive turns on and off an external current/voltage regulator providing pulse charging.
2	DCHG	OUTPUT	Logic HIGH (PFET from +5V) and LOW (BFET to battery -) 16Ω, 25mA max. drive turns on and off an external current/voltage regulator providing pulse charging.
3	PFN	OUTPUT	Polling /Fault indicator. NFET drain rated at 10Ω, 40 mA max. provides logic LOW (battery -) to turn on external indicator for missing battery or an open circuit.
4	MCN	OUTPUT	Maintenance Charge indicator. NFET drain rated at 10Ω, 40 mA max. provides LOW to (battery -) turn on external indicator when the battery is near full (info later) or when fast charge is complete and the topping and maintenance condition charge is in progress.
5	FCN	OUTPUT	Fast Charge indicator. NFET drain rated at 10Ω, 40 mA max. provides logic LOW to (battery -) turn on external indicator indicating fast charge is in progress.
6	CLN	OUTPUT	Charge Level indicator. NFET drain rated at 10Ω, 40 mA max provides logic LOW to (battery -) to activate a reduced timed charge, indicate approximate battery charge level, and assist with battery detection. (information to be provided later)
7	CTSEL	INPUT	High Impedance tri-state input for setting fast charge timer. CTSEL input can be mechanically or electronically set. Left open circuit, CTSEL floats to 2.3V. For a logic HIGH, a pull up to VDD is required. For a logic LOW, CTSEL is grounded.
8	VSS	GROUND	The return or ground of the 5V supply and battery are connected to VSS providing ground for all logic, output driver, analog, and output indicator circuits.
9	MRN	INPUT	Master Reset input has an internal pull-up of 75 kΩ. A logic LOW to battery - on the MRN pin shuts down the ICS1735, releasing MRN restarts the ICS1735. An internal power-up reset automatically occurs at initial power up. Debouncing for switch applications is provided internally.
10	RC	INPUT	Sets the frequency on the internal clock. Typically 24 kΩ is connected between this pin and V_{DD} and a 100 pF capacitor is connected between this pin and ground.
11	TENB	INPUT	Timer Enable sets the fast charge stage timer.
12	CLS	INPUT	Charge Level Sense. Uses external sense circuit to indicate approximate charge level.
13	XREF1	INPUT	External voltage reference provides means to detect the presence of a battery.
14	XREF2	INPUT	External voltage reference provides means to detect the presence of a battery.
15	N/U	Not Unused	Connect to ground
16	VDD	INPUT	+5 VDC +/- 5% is rated for 80mA minimum is recommended. The maximum average current demand for the device alone is 11mA that includes very brief 50mA peak currents. When used LEDs require additional current since they should be powered from the VDD supply. A .1uf bypass is required, as is a 4.7uf electrolytic capacitor whenever the +5VDC regulators output capacitors not close to VDD pin 16.

***** Input and output pins all have internal ESD protection diodes to VDD and VSS for 2KV protection per MIL STD 883 method 3015.7. Depending on the application, set-up, board layout, etc. additional ESD protection may be required

Fast Charge Timer Selections, Pulsed Float and Maintenance ON and OFF Times

R = 24 kΩ, C= 100 pF with typical tolerances (range below can be reduced using lower tolerance devices for R and/or ,C)

CTSEL	Fast Charge Timer	Float Charge Cycle (Time Duration **)	Maintenance Charge Cycle
L	*30 to 40 min	1 pulse on, off for 41 pulse durations (3.3 Hrs)	1 pulse on, off for 161 pulse durations
H	110 to 145 min	1 pulse on, off for 11 pulse durations (3.3 Hrs)	1 pulse on, off for 41 pulse durations
Z	300 to 400 min	1 pulse on, off for 4 pulse durations (3.3 Hrs)	1 pulse on, off for 16 pulse durations

* Note: The 30 to 40 minute charge time option is intended primarily for charging a battery that is over 3/4 full. Charging a battery from empty to full in this short period of time involves special consideration.

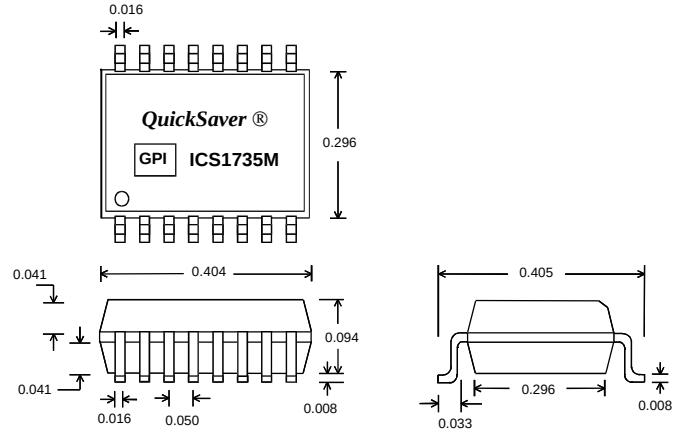
** 3.3 Hr +/- 1/2 Hr with a 24KΩ timing resistor. Increasing or decreasing the clock rate by varying the value of the timing resistor to alter the time duration of the fast charge stage correspondingly decreases or increases the float charge duration.

Absolute Maximum Ratings

Supply Voltage	6.5	V
Logic Input Levels	-0.5 to V_{DD} + 0.5	V
Ambient Operating Temperature	85	°C
Storage Temperature	-55 to 150	°C

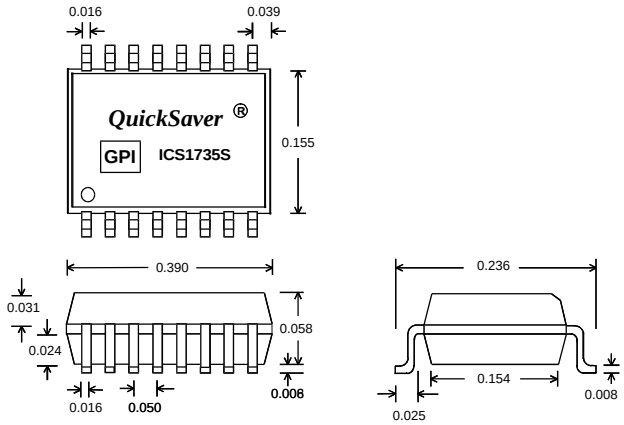
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those listed in this document is not implied. Exposure to absolute maximum rating conditions for extended periods will affect product reliability.

Package



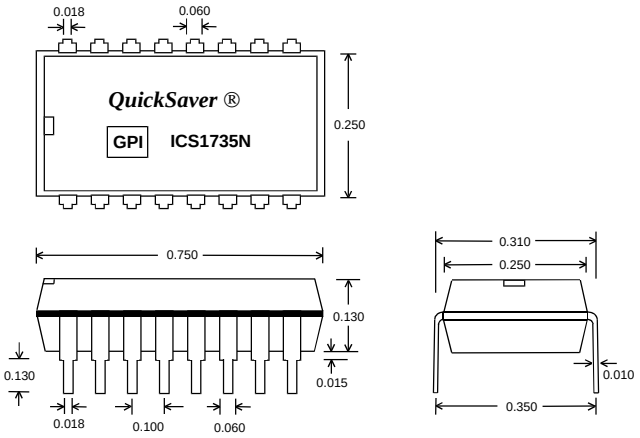
All package dimensions are in inches.

16-Pin SOIC Package (300 mil)



All package dimensions are in inches.

16-Pin SOIC Package (150 mil)



All package dimensions are in inches.

16-Pin DIP package (300 mil)

Ordering Information:
ICS1735M, ICS1735MT,
ICS1735S, ICS1735ST, ICS1735N

Example:
ICS 1735 ST

Package type: N= DIP (Plastic)
M= 300 mil SOIC
S= 150 mil SOIC
MT= 300 mil SOIC Tape and Reel
ST= 150 mil SOIC Tape and Reel

Device type: Consists of 3 to 5 digits or numbers

Prefix: ICS = Intelligent Charging Solution standard device

IMPORTANT NOTICE

Galaxy Power, Inc. (GPI) makes no claims about the capability of any battery to accept a fast charge. GPI strongly recommends that the battery manufacturer be consulted before fast charging. GPI shall be held harmless for any misapplication of this device such as: exceeding the rated specifications of the battery manufacturer; personal or product damage caused by the he charging device, circuit, or system itself; unsafe use, application, and/or manufacture of a charge system using this device.

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