PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8302

LOW SKEW, 1-TO-2 LVCMOS / LVTTL FANOUT BUFFER

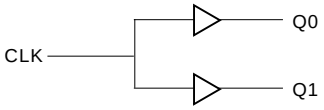
GENERAL DESCRIPTION

The ICS8302 is a low skew, 1-to-2 LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8302 has a single ended clock input. The single ended clock input accepts LVCMOS or LVTTL input levels. The ICS8302 features a pair of LVCMOS outputs. The ICS8302 is characterized at full 3.3V for input V_{DD}, and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the ICS8302 ideal for clock distribution applications demanding well defined performance and repeatibility.

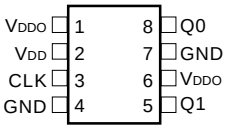
FEATURES

- 2 LVCMOS / LVTTL outputs
- LVCMOS clock input accepts LVCMOS or LVTTL input levels
- Maximum output frequency: 350MHz
- Output skew: 25ps (typical)
- Part-to-part skew: 250ps (typical)
- Small 8 lead SOIC package saves board space
- Full 3.3V or 3.3V core, 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8302
8-Lead SOIC
3.8mm x 4.8mm, x 1.47mm package body
M Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 6	V_{DDO}	Power		Output supply pins. Connect to 3.3V or 2.5V.
2	V_{DD}	Power		Positive supply pin. Connect to 3.3V.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4,7	GND	Power		Power supply ground. Connect to ground.
5	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V		23		pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			7		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			11		mA
I_{DDO}	Output Supply Current			2		mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		1.3	V
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				350	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq$ 350MHz		2.35	2.8	ns
*t*sk(o)	Output Skew; NOTE 2, 4			25	100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			250	600	ps
t_R	Output Rise Time	30% to 70%	300		800	ps
t_F	Output Fall Time	30% to 70%	300		800	ps
odc	Output Duty Cycle	$f \leq$ 200MHz	40		60	%

All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 3C. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			11		mA
I_{DDO}	Output Supply Current			2		mA

TABLE 3D. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		1.3	V
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

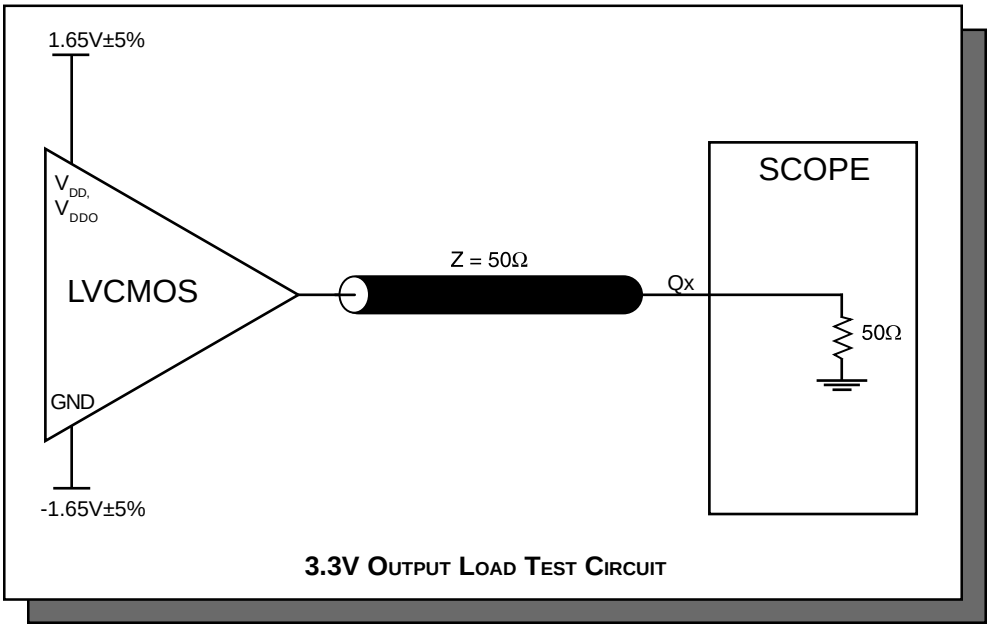
NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information Section, "3.3V/2.5V Output Load Test Circuit".

TABLE 4B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

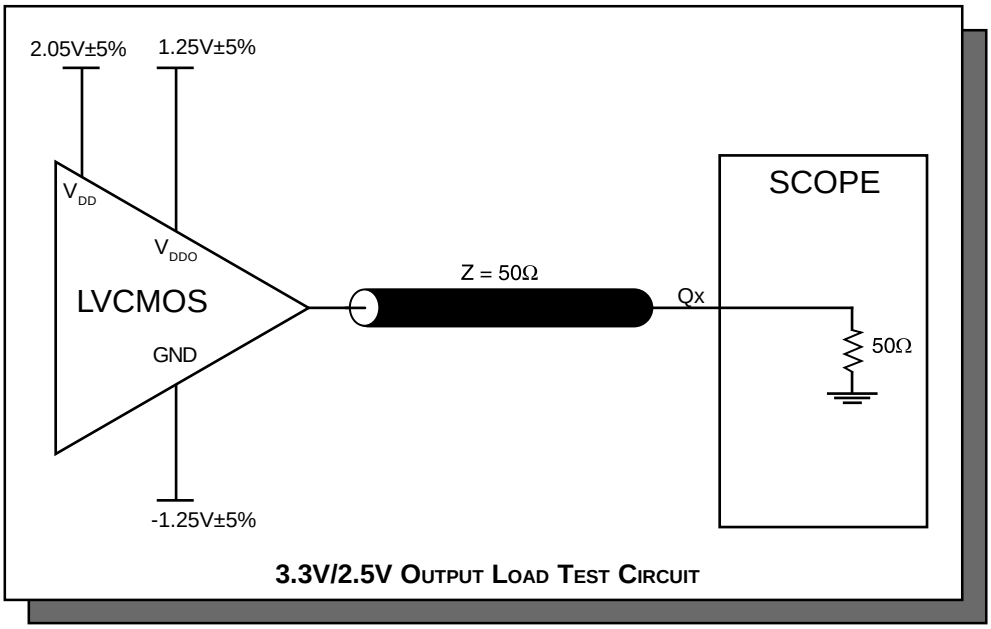
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			TBD		MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			TBD		ns
*t*sk(o)	Output Skew; NOTE 2, 4			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
t_R	Output Rise Time	30% to 70%		TBD		ps
t_F	Output Fall Time	30% to 70%		TBD		ps
odc	Output Duty Cycle			TBD		%

All parameters measured at TBD unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

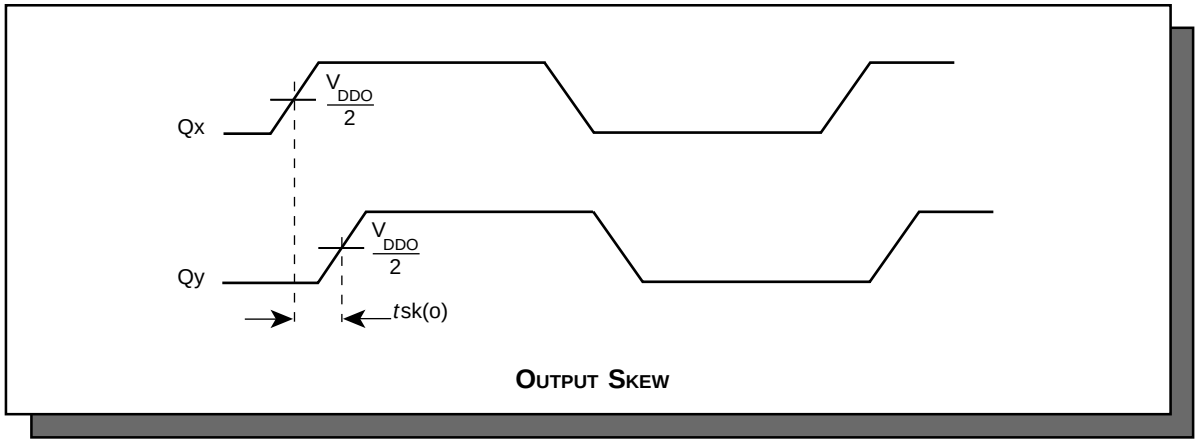
PARAMETER MEASUREMENT INFORMATION



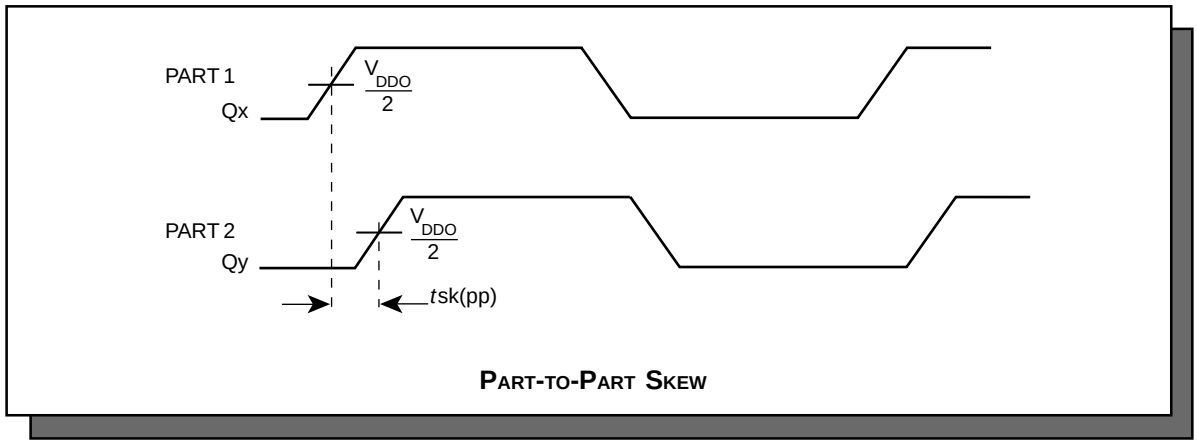
3.3V OUTPUT LOAD TEST CIRCUIT



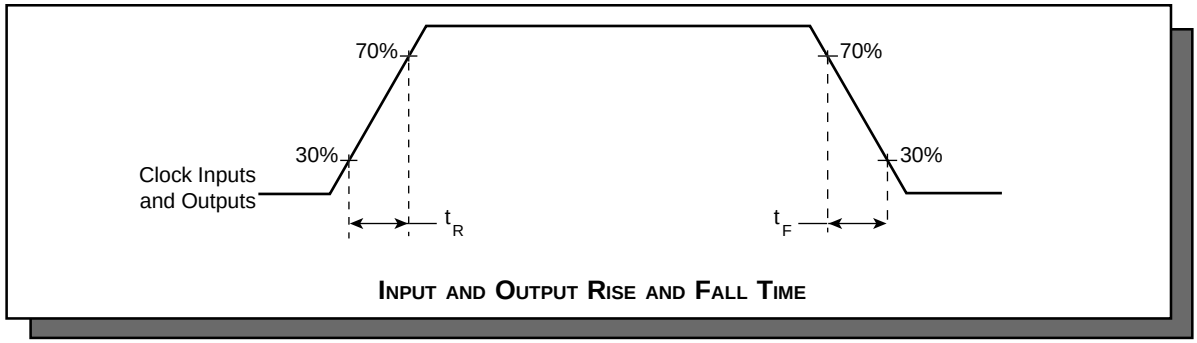
3.3V/2.5V OUTPUT LOAD TEST CIRCUIT



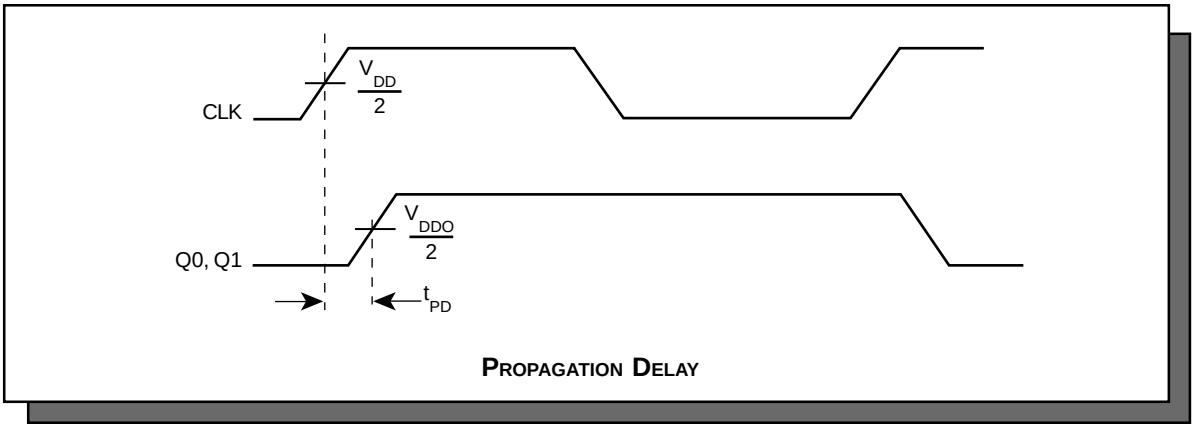
OUTPUT SKEW



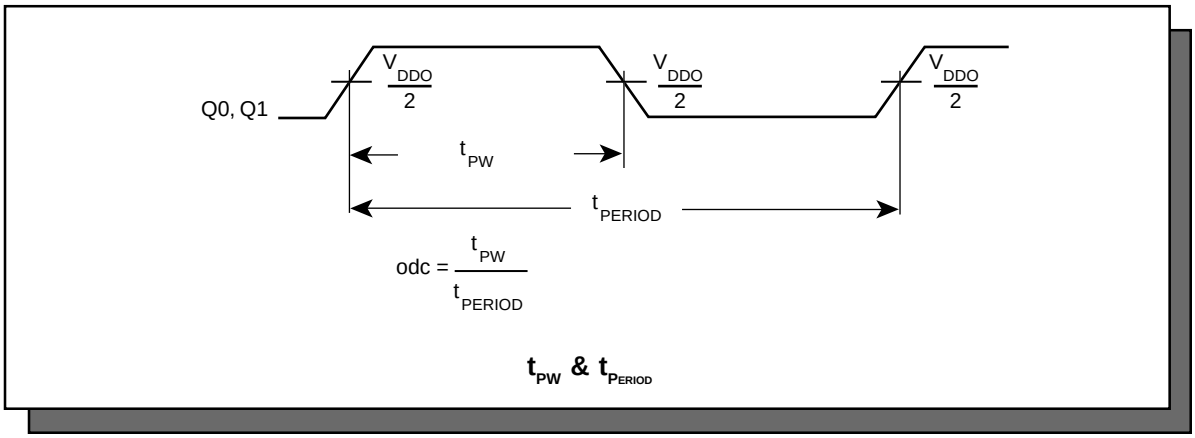
PART-TO-PART SKEW



INPUT AND OUTPUT RISE AND FALL TIME



PROPAGATION DELAY



t_{PW} & t_{PERIOD}

TABLE 5. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8302 is: 322

PACKAGE OUTLINE - SUFFIX M

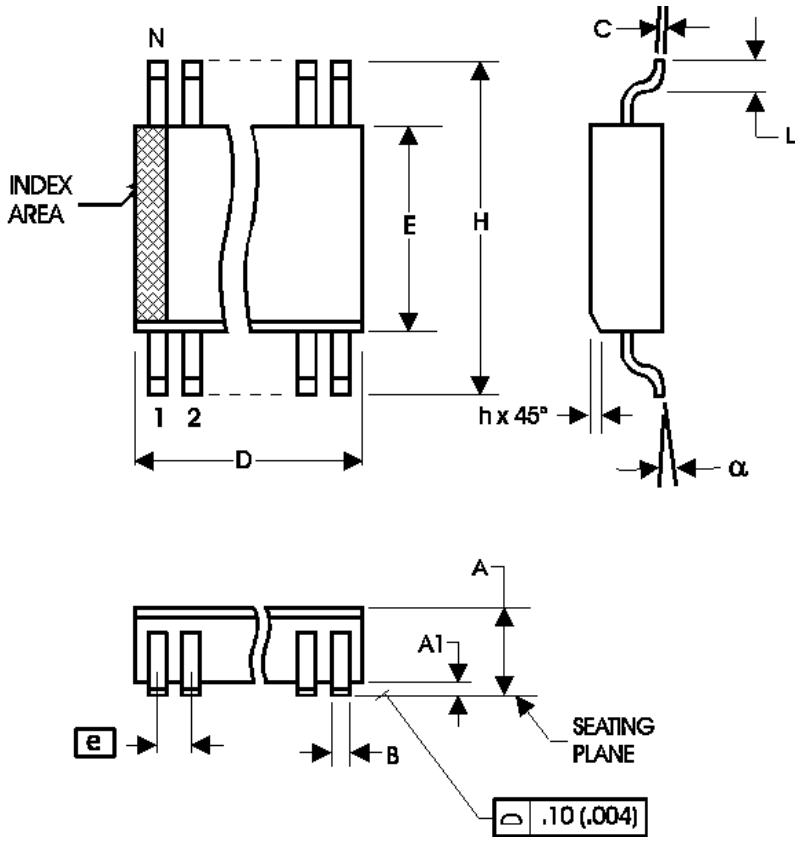


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8302AM	8302AM	8 lead SOIC	96 per tube	0°C to 70°C
ICS8302AMT	8302AM	8 lead SOIC on Tape and Reel	2500	0°C to 70°C