



2.5V Wide Range Frequency Clock Driver (33MHz - 233MHz)

Recommended Application:

Zero Delay Board Fan Out

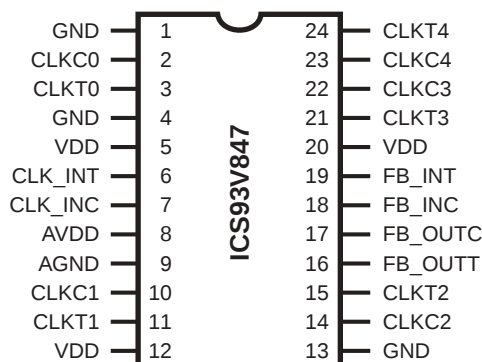
Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 5 differential clock distribution (SSTL_2)
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs

Switching Characteristics:

- Period jitter (>66MHz): <40ps
- CYCLE - CYCLE jitter (66MHz): <120ps
- CYCLE - CYCLE jitter (>100MHz): <65ps
- OUTPUT - OUTPUT skew: <60ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

Pin Configuration



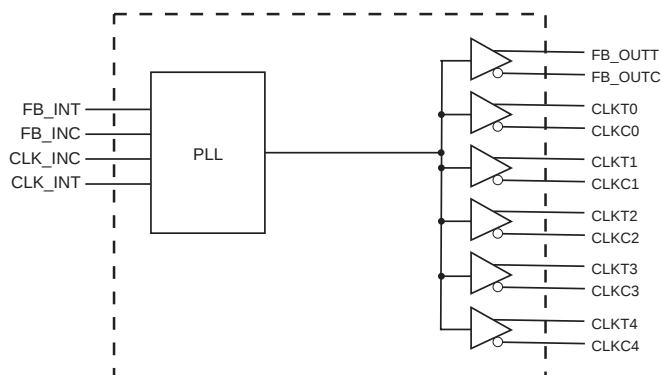
24-Pin TSSOP

4.40 mm. Body, 0.65 mm. pitch

Functionality

INPUTS			OUTPUTS				PLL State
AVDD	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	L	H	L	H	L	H	Bypassed/off
GND	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	H	L	H	L	H	on
2.5V (nom)	H	L	H	L	H	L	on

Block Diagram



ICS93V847

Advance Information



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
5, 12, 20	VDD	PWR	Power supply 2.5V
1, 4, 13	GND	PWR	Ground
8	AVDD	PWR	Analog power supply, 2.5V
9	AGND	PWR	Analog ground.
3, 11, 15, 21, 24	CLKT(4:0)	OUT	"True" Clock of differential pair outputs.
2, 10, 14, 22, 23	CLKC(4:0)	OUT	"Complementary" clocks of differential pair outputs.
6	CLK_INT	IN	"True" reference clock input
7	CLK_INC	IN	"Complementary" reference clock input
16	FB_OUTT	OUT	"True" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
17	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
19	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
18	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.

This PLL Clock Buffer is designed for a V_{DD} of 2.5V, an AV_{DD} of 2.5V and differential data input and output levels.

The ICS93V847 is a zero delay buffer that distributes a differential clock input pair (CLK_INT, CLK_INC) to five differential pair of clock outputs (CLKT(4:0), CLKC(4:0)) and one differential pair feedback clock output (FB_OUT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INT, CLK_INC), the feedback clocks (FB_INT, FB_INC) and the Analog Power input (AV_{DD}). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

The PLL in ICS93V847 clock driver uses the input clocks (CLK_INC, CLK_INT) and the feedback clocks (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter output differential clocks (CLKT(4:0), CLKC(4:0)). ICS93V847 is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

ICS93V847 is characterized for operation from 0°C to 85°C.



Absolute Maximum Ratings

Supply Voltage (VDD & AVDD)	-0.5V to 4.6V
Logic Inputs	GND -0.5 V to V _{DD} +0.5 V
Ambient Operating Temperature	0°C to +85°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I _{IH}	V _I = V _{DD} or GND	5			μA
Input Low Current	I _{IL}	V _I = V _{DD} or GND			5	μA
Operating Supply Current	I _{DD2.5}	C _L = 0pf				mA
	I _{DDPD}	C _L = 0pf			90	mA
Input Clamp Voltage	V _{IK}	V _{DD} = 2.3V I _{in} = -18mA			-1.2	V
High-level output voltage	V _{OH}	I _{OH} = -1 mA	V _{DD} -0.1			V
		I _{OH} = -12 mA	1.7			V
Low-level output voltage	V _{OL}	I _{OL} = 1 mA			0.1	V
		I _{OH} = 12 mA			0.6	V
Input Capacitance ¹	C _{IN}	V _I = GND or V _{DD}		3		pF
Output Capacitance ¹	C _{OUT}	V _{OUT} = GND or V _{DD}		3		pF
Output differential-pair crossing voltage	V _{OC}		(V _{DD} /2) -0.2		(V _{DD} /2) +0.2	V

¹Guaranteed by design at 233MHz, not 100% tested in production.

**Recommended Operating Condition** (see note1)
 $T_A = 0 - 85^{\circ}\text{C}$; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DDQ}, A_{VDD}		2.3		2.7	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_INT, FB_INC		0.4	$V_{DD}/2 - 0.18$	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_INT, FB_INC	$V_{DD}/2 + 0.18$	0.21		V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD}	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLK_INT, CLK_INC, FB_INT, FB_INC	0.36		$V_{DD} + 0.6$	V
		AC - CLK_INT, CLK_INC, FB_INT, FB_INC	0.7		$V_{DD} + 0.6$	V
Output differential cross-voltage (note 4)	V_{OX}		$V_{DD}/2 - 0.15$		$V_{DD}/2 + 0.15$	V
Input differential cross-voltage (note 4)	V_{IX}		$V_{DD}/2 - 0.2$		$V_{DD}/2 + 0.2$	V
High level output current	I_{OH}				-12	mA
Low level output current	I_{OL}				12	mA
High Impedance Output Current	I_{OZ}	$V_{DD}=2.7\text{V}$, $V_{out}=V_{DD}$ or GND		0.1	± 10	mA
Operating free-air temperature	T_A		0		85	$^{\circ}\text{C}$

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VTR is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.



Timing Requirements

$T_A = 0 - 85^\circ\text{C}$; Supply Voltage AVDD, VDD = 2.5 V $\pm$ 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$f_{req_{op}}$	2.5V $\pm$ 0.2V @ 25°C	33	233	MHz
Application Frequency Range	$f_{req_{App}}$	2.5V $\pm$ 0.2V @ 25°C	60	170	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			100	μs

Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}^1	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	t_{PHL}^1	CLK_IN to any output		5.5		ns
Jitter period	$t_{jit(per)}$	66/100/125/133/167MHz	-40		40	ps
Half-period jitter	$t_{jit(hper)}$	100/133/167MHz	-100		100	
Input clock slew rate	$t_{sl(I)}$		1		4	
Output clock slew rate	$t_{sl(O)}$		1		4	
Cycle to Cycle Jitter ¹	$t_{cyc-t_{cyc}}$	66/100/125/133/167MHz			60	ps
Phase error	$t_{(phase\ error)}^4$		-50	0	50	ps
Output to Output Skew	t_{skew}			40	60	ps
Rise Time, Fall Time	t_r, t_f	Load = 120W/16pF	650	800	950	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle= t_{WH}/t_c , where the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.



Parameter Measurement Information

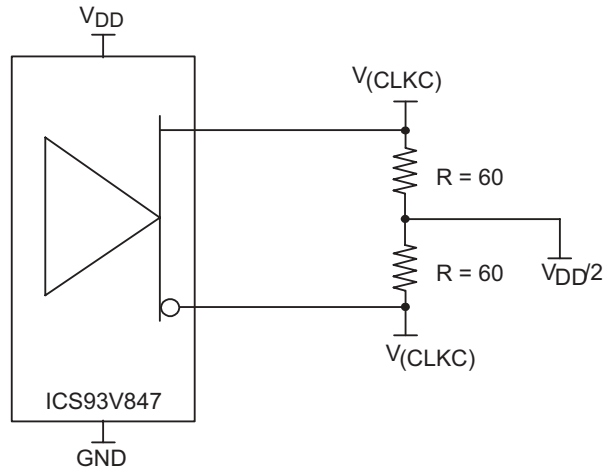
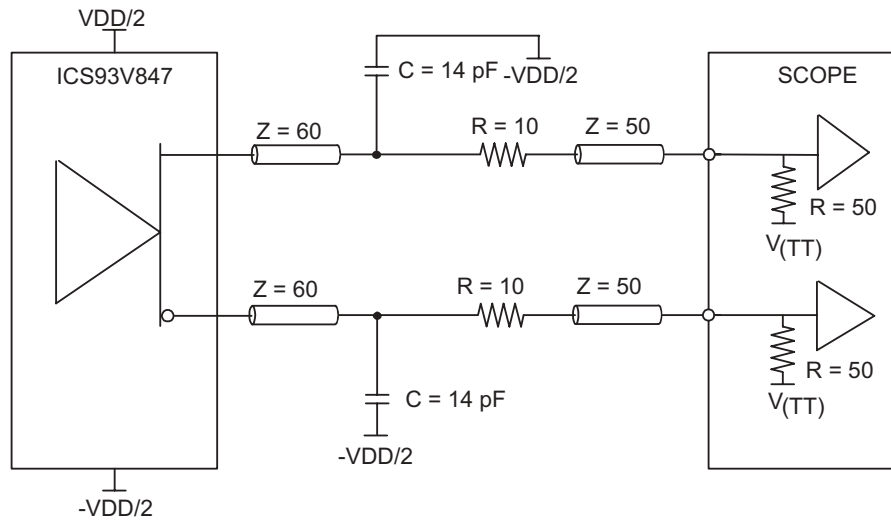


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)} = \text{GND}$

Figure 2. Output Load Test Circuit

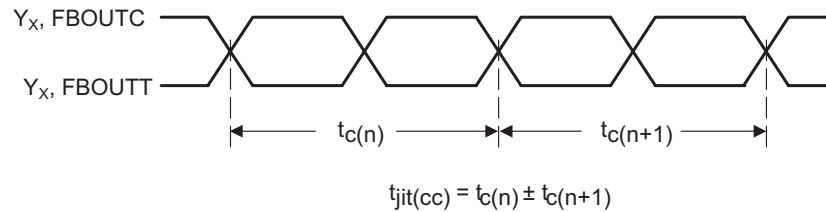


Figure 3. Cycle-to-Cycle Jitter



Parameter Measurement Information

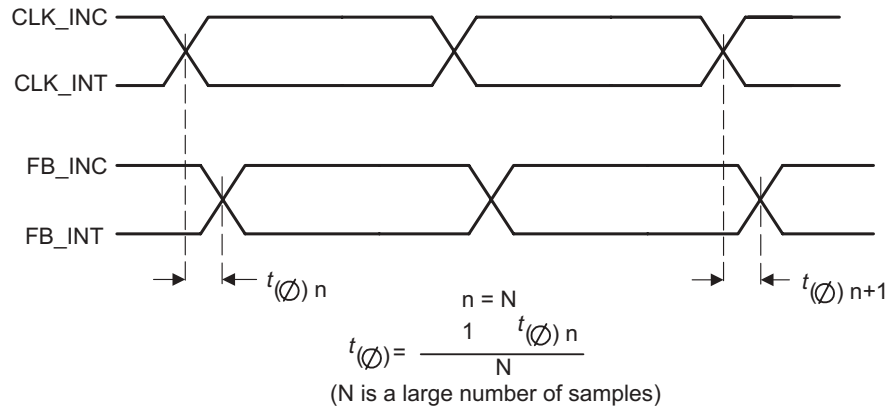


Figure 4. Static Phase Offset

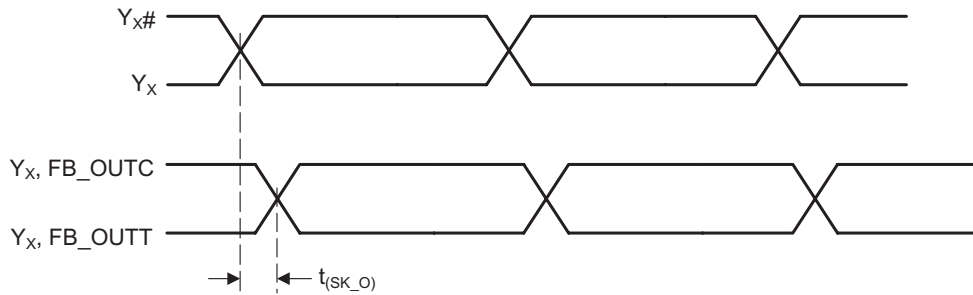


Figure 5. Output Skew

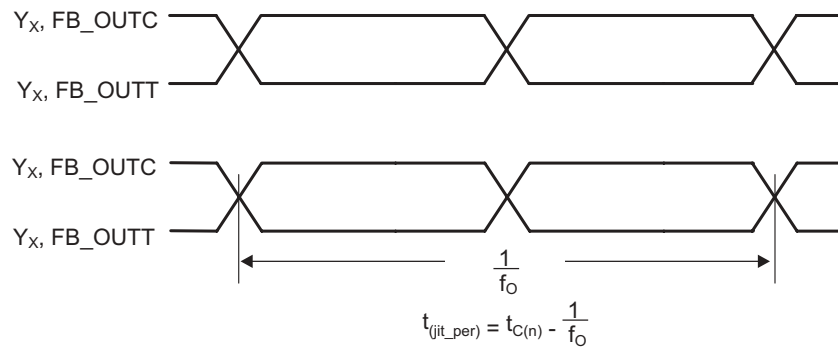


Figure 6. Period Jitter



Parameter Measurement Information

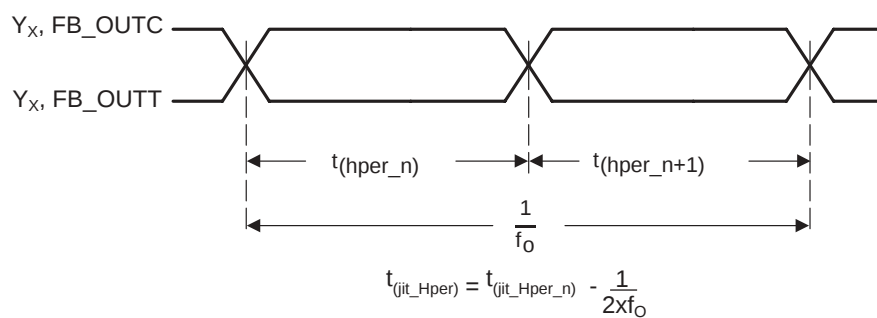


Figure 7. Half-Period Jitter

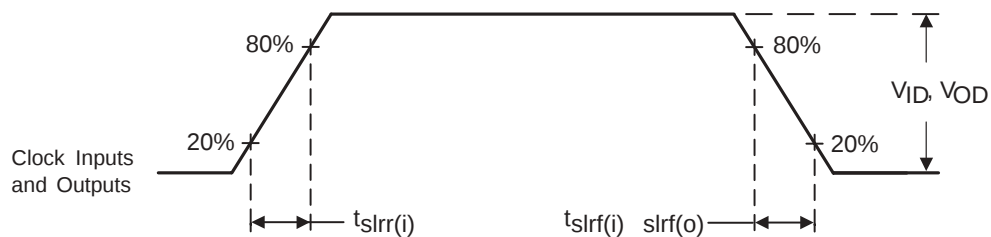
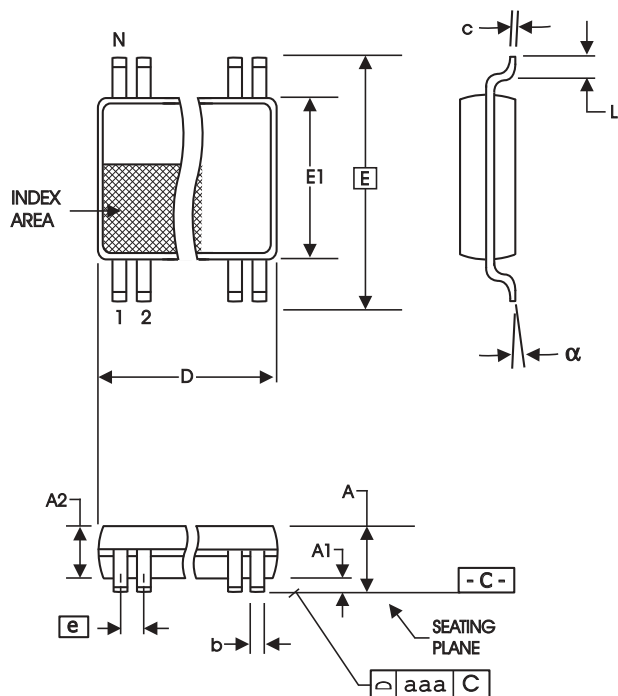


Figure 8. Input and Output Slew Rates



ICS93V847

Advance Information



SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
24	7.70	7.90	.303	.311

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

Ordering Information

ICS93V847yG-T

Example:

ICS XXXX y G - PPP - T

Designation for tape and reel packaging

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

G=TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix

ICS = Standard Device