



HIGH-SPEED CMOS QUAD 2-INPUT MULTIPLEXER

IDTQS74FCT158AT/CT

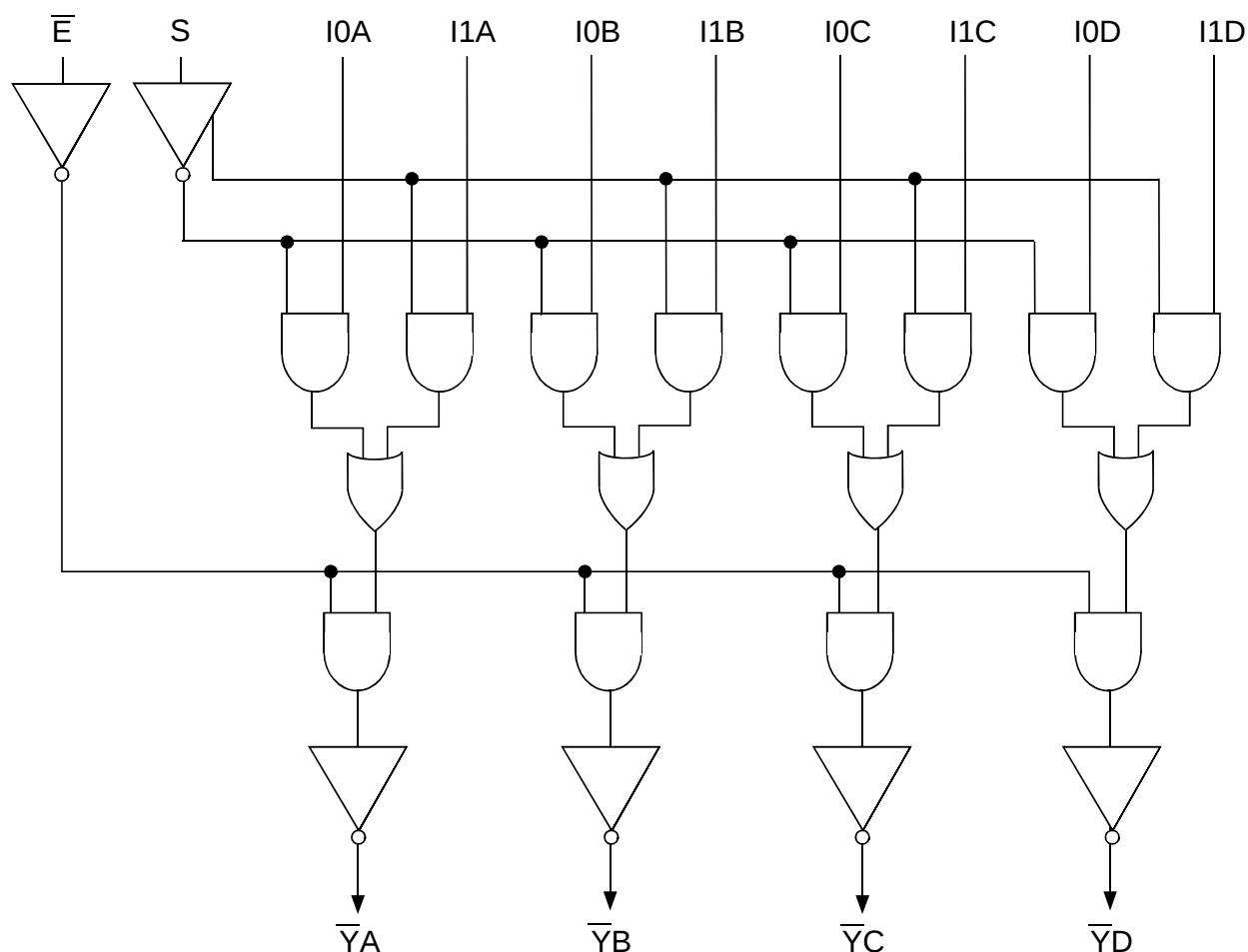
FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- A and C grades with 4.3ns for C
- $I_{OL} = 48\text{mA}$
- Available in QSOP package

DESCRIPTION:

The IDTQS74FCT158T is a high-speed CMOS TTL-compatible, quad, 2-input multiplexer. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM

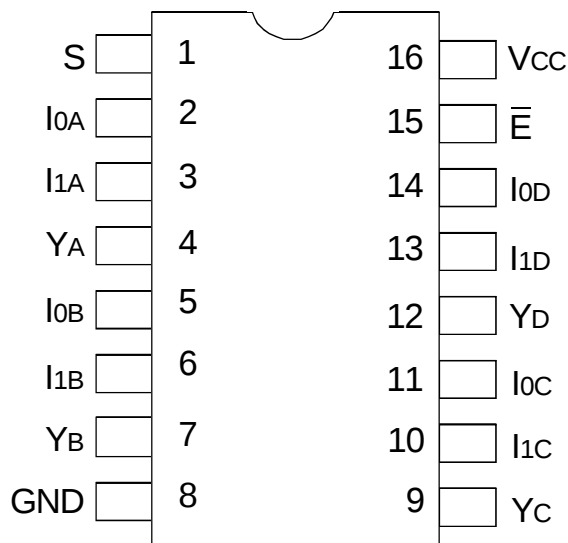


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INDUSTRIAL TEMPERATURE RANGE

JANUARY 2004

PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current Max Current Sink/Pin	+120	mA
I _{IK}	Input Diode Current, V _{IN} < 0	-20	mA
I _{OK}	DC Output Current, V _{OUT} < 0	-50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4	—	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	—	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I _{xx}	Data Inputs
S	Select Input
E-bar	Enable Input
Y _A - Y _D	Data Outputs

FUNCTION TABLE⁽¹⁾

Inputs						Function
E-bar	S	Y _A	Y _B	Y _C	Y _D	
H	X	H	H	H	H	Disable
L	L	I _{0A}	I _{0B}	I _{0C}	I _{0D}	Select 0
L	H	I _{1A}	I _{1B}	I _{1C}	I _{1D}	Select 1

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
ΔV _T	Input Hysteresis	V _{TLH} - V _{THL} for all inputs		—	0.2	—	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	0 ≤ V _{IN} ≤ V _{CC}	—	—	±5	μA
I _{IL}	Input LOW Current						
I _{OS}	Short Circuit Current	V _{CC} = Max., V _{OUT} = GND ⁽²⁾		−60	—	—	mA
V _{IC}	Input Clamp Voltage	V _{CC} = Min., I _{IN} = −18mA, T _A = 25°C ⁽²⁾		—	−0.7	−1.2	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = −15mA	2.4	—	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 48mA	—	—	0.5	V

NOTES:

- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ $\text{freq} = 0$	—	2	mA
I_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/ MHz

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under DC Electrical Characteristics.
 - Per TTL driven input ($V_{IN} = 3.4\text{V}$).
 - For flip-flops, I_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.
 - $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4\text{V})$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Output Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Output Frequency}$
 $N_i = \text{Number of Outputs at } f_i$
- All currents are in milliamps and all frequencies are in megahertz.

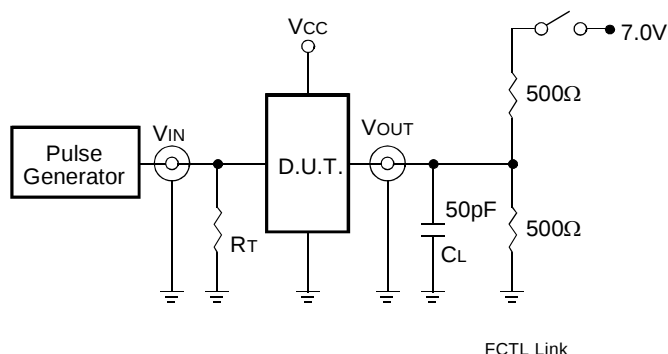
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

Symbol	Parameter	74FCT158AT		74FCT158CT		Unit
		Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay I _{xx} to Y _x	1.5	5	1.5	4.3	ns
t _{PLH} t _{PHL}	Propagation Delay S to Y _x	1.5	7	1.5	5.2	ns
t _{PLH} t _{PHL}	Propagation Delay $\bar{E}$ to Y _x	1.5	6	1.5	4.8	ns

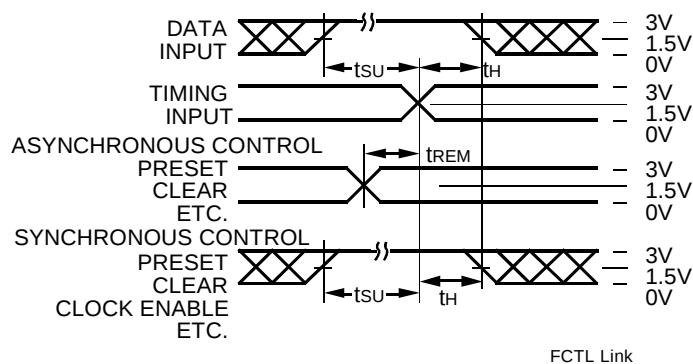
NOTE:

1. C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

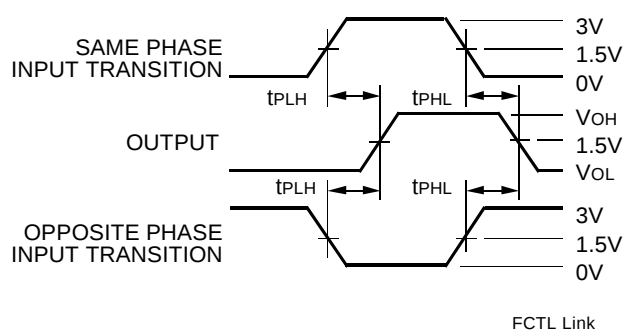
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



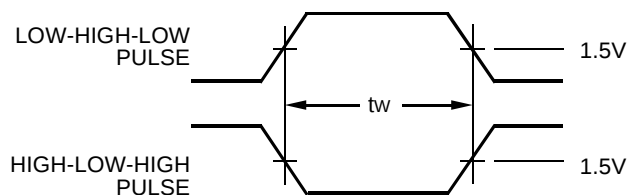
Propagation Delay

SWITCH POSITION

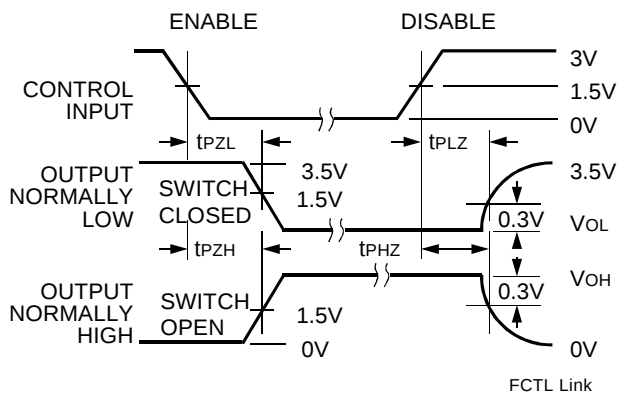
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



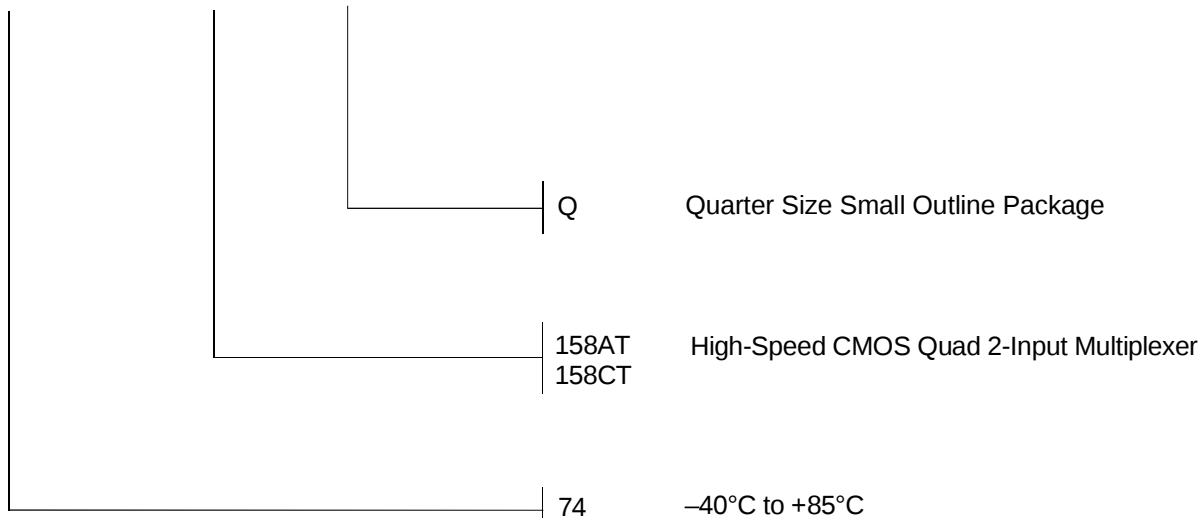
Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDTQS XX FCT XXXX XX
Temp. Range Device Type Package



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