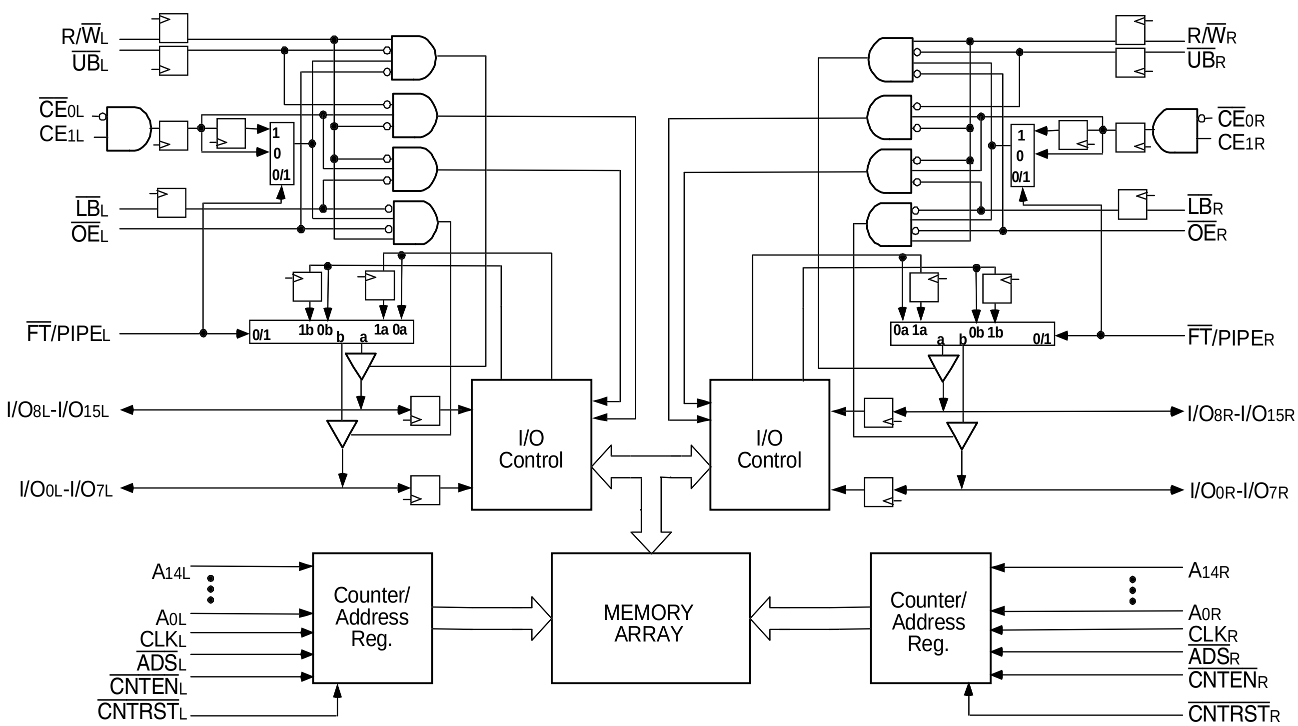
HIGH-SPEED 32K x 16 SYNCHRONOUS DUAL-PORT STATIC RAM

IDT709279S/L

Features

- **True Dual-Ported memory cells which allow simultaneous access of the same memory location**
- **High-speed clock to data access**
  - *Commercial: 9/12/15ns (max.)*
  - *Industrial: 12ns (max.)*
- **Low-power operation**
  - *IDT709279S*
    Active: 950mW (typ.)
    Standby: 5mW (typ.)
  - *IDT709279L*
    Active: 950mW (typ.)
    Standby: 1mW (typ.)
- **Flow-Through or Pipelined output mode on either port via the $\overline{FT}$/PIPE pin**
- **Counter enable and reset features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Full synchronous operation on both ports**
  - *4ns setup to clock and 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 9ns clock to data out in the Pipelined output mode*
  - *Self-timed write allows fast cycle time*
  - *15ns cycle time, 66MHz operation in Pipelined output mode*
- **Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility**
- **TTL- compatible, single 5V (±10%) power supply**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Available in a 100-pin Thin Quad Flatpack (TQFP) package**

Functional Block Diagram



3243 drw 01

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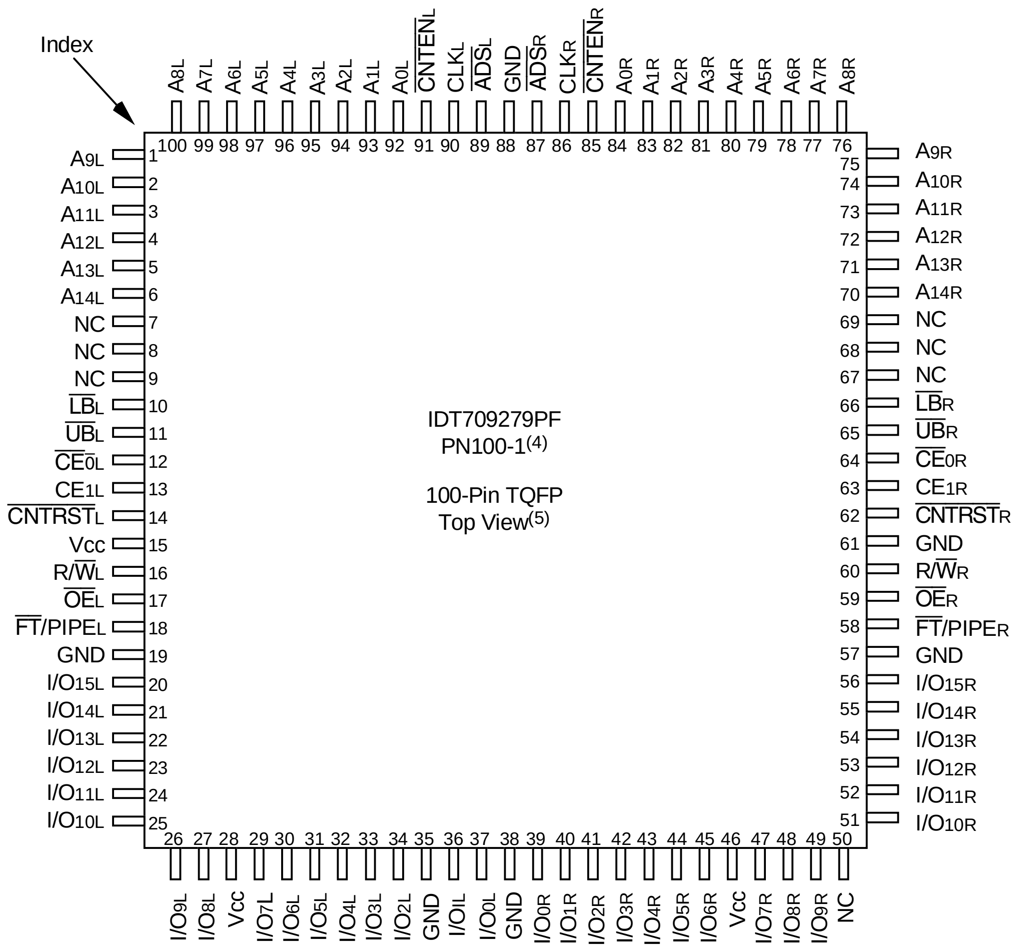
Description

The IDT709279 is a high-speed 32K x 16 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709279 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 950mW of power.

Pin Configurations(1,2,3)



3243 drw 02

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{14L}	A_{0R} - A_{14R}	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
CLK_L	CLK_R	Clock
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through/Pipeline
V_{CC}		Power
GND		Ground

3243 tbl 01

Truth Table I—Read/Write and Enable Control(1,2,3)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	$R/\overline{W}$	Upper Byte I/O_{8-15}	Lower Byte I/O_{0-7}	Mode
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	D_{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	D_{IN}	Write to Lower Byte Only
X	↑	L	H	L	L	L	D_{IN}	D_{IN}	Write to Both Bytes
L	↑	L	H	L	H	H	D_{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	D_{OUT}	Read Lower Byte Only
L	↑	L	H	L	L	H	D_{OUT}	D_{OUT}	Read Both Bytes
H	X	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

3243 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

Truth Table II—Address Counter Control(1,2)

Address	Previous Address	Addr Used	CLK	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	$\overline{\text{CNTRST}}$	I/O(3)	MODE
X	X	0	↑	X	X	L(4)	$D_{I/O}(0)$	Counter Reset to Address 0
An	X	An	↑	L(4)	X	H	$D_{I/O}$ (n)	External Address Used
An	Ap	Ap	↑	H	H	H	$D_{I/O}(p)$	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L(5)	H	$D_{I/O}(p+1)$	Counter Enabled—Internal Address generation

3243 tbl 03

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. $\overline{\text{CE}}_0$, $\overline{\text{LB}}$, $\overline{\text{UB}}$, and $\overline{\text{OE}}$ = V_{IL}; CE_1 and R/$\overline{\text{W}}$ = V_{IH}.
3. Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{\text{ADS}}$ is independent of all other signals including $\overline{\text{CE}}_0$, CE_1, $\overline{\text{UB}}$ and $\overline{\text{LB}}$.
5. The address counter advances if $\overline{\text{CNTEN}}$ = V_{IL} on the rising edge of CLK, regardless of all other signals including $\overline{\text{CE}}_0$, CE_1, $\overline{\text{UB}}$ and $\overline{\text{LB}}$.

Recommended Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3243 tbl 04

NOTES:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(1)	V
V_{IL}	Input Low Voltage	-0.5(2)	—	0.8	V

3243 tbl 05

NOTES:
1. V_{TERM} must not exceed V_{CC} + 10%.
2. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	DC Output Current	50	mA

3243 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.

CAPACITANCE(1)

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}(3)	Output Capacitance	V_{OUT} = 3dV	10	pF

3243 tbl 07

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C_{OUT} also references $C_{I/O}$.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	709279S/L Min.	709279S/L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$CE_0 = V_{IH}$ or $CE_1 = V_{IL}$, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

3243 tbl 08

NOTE:
1. At Vcc ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[6] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		709279X9 Com'l Only Typ.[4]	709279X9 Com'l Only Max.	709279X12 Com'l & Ind Typ.[4]	709279X12 Com'l & Ind Max.	709279X15 Com'l Only Typ.[4]	709279X15 Com'l Only Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ Outputs Disabled f = f_{MAX}[1]	COM'L	S	210	390	200	345	190	325	mA
				L	210	350	200	305	190	285	
			IND	S	—	—	200	380	—	—	
				L	—	—	200	340	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ f = f_{MAX}[1]	COM'L	S	50	135	50	110	50	110	mA
				L	50	115	50	90	50	90	
			IND	S	—	—	50	125	—	—	
				L	—	—	50	105	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"} = V_{IL}$ and $\overline{CE}_{"B"} = V_{IH}$[3] Active Port Outputs Disabled, f=f_{MAX}[3]	COM'L	S	140	270	130	230	120	220	mA
				L	140	240	130	200	120	190	
			IND	S	—	—	130	245	—	—	
				L	—	—	130	215	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports CE_R and $\overline{CE}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0[2]	COM'L	S	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	
			IND	S	—	—	1.0	15	—	—	
				L	—	—	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq 0.2V$ and $\overline{CE}_{"B"} \geq V_{CC} - 0.2V$[5] $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled, f = f_{MAX}[1]	COM'L	S	130	245	120	205	110	195	mA
				L	130	225	120	185	110	175	
			IND	S	—	—	120	220	—	—	
				L	—	—	120	200	—	—	

3243 tbl 09

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. Vcc = 5V, TA = 25°C for Typ, and are not production tested. $I_{CC\,DC}$(f=0) = 150mA (Typ).
5. $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
   $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
   $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{CC} - 0.2V$
   $\overline{CE}_X \geq V_{CC} - 0.2V$ means $\overline{CE}_{0X} \geq V_{CC} - 0.2V$ or $CE_{1X} \leq 0.2V$
   "X" represents "L" for left port or "R" for right port.
6. 'X' in part numbers indicate power rating (S or L).

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3243 tbl 10

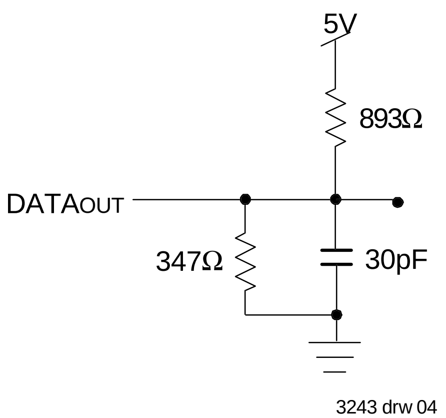


Figure 1. AC Output Test load.

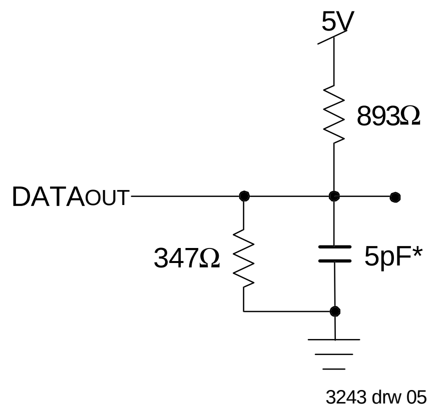


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

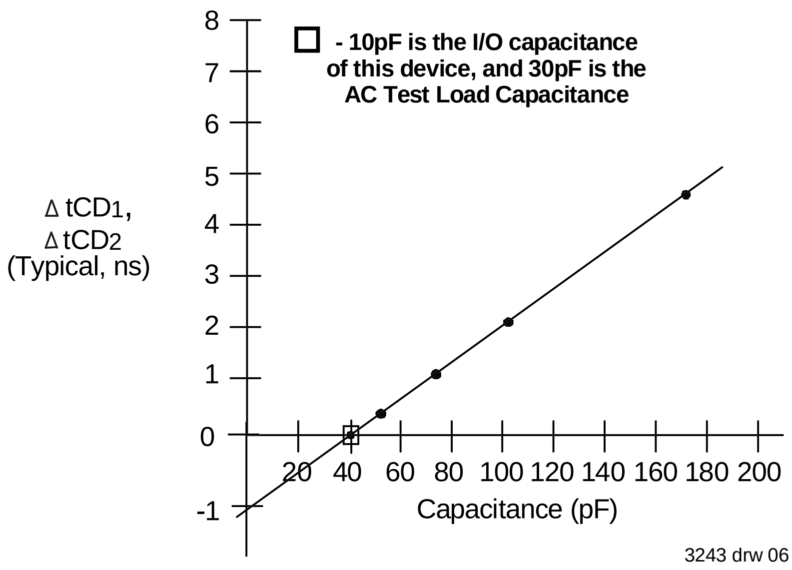


Figure 3. Typical Output Derating (Lumped Capacitive Load).

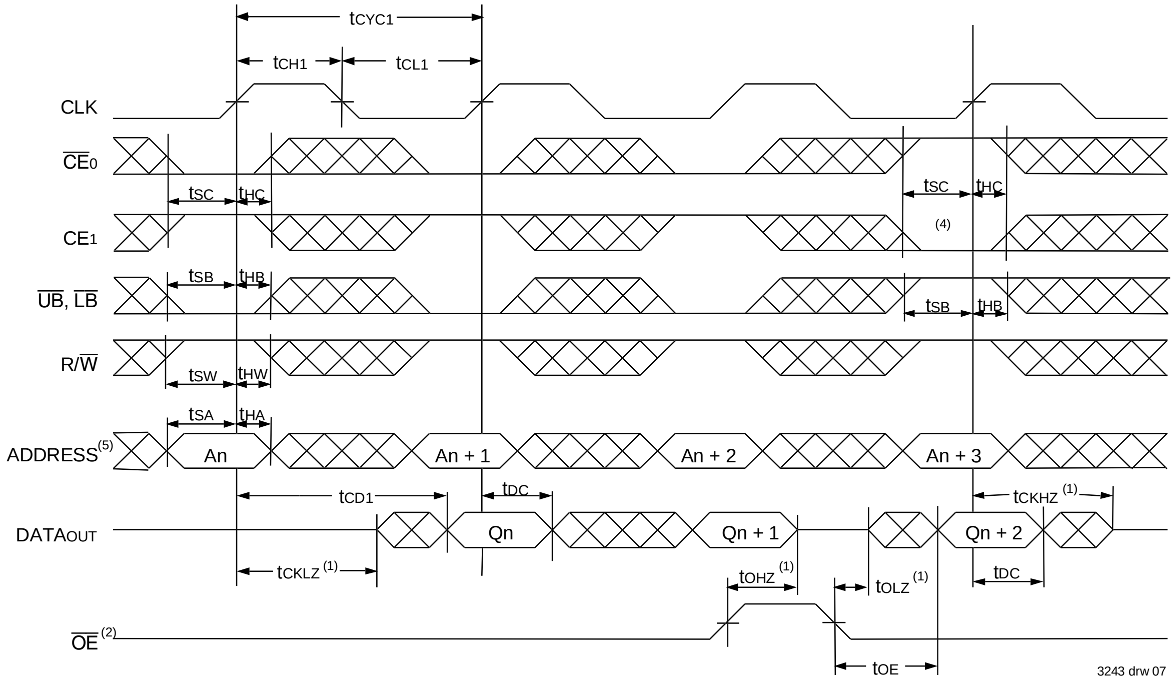
AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3,4] (Vcc = 5V ± 10%, TA = 0°C to +70°C)

		709279X9 Com'l Only		709279X12 Com'l & Ind		709279X15 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC1}	Clock Cycle Time (Flow-Through)[2]	25	—	30	—	35	—	ns
t_{CYC2}	Clock Cycle Time (Pipelined)[2]	15	—	20	—	25	—	ns
t_{CH1}	Clock High Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_{CL1}	Clock Low Time (Flow-Through)[2]	12	—	12	—	12	—	ns
t_{CH2}	Clock High Time (Pipelined)[2]	6	—	8	—	10	—	ns
t_{CL2}	Clock Low Time (Pipelined)[2]	6	—	8	—	10	—	ns
t_R	Clock Rise Time	—	3	—	3	—	3	ns
t_F	Clock Fall Time	—	3	—	3	—	3	ns
t_{SA}	Address Setup Time	4	—	4	—	4	—	ns
t_{HA}	Address Hold Time	1	—	1	—	1	—	ns
t_{SC}	Chip Enable Setup Time	4	—	4	—	4	—	ns
t_{HC}	Chip Enable Hold Time	1	—	1	—	1	—	ns
t_{SB}	Byte Enable Setup Time	4	—	4	—	4	—	ns
t_{HB}	Byte Enable Hold Time	1	—	1	—	1	—	ns
t_{SW}	R/$\overline{W}$ Setup Time	4	—	4	—	4	—	ns
t_{HW}	R/$\overline{W}$ Hold Time	1	—	1	—	1	—	ns
t_{SD}	Input Data Setup Time	4	—	4	—	4	—	ns
t_{HD}	Input Data Hold Time	1	—	1	—	1	—	ns
t_{SAD}	$\overline{ADS}$ Setup Time	4	—	4	—	4	—	ns
t_{HAD}	$\overline{ADS}$ Hold Time	1	—	1	—	1	—	ns
t_{SCN}	$\overline{CNTEN}$ Setup Time	4	—	4	—	4	—	ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	1	—	1	—	1	—	ns
t_{SRST}	$\overline{CNTRST}$ Setup Time	4	—	4	—	4	—	ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	1	—	1	—	1	—	ns
t_{OE}	Output Enable to Data Valid	—	12	—	12	—	15	ns
t_{OLZ}	Output Enable to Output Low-Z[1]	2	—	2	—	2	—	ns
t_{OHZ}	Output Enable to Output High-Z[1]	1	7	1	7	1	7	ns
t_{CD1}	Clock to Data Valid (Flow-Through)[2]	—	20	—	25	—	30	ns
t_{CD2}	Clock to Data Valid (Pipelined)[2]	—	9	—	12	—	15	ns
t_{DC}	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1]	2	9	2	9	2	9	ns
t_{CKLZ}	Clock High to Output Low-Z[1]	2	—	2	—	2	—	ns
Port-to-Port Delay								
t_{CWDD}	Write Port Clock High to Read Data Delay	—	35	—	40	—	50	ns
t_{CCS}	Clock-to-Clock Setup Time	—	15	—	15	—	20	ns

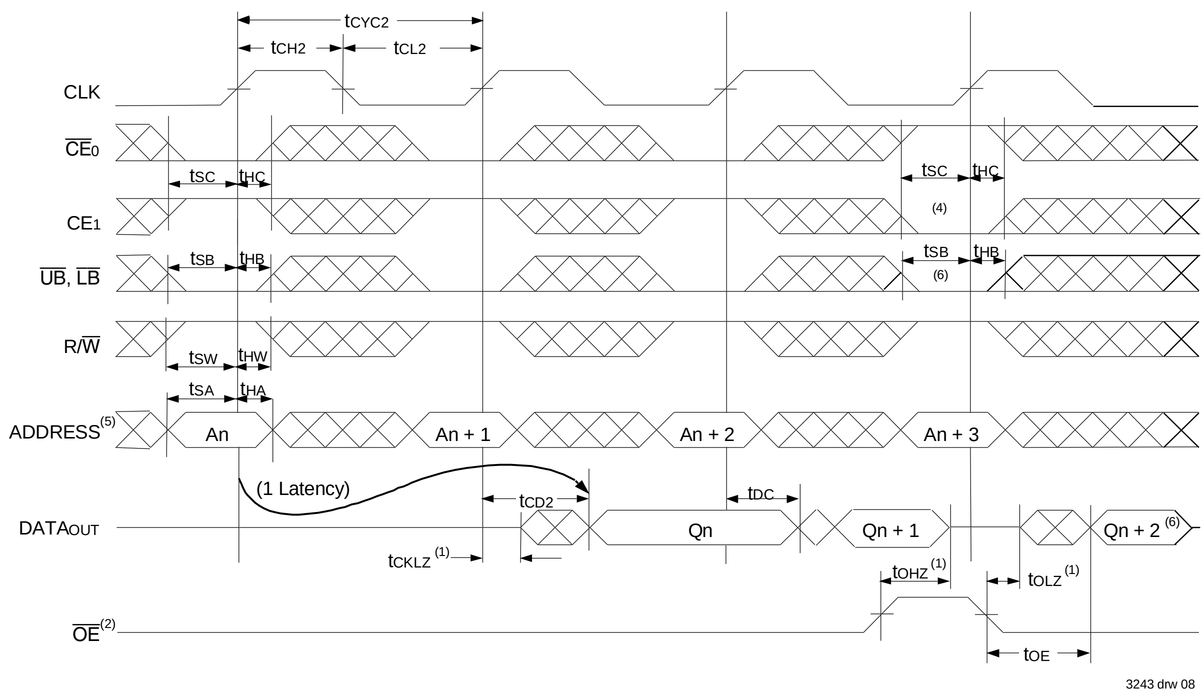
3243 tbl 11

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}$/PIPE = V_{IH}. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}$/PIPE = V_{IL} for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}$/PIPE. $\overline{FT}$/PIPE should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).

Timing Waveform of Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE"x" = VIL)(3,7)



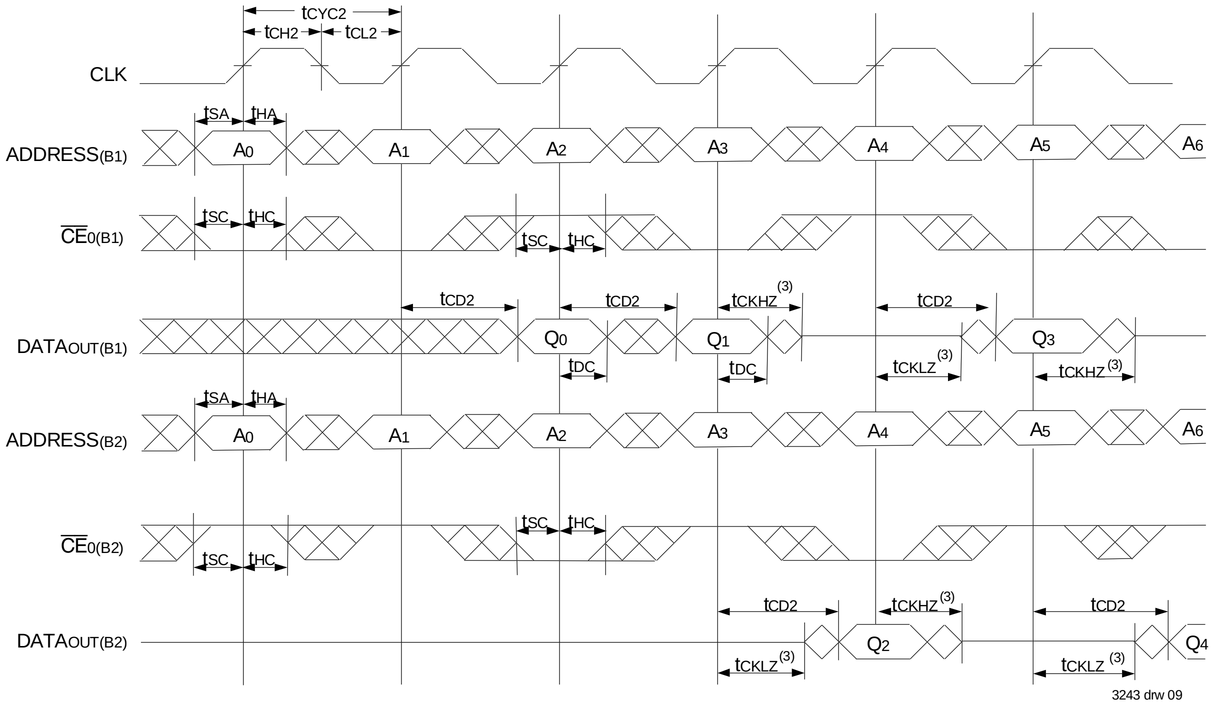
Timing Waveform of Read Cycle for Pipelined Output ($\overline{FT}$/PIPE"x" = VIH)(3,7)



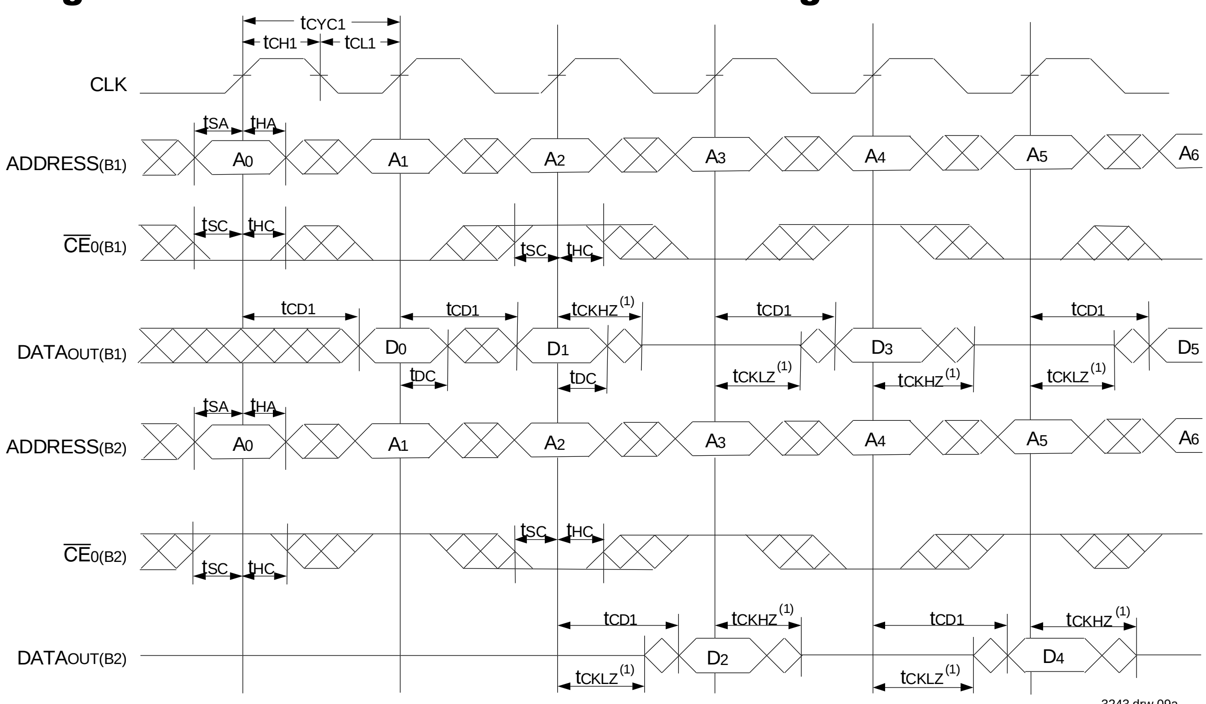
NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = VIL, $\overline{CNTEN}$ and $\overline{CNTRST}$ = VIH.
4. The output is disabled (High-Impedance state) by $\overline{CE_0}$ = VIH, CE1 = VIL, $\overline{UB}$ = VIH, or $\overline{LB}$ = VIH following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If $\overline{UB}$ or $\overline{LB}$ was HIGH, then the Upper Byte and/or Lower Byte of DATAOUT for Qn + 2 would be disabled (High-Impedance state).
7. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read(1,2)



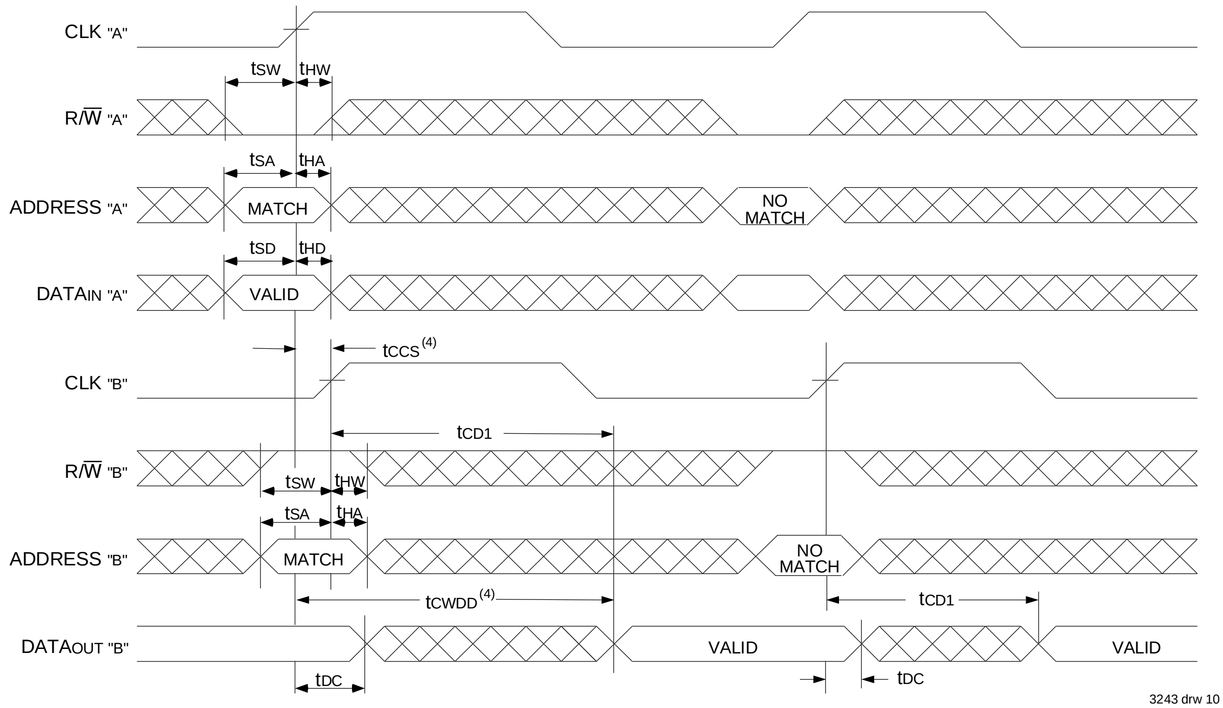
Timing Waveform of a Bank Select Flow-Through Read(6)



NOTES:

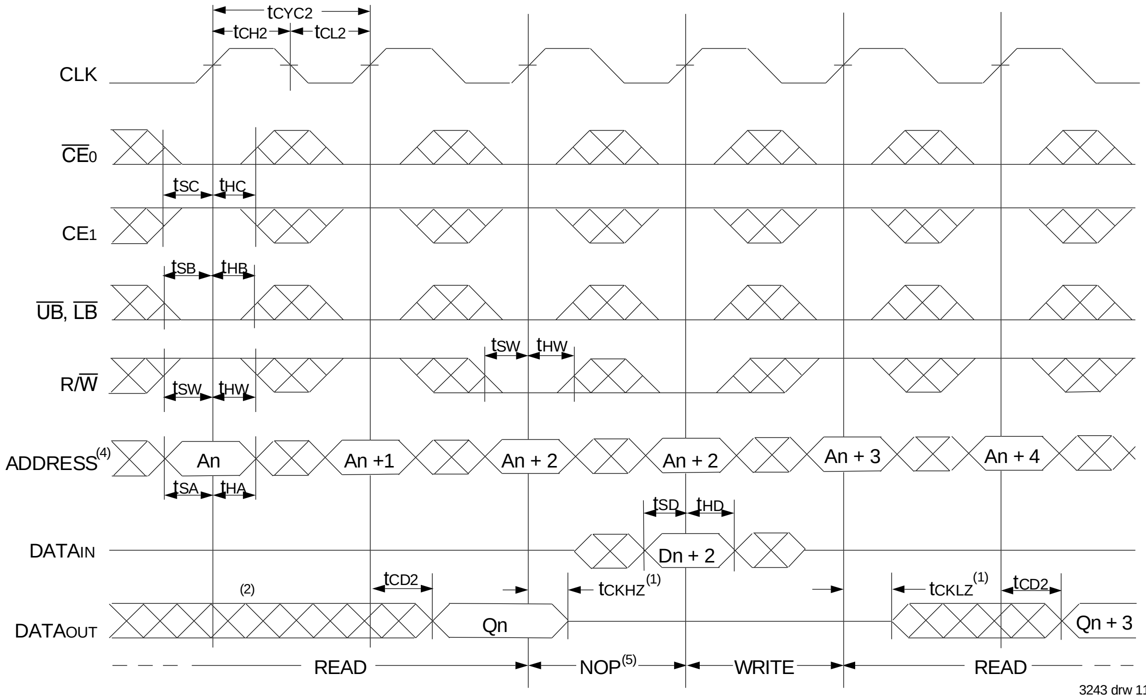
1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT709279 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and $\overline{ADS}$ = V_{IL}; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
5. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until t_{CCS} + t_{CD1}. t_{CWDD} does not apply in this case.

Timing Waveform with Port-to-Port Flow-Through Read(1,2,3,5)

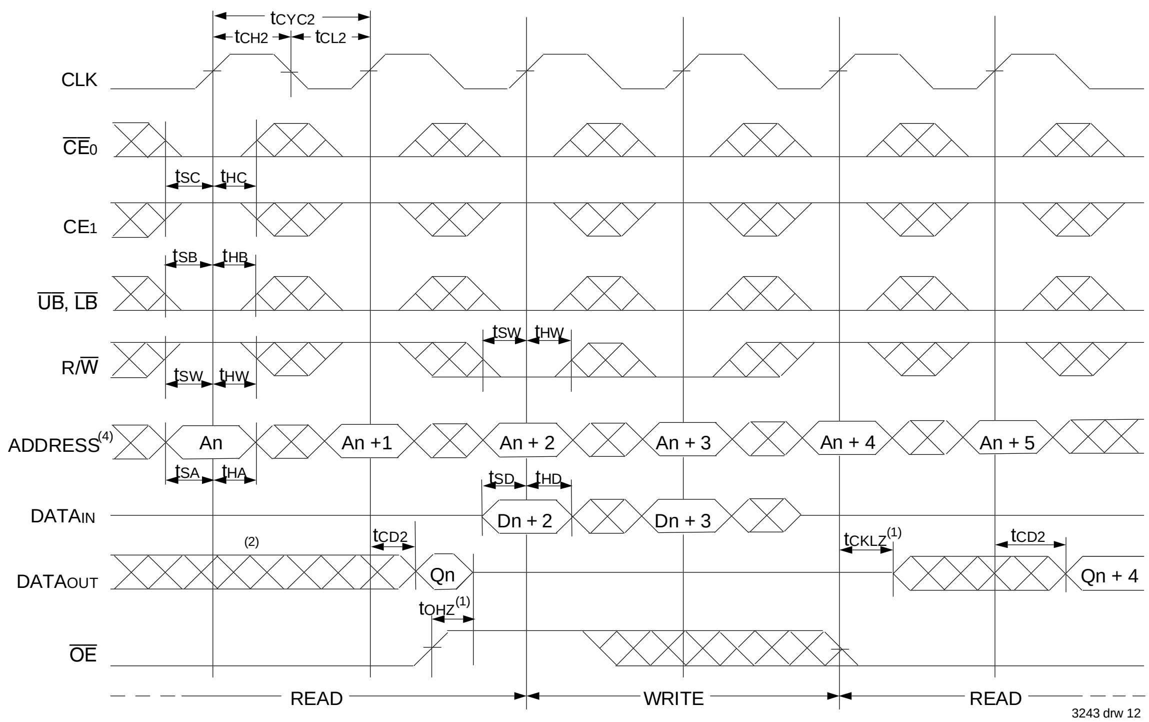


NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
3. $\overline{OE}$ = V_{IL} for the Right Port, which is being read from. $\overline{OE}$ = V_{IH} for the Left Port, which is being written to.
4. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS} > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.
5. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)[3]

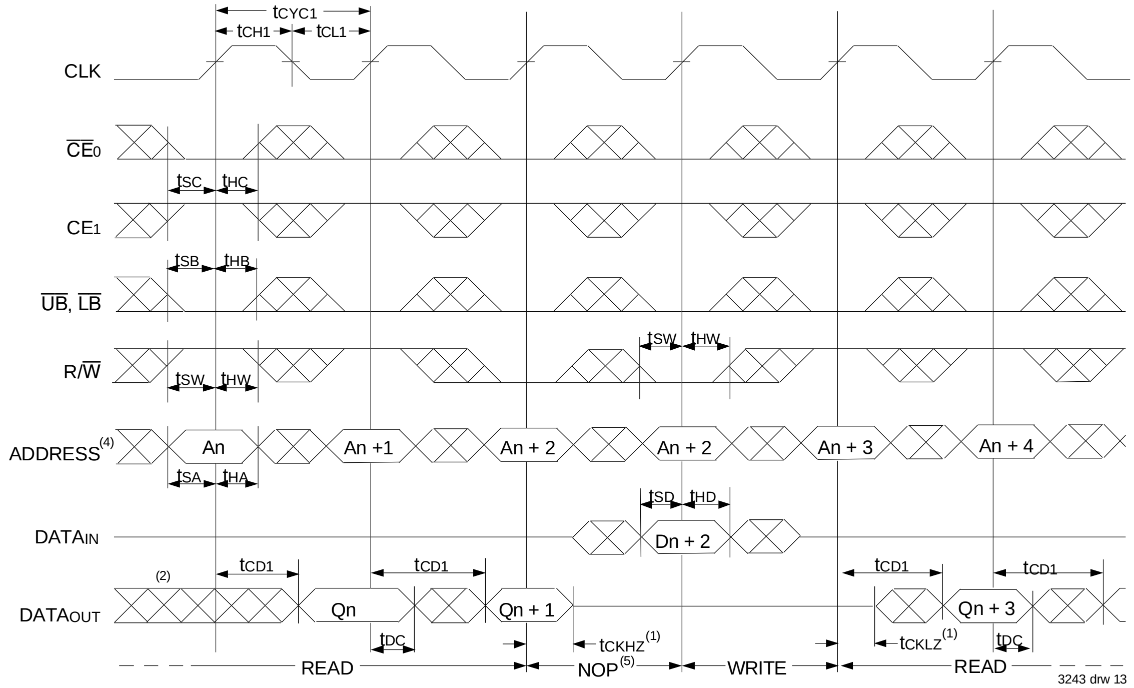


Timing Waveforn of Pipelined Read-to-Write-to-Read (OE Controlled)[3]

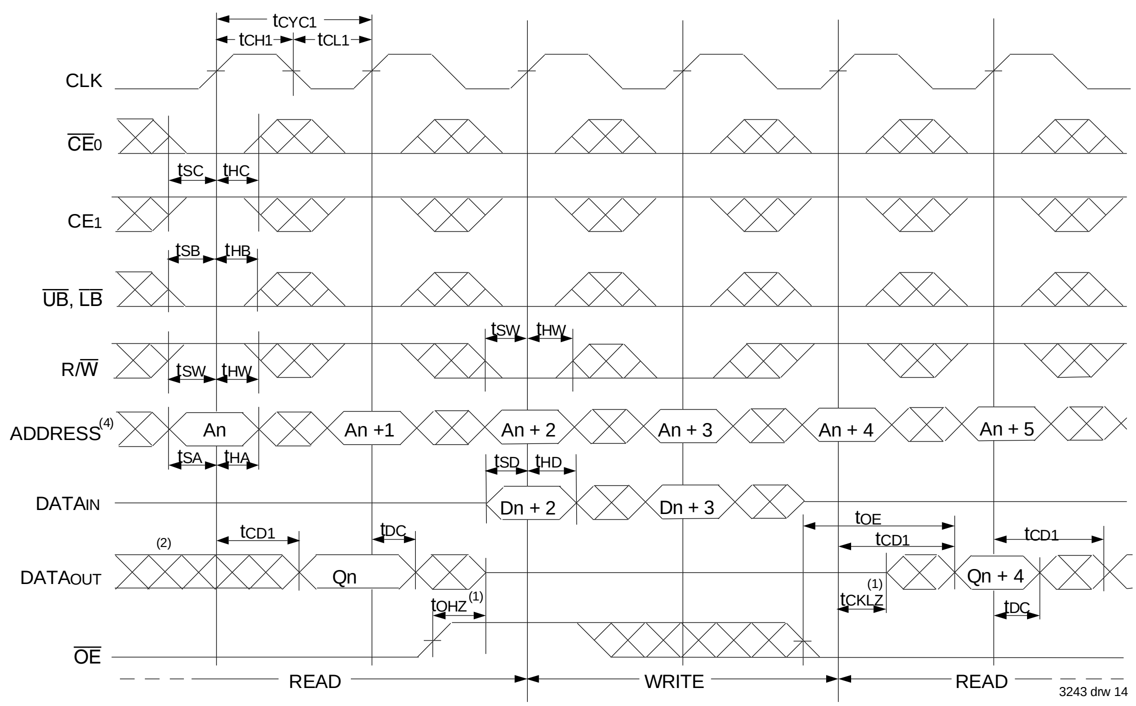


NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)

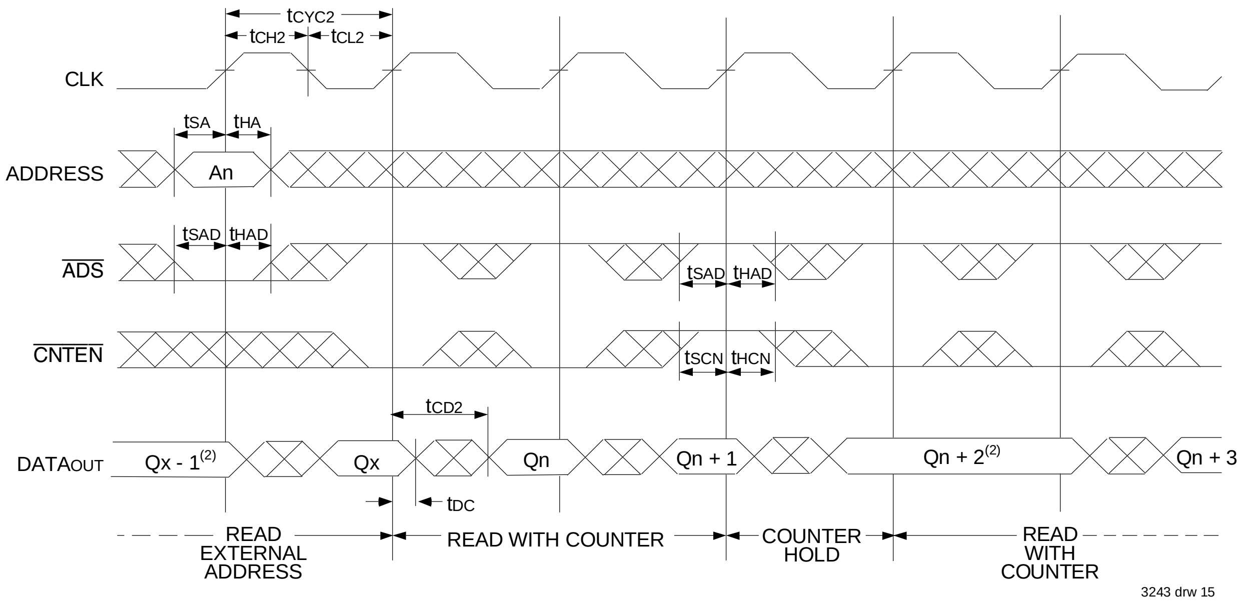


Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)

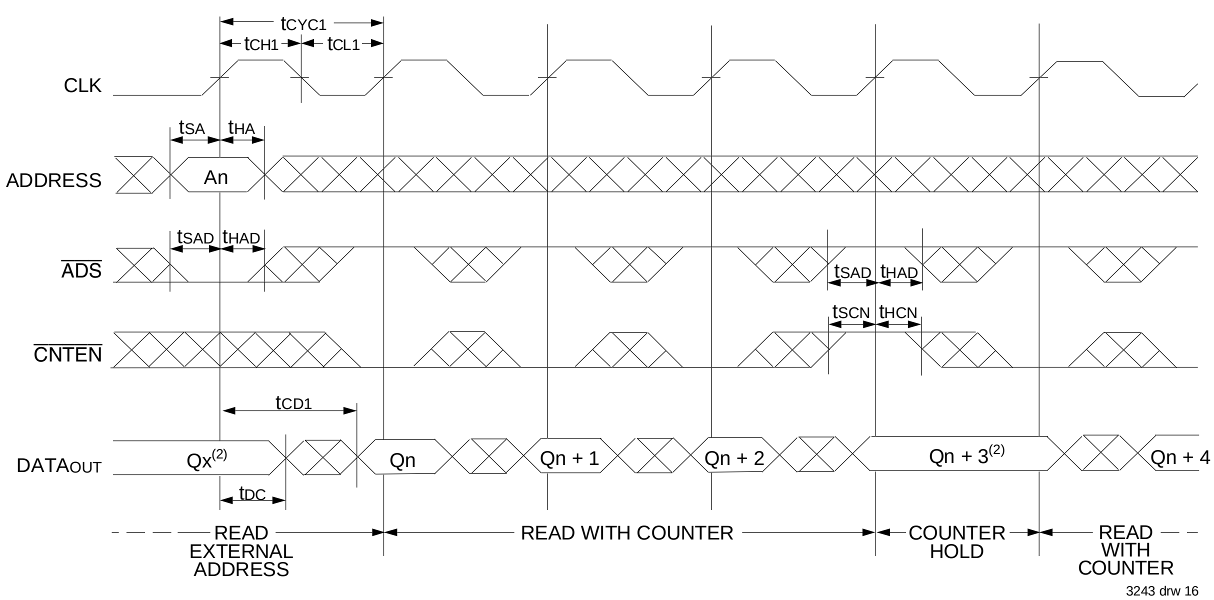


NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance is determined by the previous cycle control signals.
3. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance(1)

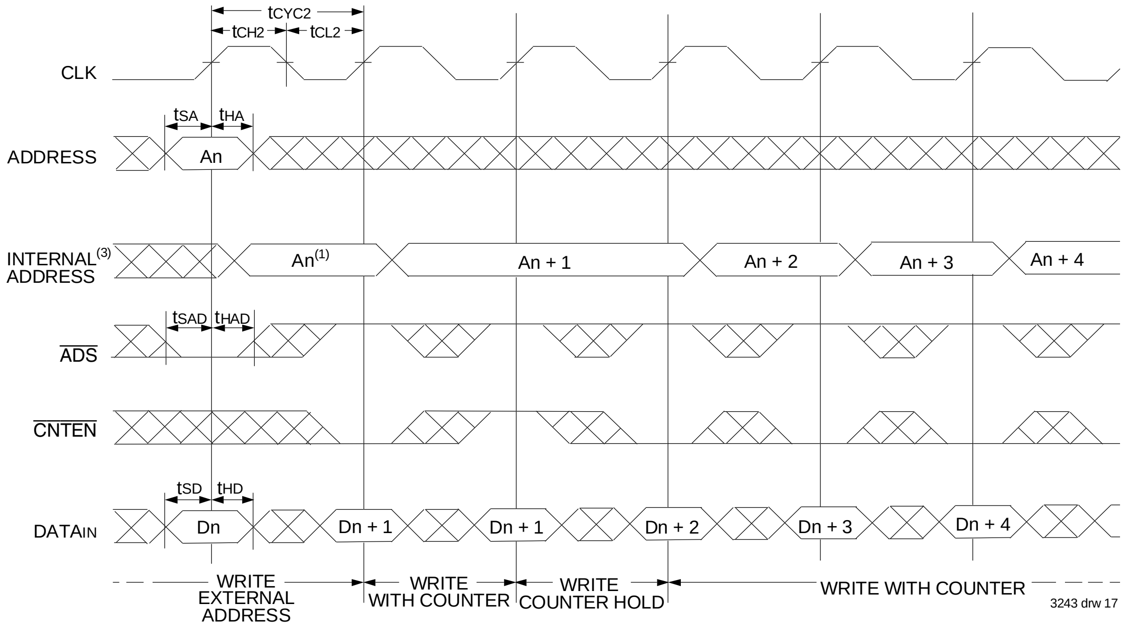


Timing Waveform of Flow-Through Read with Address Counter Advance(1)

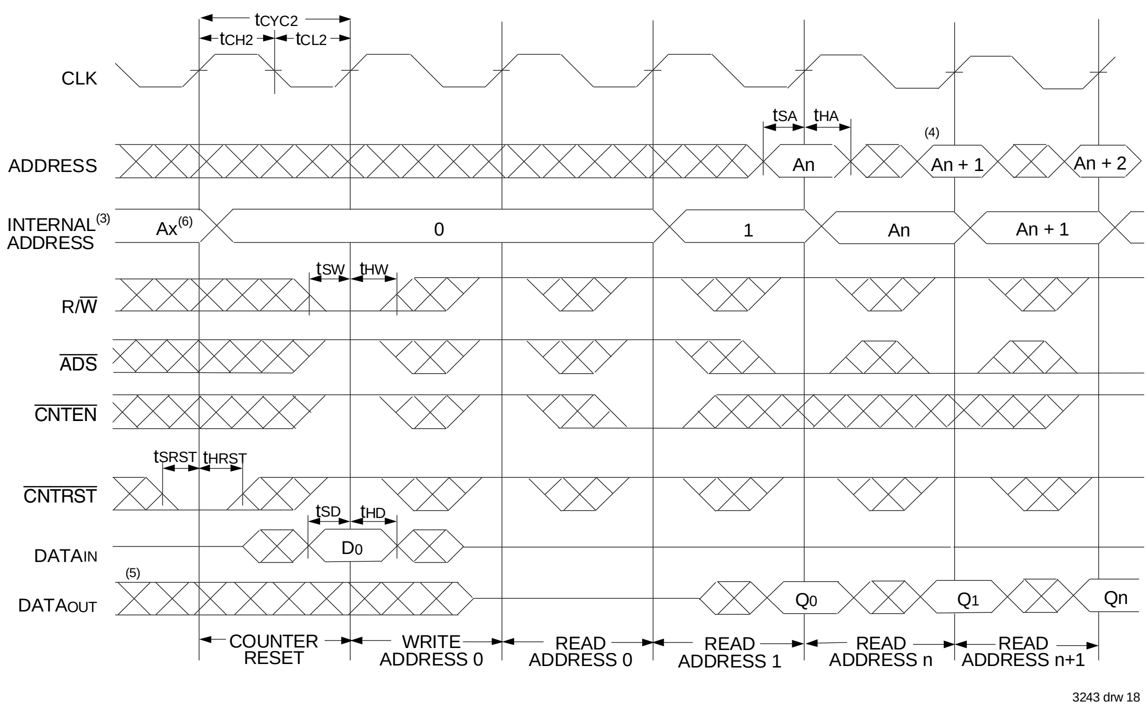


NOTES:
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$ = V_{IL}; CE_1, R/$\overline{W}$, and $\overline{CNTRST}$ = V_{IH}.
2. If there is no address change via $\overline{ADS}$ = V_{IL} (loading a new address) or $\overline{CNTEN}$ = V_{IL} (advancing the address), i.e. $\overline{ADS}$ = V_{IH} and $\overline{CNTEN}$ = V_{IH}, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)(1)



Timing Waveform of Counter Reset (Pipelined Outputs)(2)



NOTES:
1. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
2. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$ = V_{IL}; CE_1 = V_{IH}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = V_{IL} advances Internal Address from ‘An’ to ‘An +1’. The transition shown indicates the time required for the counter to advance. The ‘An +1’Address is written to during this cycle.

A Functional Description

The IDT709279 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE}_0$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709279's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT709279 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The 709279 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 32-bit or wider applications.

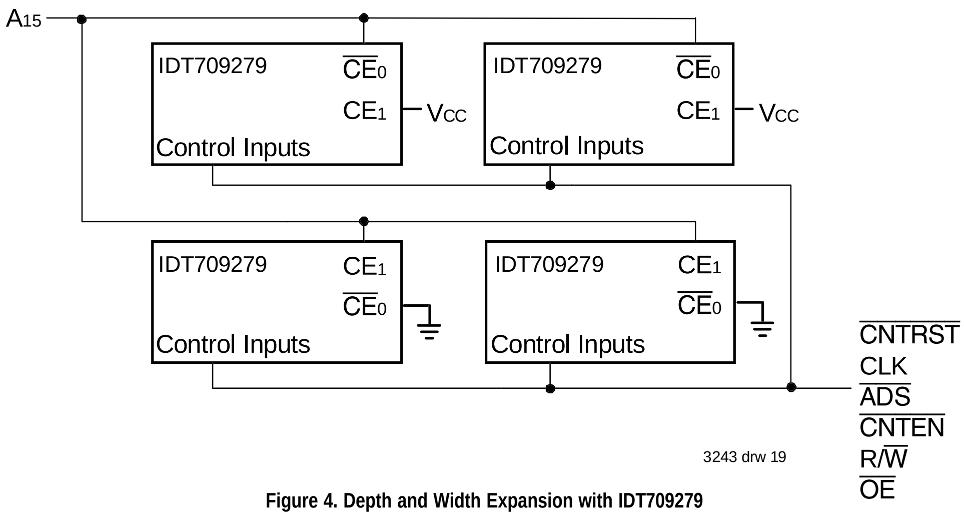
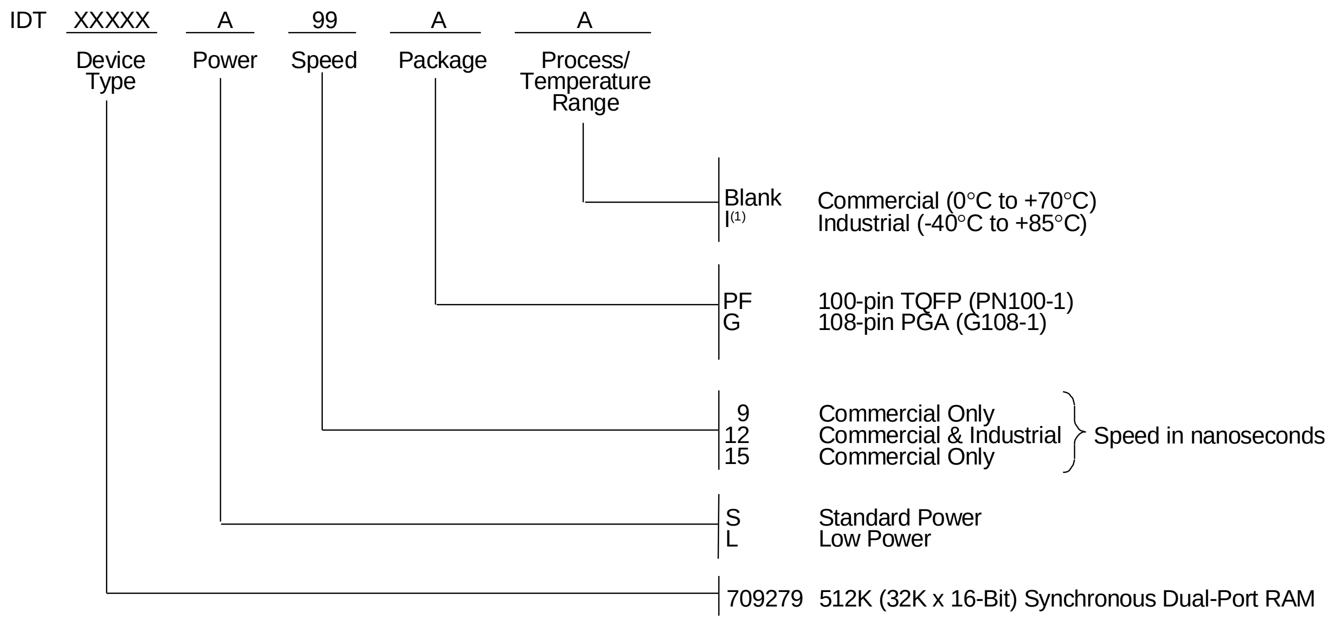


Figure 4. Depth and Width Expansion with IDT709279

Ordering Information



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NOTES:

1. Industrial temperature range is available.
For specific speeds, packages and powers contact your sales office.

Ordering Information for Flow-through Devices

Old Flow-through Part	New Combined Part
70927S/L20	709279S/L9
70927S/L25	709279S/L12
70927S/L30	709279S/L15

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Datasheet Document History

12/9/98:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Added additional notes to pin configurations
	Pages 13 & 14 Updated timing waveforms
	Page 15 Added Depth and Width Expansion section
6/3/99	Changed drawing format
	Page 3 Deleted note 6 for Table II
11/10/99:	Replaced IDT logo
3/31/00:	Combined Pipelined 709279 family and Flow-through 70927 family offerings into one data sheet
	Changed ±200mV in waveform notes to 0mV
	Added corresponding part chart with ordering information
5/24/00:	Page 1 Inserted diamond in copy
	Page 4 Changed information in Truth Table II, Increased storage temperature parameter, clarified T_A parameter
	Page 5 Changed DC Electrical parameters–changed wording from "Open" to "Disabled"
	Page 16 Fixed typeface in heading
	Added Industrial Temperature Ranges and removed related notes
8/24/01:	Pages 1, 16 and Page Header Removed Preliminary status
	Page 5 & 7 Removed Industrial Temperature Ranges for 15ns speed from DC and AC Electrical Characteristics
	Page 16 Removed Industrial Temperature from 15ns speed in ordering information

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