



**QUICKSWITCH® PRODUCTS**  
**HIGH-SPEED CMOS**  
**QUICKSWITCH**  
**DUAL 4:1 MUX/DEMUX**

**IDTQS3253**

**FEATURES:**

- Enhanced N channel FET with no inherent diode to Vcc
- 5Ω bidirectional switches connect inputs to outputs
- Pin compatible with the 74F253, 74FCT253, and 74FCT253T
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control inputs
- TTL-compatible control inputs
- Available in SOIC, QSOP, and S1 packages

**APPLICATIONS:**

- Logic replacement
- Video, audio, graphics switching, muxing
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Power conservation
- Bus funneling

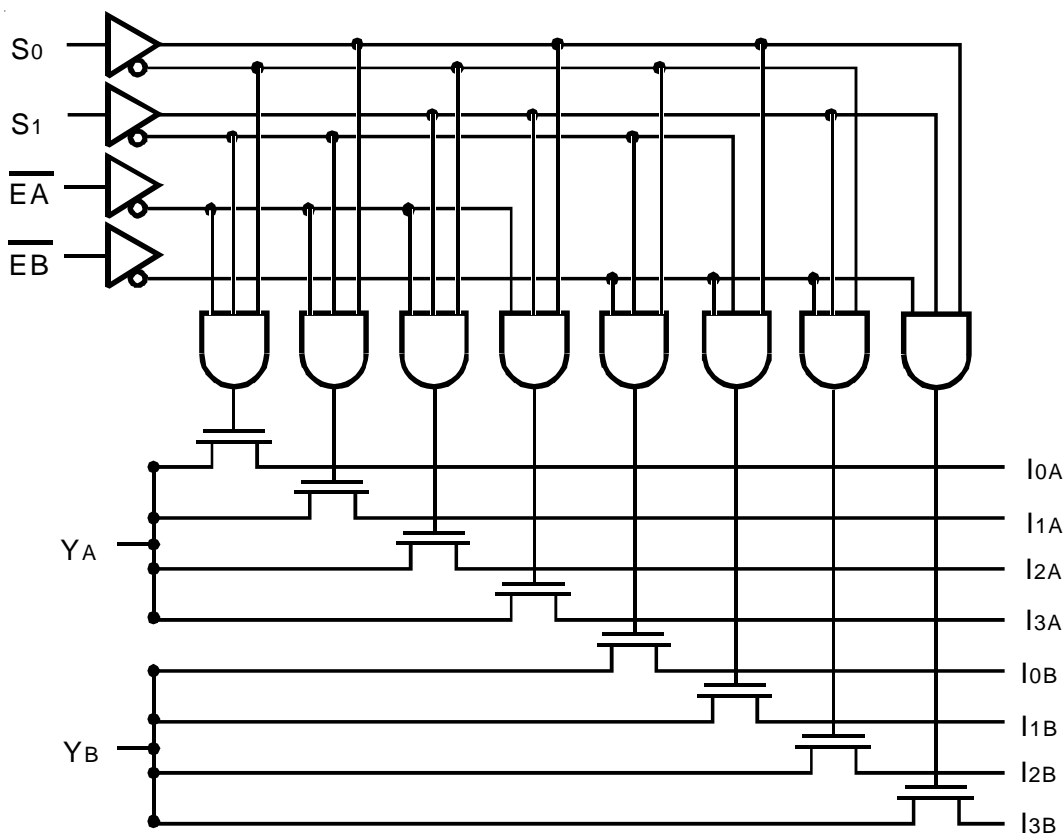
**DESCRIPTION:**

The QS3253 is a high-speed CMOS TTL-compatible dual 4:1 multiplexer/demultiplexer with 3-state outputs. The QS3253 is function and pinout compatible version of the 74F253, 74FCT253, and the 74ALS/AS/LS253 dual 4:1 multiplexers. The low ON resistance of the QS3253 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise.

Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

The QS3253 is characterized for operation at -40°C to +85°C.

**FUNCTIONAL BLOCK DIAGRAM**

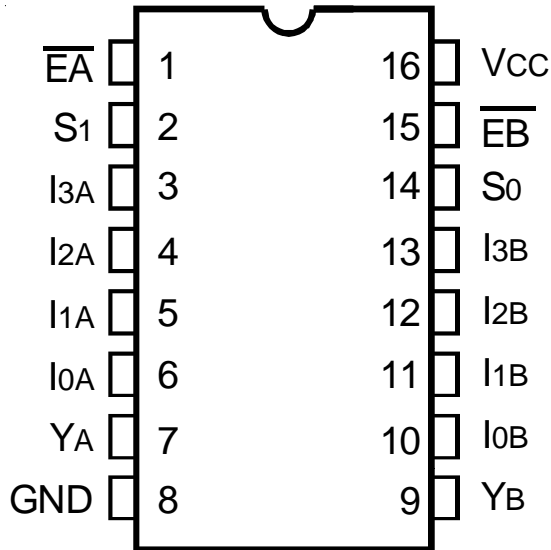


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**INDUSTRIAL TEMPERATURE RANGE**

**AUGUST 2001**

## PIN CONFIGURATION



SOIC/ QSOP/ S1  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Supply Voltage to Ground	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Switch Voltage Vs	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Input Voltage VIN	-0.5 to +7	V
VAC	AC Input Voltage (pulse width ≤ 20ns)	-3	V
IOUT	DC Output Current	120	mA
PMAX	Maximum Power Dissipation (TA = 85°C)	0.5	W
TSTG	Storage Temperature	-65 to +150	°C

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

## CAPACITANCE (TA = +25°C, f = 1MHz, VIN = 0V, VOUT = 0V)

Pins		Typ.	Max. <sup>(1)</sup>	Unit
Control Inputs		4	5	pF
Quickswitch Channels (Switch OFF)	Demux	5	7	pF
	Mux	14	16	

### NOTE:

- This parameter is guaranteed but not production tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
Ixx	I	Data Inputs
S0 - S2	I	Select Inputs
EA, EB	I	Enable Input
YA, YB	O	Data Output

## FUNCTION TABLE<sup>(1)</sup>

Enable		Select		Outputs		Function
EA	EB	S1	S0	YA	YB	
H	X	X	X	Hi-Z	X	Disconnected
X	H	X	X	X	Hi-Z	Disconnected
L	L	L	L	I0A	I0B	S1 - 0 = 0
L	L	L	H	I1A	I1B	S1 - 0 = 1
L	L	H	L	I2A	I2B	S1 - 0 = 2
L	L	H	H	I3A	I3B	S1 - 0 = 3

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedence

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

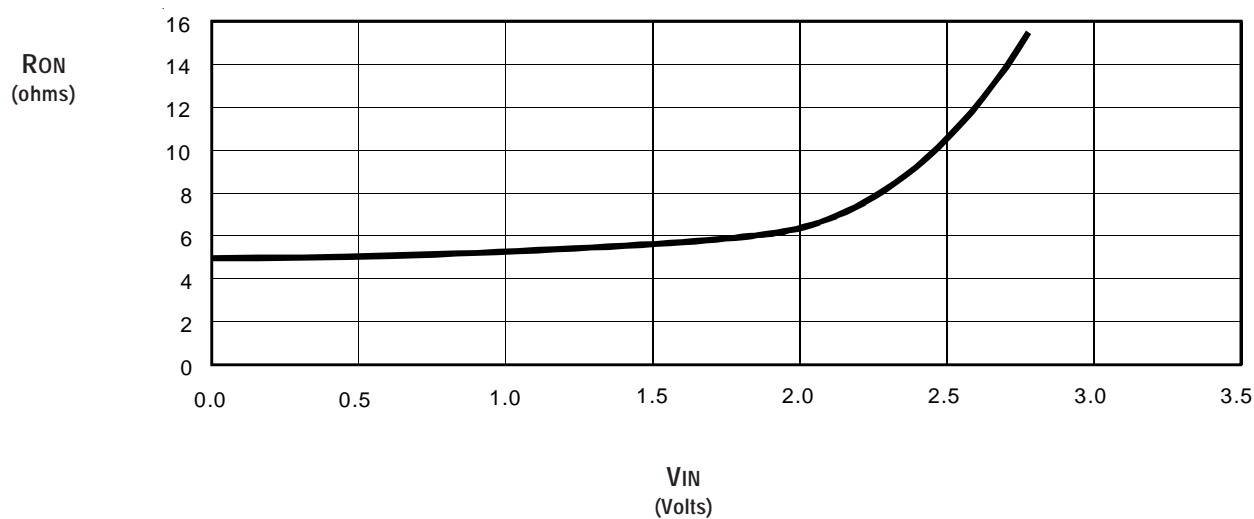
Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH for Control Pins	2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$I_{IN}$	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	Off-State Output Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$R_{ON}$	Switch ON Resistance	$V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$	—	5	7	$\Omega$
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	10	15	
$V_P$	Pass Voltage <sup>(2)</sup>	$V_{IN} = V_{CC} = 5\text{V}, I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

### NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ .

2. Pass Voltage is guaranteed but not production tested.

## TYPICAL ON RESISTANCE vs $V_{IN}$ AT $V_{CC} = 5\text{V}$



## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Max.	Unit
I <sub>CCQ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub> , f = 0	3	μA
ΔI <sub>CC</sub>	Power Supply Current per Control Input HIGH <sup>(2)</sup>	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V, f = 0	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current per MHz <sup>(3)</sup>	V <sub>CC</sub> = Max., I and Y pins open Control Inputs Toggling at 50% Duty Cycle	0.25	mA/MHz

### NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input (V<sub>IN</sub> = 3.4V, control inputs only). I and Y pins do not contribute to ΔI<sub>CC</sub>.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0V ± 5%;

C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Parameter	Min. <sup>(1)</sup>	Typ.	Max.	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Data Propagation Delay <sup>(2,3)</sup> I <sub>x</sub> to Y	—	—	0.25	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Switch Turn-on Delay S <sub>x</sub> to Y	0.5	—	6.6	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Switch Turn-on Delay $\overline{E}_x$ to Y	0.5	—	6	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Switch Turn-off Delay <sup>(2)</sup> $\overline{E}_x$ to Y, S <sub>x</sub> to Y	0.5	—	6	ns

### NOTES:

1. Minimums are guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C<sub>L</sub> = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ORDERING INFORMATION

IDTQS	XXXXX	XX		
	Device Type	Package		
			SO	Small Outline IC
			Q	Quarter Size Outline Package
			S1	Quarter Size Outline Package
			3253	High Speed CMOS Quickswitch Dual 4:1 Mux/Demux



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**  
800-345-7015 or 408-727-6116  
fax: 408-492-8674  
[www.idt.com](http://www.idt.com)

**for Tech Support:**  
[logichelp@idt.com](mailto:logichelp@idt.com)  
(408) 654-6459