



3.3V CMOS 12-BIT SYNCHRONOUS BUS EXCHANGER WITH BUS-HOLD AND 5 VOLT TOLERANT I/O

IDT74LVCH16276A

FEATURES:

- Typical $t_{SK(O)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu W$ typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

The LVCH16276A synchronous bus exchanger is built using advanced dual metal CMOS technology. The LVCH16276A is a high-speed, bidirectional, 12-bit, registered, bus multiplexer for use in synchronous memory interleaving applications. All registers have a common clock and use a clock enable ($\overline{CE}_{xxx}$) on each data register to control data sequencing. The output enables and mux select ($\overline{OE}_A$, $\overline{OE}_B$ and SEL) are also under synchronous control allowing direction changes to be edge triggered events.

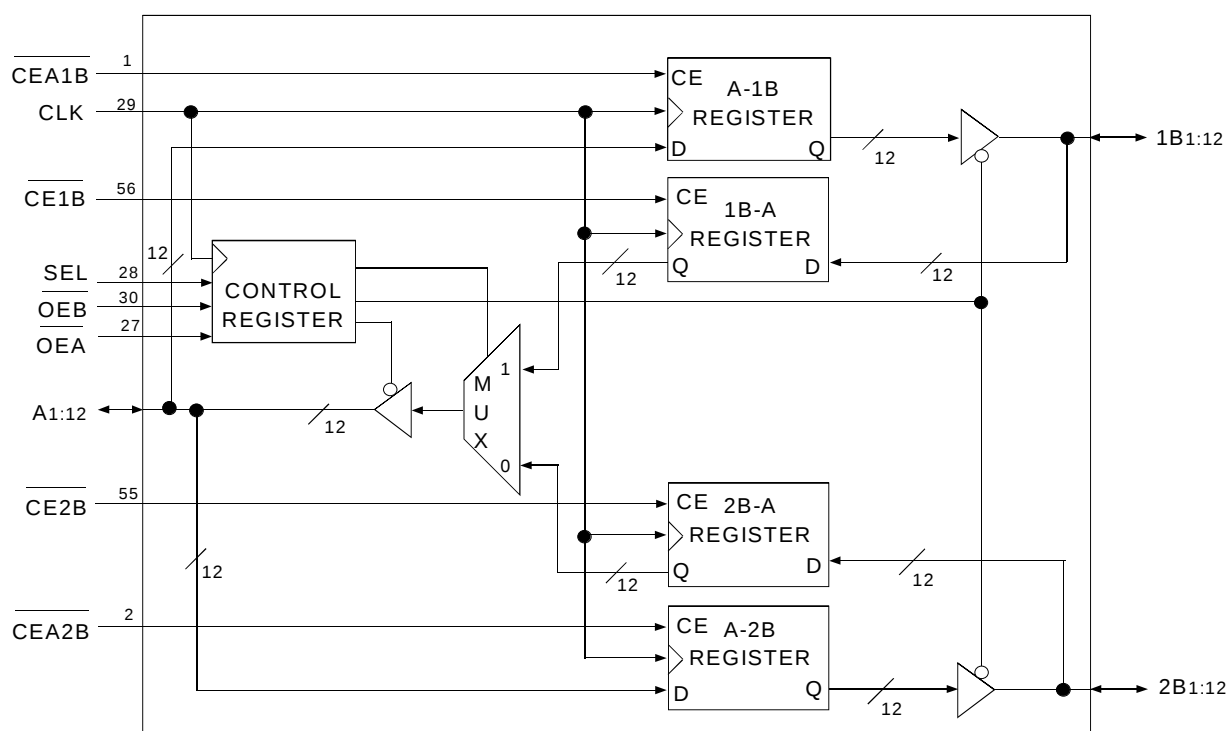
The tri-port bus exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The clock enable ($\overline{CE}_{1B}$, $\overline{CE}_{2B}$, $\overline{CE}_{A1B}$ and $\overline{CE}_{A2B}$) inputs control the data storage. Both B ports have a common output enable ($\overline{OE}_B$) to aid in synchronously loading the B registers from the B port.

All pins of the LVCH16276A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16276A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16276A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

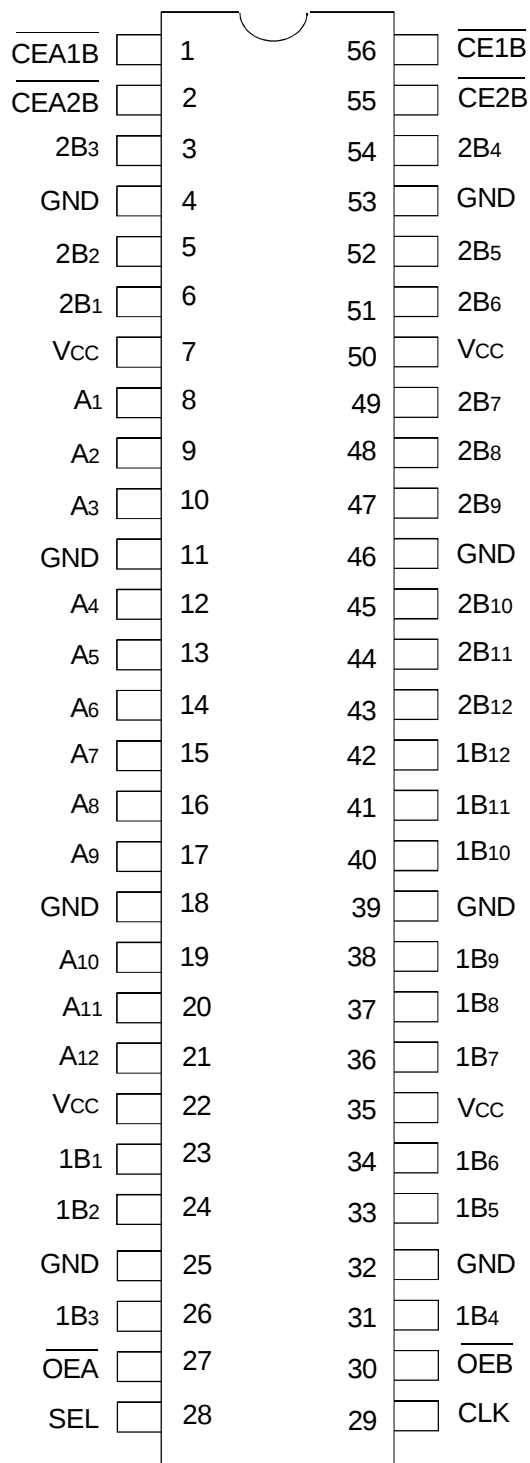


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INDUSTRIAL TEMPERATURE RANGE

JANUARY 2004

PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +6.5	V
TSTG	Storage Temperature	−65 to +150	°C
IOUT	DC Output Current	−50 to +50	mA
IIK IOK	Continuous Clamp Current, Vi < 0 or Vo < 0	−50	mA
ICC Iss	Continuous Current through each Vcc or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOU = 0V	6.5	8	pF
CIO	I/O Port Capacitance	VIN = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Signal	I/O	Description
A(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. ⁽¹⁾
1B(1:12)	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. ⁽¹⁾
2B(1:12)	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. ⁽¹⁾
CLK	I	Clock Input.
$\overline{\text{CEA1B}}$	I	Clock Enable Input for the A-1B Register. If $\overline{\text{CEA1B}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
$\overline{\text{CEA2B}}$	I	Clock Enable Input for the A-2B Register. If $\overline{\text{CEA2B}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
$\overline{\text{CE1B}}$	I	Clock Enable Input for the 1B-A Register. If $\overline{\text{CE1B}}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).
$\overline{\text{CE2B}}$	I	Clock Enable Input for the 2B-A Register. If $\overline{\text{CE2B}}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).
SEL	I	1B or 2B Part Selection. When HIGH during the rising edge of CLK, SEL enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, SEL enables data transfer from 2B Port to A Port.
$\overline{\text{OE A}}$	I	Synchronous Output Enable for A Port (Active LOW).
$\overline{\text{OE B}}$	I	Synchronous Output Enable for 1B Port and 2B Port (Active LOW).

NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES⁽¹⁾

Inputs							Outputs
1Bx	2Bx	SEL	$\overline{\text{CE1B}}$	$\overline{\text{CE2B}}$	$\overline{\text{OE A}}$	CLK	Ax
H	X	H	L	X	L	↑	H
L	X	H	L	X	L	↑	L
X	X	H	H	X	L	↑	A ⁽²⁾
X	H	L	X	L	L	↑	H
X	L	L	X	L	L	↑	L
X	X	L	X	H	L	↑	A ⁽²⁾
X	X	X	X	X	H	↑	Z

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- A, B = Output level before the indicated steady-state input conditions were established.

Inputs					Outputs	
Ax	$\overline{\text{CEA1B}}$	$\overline{\text{CEA2B}}$	$\overline{\text{OE B}}$	CLK	1Bx	2Bx
H	L	L	L	↑	H	H
L	L	L	L	↑	L	L
H	L	H	L	↑	H	B ⁽²⁾
L	L	H	L	↑	L	B ⁽²⁾
H	H	L	L	↑	B ⁽²⁾	H
L	H	L	L	↑	B ⁽²⁾	L
X	H	H	L	↑	B ⁽²⁾	B ⁽²⁾
X	X	X	H	↑	Z	Z
X	X	X	L	↑	Active	Active

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	500	μA

NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	—	—	—	μA
			$V_I = 0.7\text{V}$	—	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

NOTES:

- Pins with Bus-Hold are identified in the pin description.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.
TA = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Bus Exchanger Outputs enabled	CL = 0pF, f = 10Mhz		pF
CPD	Power Dissipation Capacitance per Bus Exchanger Outputs disabled			

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay CLK to 1Bx or CLK to 2Bx	1.5	6.6	1.5	5.7	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to Ax	1.5	7	1.5	5.8	ns
	SEL stable, $\overline{\text{CE}}\text{x}\overline{\text{B}}$ Enabled	1.5	7.5	1.5	6.5	
	SEL changing, $\overline{\text{CE}}\text{x}\overline{\text{B}}$ Disabled	1.5	7.6	1.5	6.6	
t _{PZH} t _{PZL}	Output Enable Time CLK to Ax, CLK to 1Bx, or CLK to 2Bx	1.5	6.8	1.5	5.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to Ax, CLK to 1Bx, or CLK to 2Bx	1.5	6.6	1.5	6.6	ns
t _{SU}	Set-Up Time, HIGH or LOW Data to CLK	1.5	—	1.5	—	ns
t _{SU}	Set-Up Time, $\overline{\text{OE}}\overline{\text{A}}$ to CLK, $\overline{\text{OE}}\overline{\text{B}}$ to CLK	1.5	—	1.5	—	ns
t _{SU}	Set-Up Time, SEL to CLK	1.5	—	1.5	—	ns
t _{SU}	Set-Up Time, $\overline{\text{CE}}\text{A}1\overline{\text{B}}$ to CLK, $\overline{\text{CE}}1\overline{\text{B}}$ to CLK , $\overline{\text{CE}}2\overline{\text{B}}$ to CLK, or $\overline{\text{CE}}\text{A}2\overline{\text{B}}$ to CLK	1.8	—	1.8	—	ns
t _H	Hold Time, CLK to Data	1	—	1	—	ns
t _H	Hold Time, CLK to $\overline{\text{OE}}\overline{\text{A}}$, CLK to $\overline{\text{OE}}\overline{\text{B}}$, CLK to SEL	1	—	1	—	ns
t _H	Hold Time, CLK to $\overline{\text{CE}}\text{A}1\overline{\text{B}}$, CLK to $\overline{\text{CE}}1\overline{\text{B}}$, CLK to $\overline{\text{CE}}2\overline{\text{B}}$, CLK to $\overline{\text{CE}}\text{A}2\overline{\text{B}}$	0.7	—	0.7	—	ns
t _W	Pulse Width, CLK HIGH	2.5	—	2.5	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	500	—	500	ps

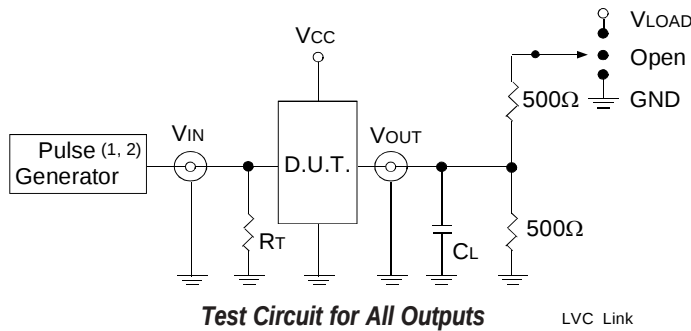
NOTES:

- See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
- Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

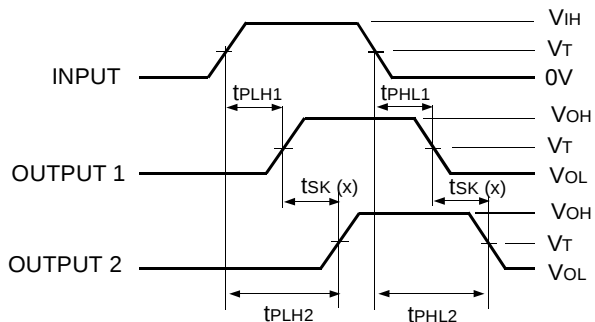
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2\text{ns}$; $t_f \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

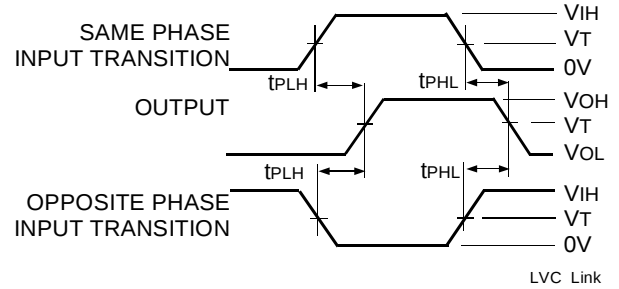


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

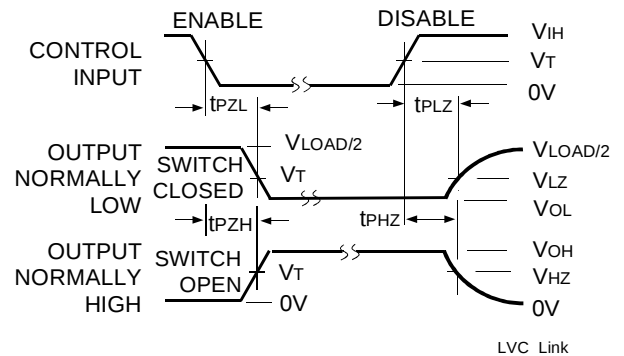
Output Skew - $t_{SK}(x)$

NOTES:

1. For $t_{SK}(0)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.



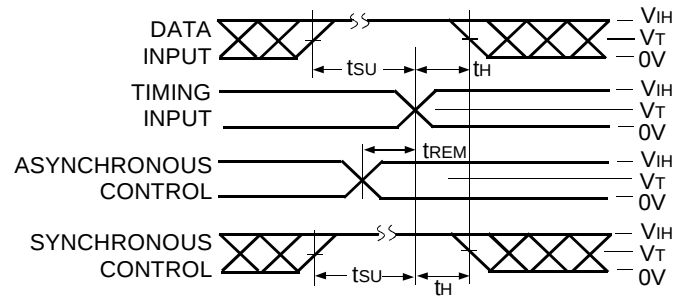
Propagation Delay



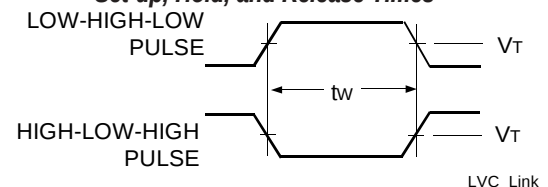
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package
						PA	Thin Shrink Small Outline Package
					276A		12-Bit Synchronous Bus Exchanger
				16			Double-Density, $\pm 24\text{mA}$
			H				Bus-hold
				74			-40°C to $+85^{\circ}\text{C}$



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