



3.3V CMOS OCTAL EDGE-TRIGGERED D-TYPE FLIP- FLOP WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

IDT74LVC574A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-rail output swing for increased noise margin
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SOIC, SSOP, QSOP, and TSSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

The LVC574A octal edge-triggered D-type flip-flop is built using advanced dual-metal CMOS technology. The device features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The LVC574A is particularly suitable for implementing buffer registers, input-output (I/O) ports, bidirectional bus drivers, and working registers.

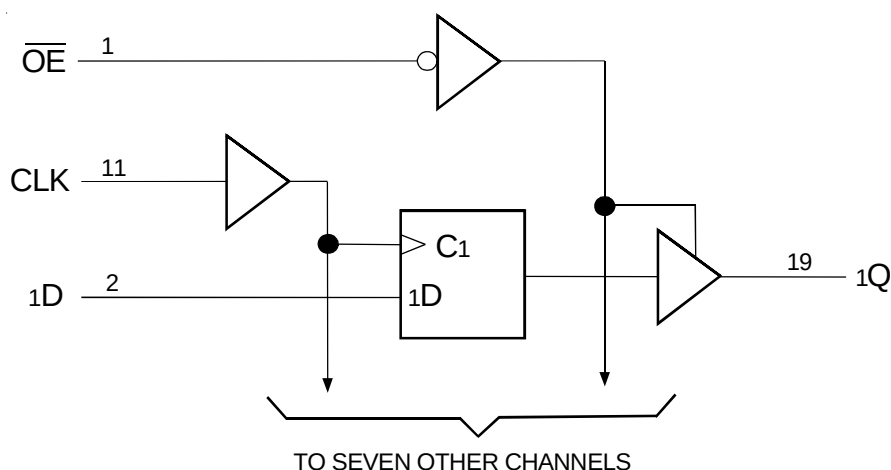
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

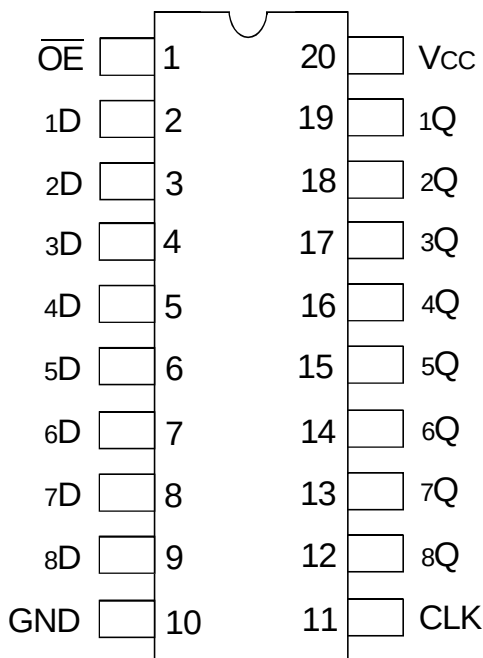
The LVC574A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +6.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	−50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Inputs (Active LOW)
CLK	Clock Input
x _D	Data Inputs
x _Q	3-State Outputs

FUNCTION TABLE (EACH FLIP-FLOP)⁽¹⁾

Inputs			Outputs
$\overline{OE}$	CLK	x _D	x _Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ⁽²⁾
H	X	X	Z

NOTES:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	500	μA

NOTES:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3\text{V}$		2.4	—	
		$V_{CC} = 3\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
 $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Flip-Flop Outputs enabled	$C_L = 0pF$, $f = 10MHz$	43	pF
CPD	Power Dissipation Capacitance per Flip-Flop Outputs disabled		15	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CLK to xQ	—	8	2.2	7	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OE}$ to xQ	—	8.5	1.5	7.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OE}$ to xQ	—	7	1.7	6.4	ns
t _w	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	ns
t _{su}	Set-up Time, data before CLK↑	2	—	2	—	ns
t _h	Hold Time, data after CLK↑	1.5	—	1.5	—	ns
t _{sk(0)}	Output Skew ⁽²⁾	—	—	—	1	ns

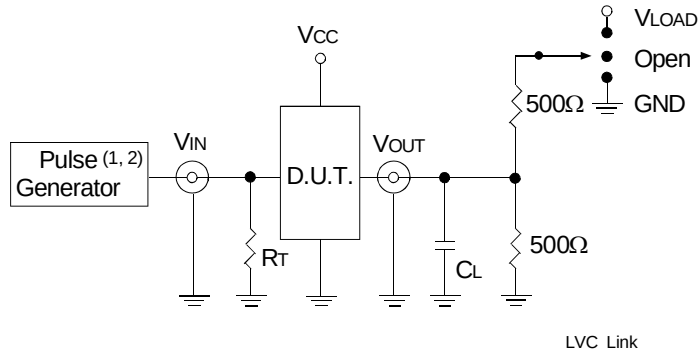
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

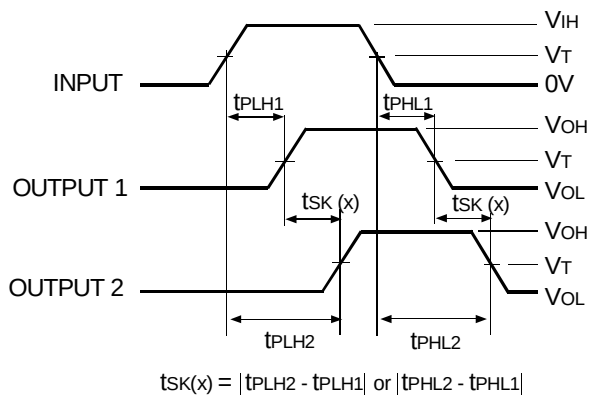
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_f ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_f ≤ 2ns.

SWITCH POSITION

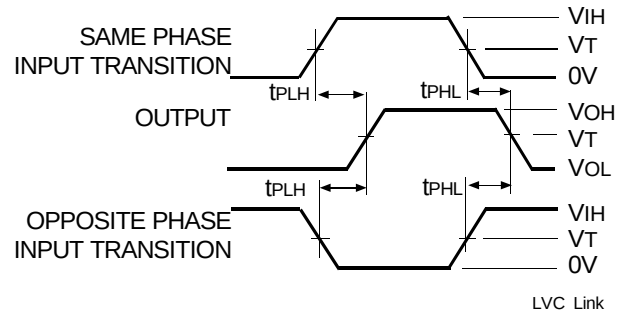
Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



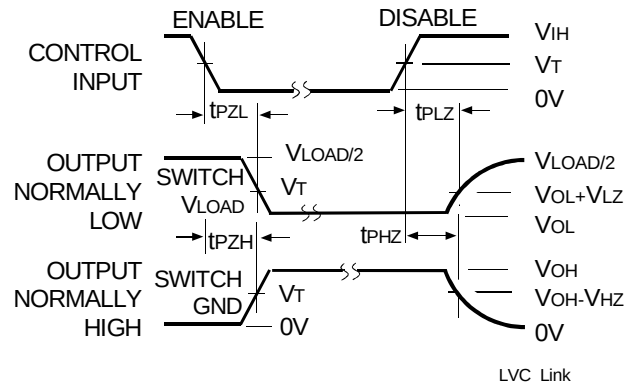
Output Skew - tsk(x)

NOTES:

1. For tsk(0) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



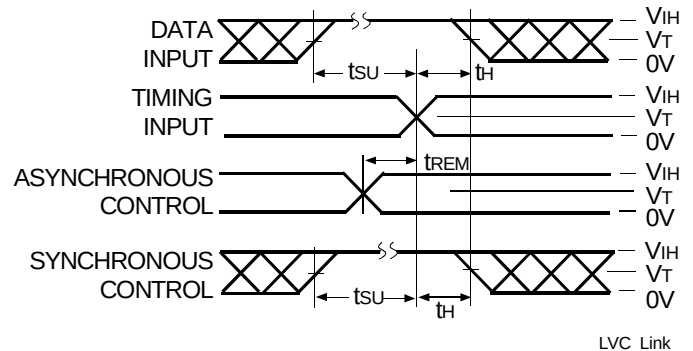
Propagation Delay



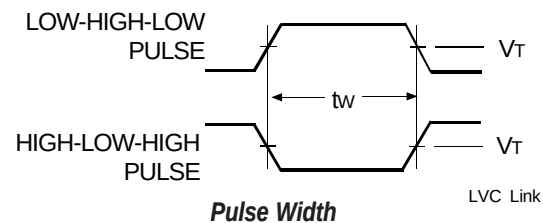
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT	XX	LVC	X	XXXX	XX	
	Temp. Range		Bus-Hold	Device Type	Package	
					SO	Small Outline IC (gull wing)
					PY	Shrink Small Outline Package
					Q	Quarter Size Small Outline Package
					PG	Thin Shrink Small Outline Package
				574A		Octal Edge-Triggered D-Type Flip-Flop with 3-State Outputs, $\pm 24\text{mA}$
			Blank			No Bus-hold
			74			-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459