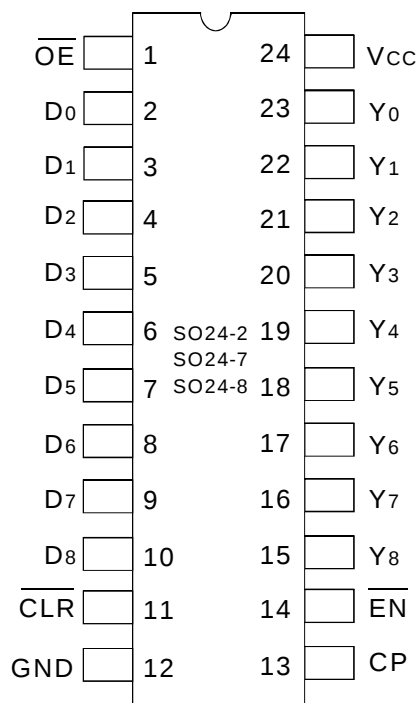




The FCT823T high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

DSC-5487/1

PIN CONFIGURATION



SOIC/ SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Inputs and Vcc terminals only.
- Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOU = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	I/O	Description
Dx	I	D Flip-Flop Data Inputs
CLR	I	When the clear input is LOW and OE is LOW, the Qx outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Yx	O	Register 3-State Outputs
EN	I	Clock Enable. When the clock enable is LOW, data on the Dx output is transferred to the Qx output on the LOW-to-HIGH transition. When the clock enable is HIGH, the Qx outputs do not change state, regardless of the data or clock input transitions.
OE	I	Output Control. When the OE is HIGH, the Yx outputs are in the high-impedance state. When the OE is LOW, the TRUE register data is present at the Yx outputs.

FUNCTION TABLE⁽¹⁾

Inputs					Internal/Outputs		Function
OE	CLR	EN	Dx	CP	Qx	Yx	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_I = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48\text{mA}$	—	0.3	0.5	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \overline{EN} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \overline{EN} = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2	5.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \overline{EN} = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6	16.3 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input; ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$f_i = \text{Output Frequency}$

$N_i = \text{Number of Outputs at } f_i$

All currents are in milliamps and all frequencies are in megahertz.

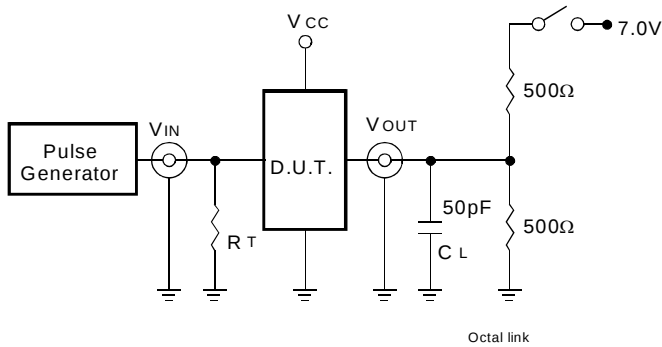
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT823AT		FCT823CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Yx ($\overline{OE} = \text{LOW}$)	CL = 50pF RL = 500Ω	1.5	10	1.5	6	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	20	1.5	12.5	ns
t _{SU}	Set-up Time HIGH or LOW Dx to CP	CL = 50pF	4	—	3	—	ns
t _H	Hold Time HIGH or LOW Dx to CP	RL = 500Ω	2	—	1.5	—	ns
t _{SU}	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4	—	3	—	ns
t _H	Hold Time HIGH or LOW $\overline{EN}$ to CP		2	—	0	—	ns
t _{PHL}	Propagation Delay, $\overline{CLR}$ to Yx		1.5	14	1.5	8	ns
t _{REM}	Recovery Time $\overline{CLR}$ to CP		6	—	6	—	ns
t _W	Clock Pulse Width HIGH or LOW		7	—	6	—	ns
t _W	$\overline{CLR}$ Pulse Width LOW		6	—	6	—	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OE}$ to Yx	CL = 50pF RL = 500Ω	1.5	12	1.5	7	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23	1.5	12.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OE}$ to Yx	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	7	1.5	6	ns
		CL = 50pF RL = 500Ω	1.5	8	1.5	6.5	ns

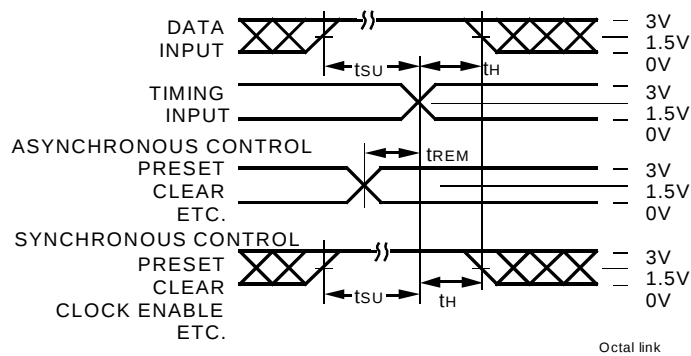
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

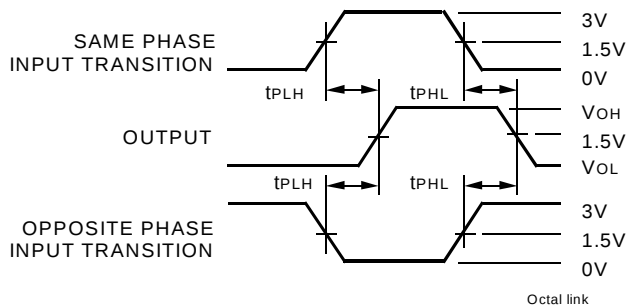
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



Propagation Delay

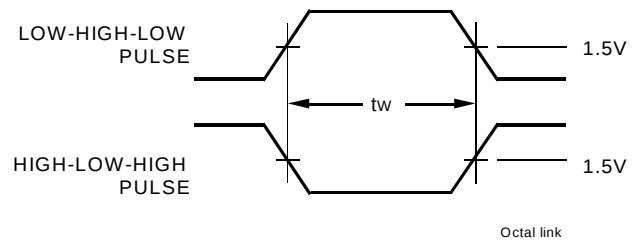
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

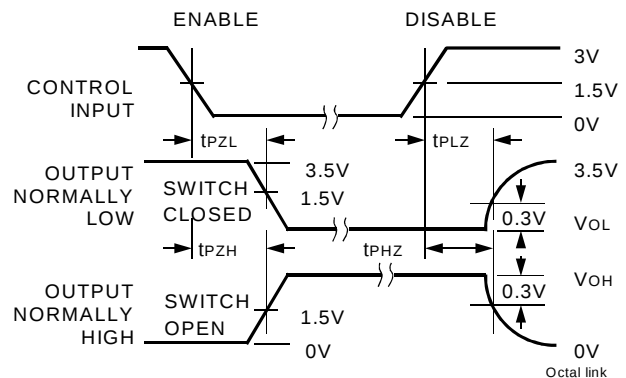
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

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graph LR
    Root[74] --- Branch1(( ))
    Branch1 --- FCT[FCT]
    Branch1 --- TempRange[Temp. Range]
    FCT --- Branch2(( ))
    Branch2 --- 823AT[823AT]
    Branch2 --- 823CT[823CT]
    823AT --- BusInterface[Bus Interface Register]
    823CT --- BusInterface
    TempRange --- Branch3(( ))
    Branch3 --- SO[SO]
    Branch3 --- PY[PY]
    Branch3 --- Q[Q]
    SO --- SO242[Small Outline IC SO24-2]
    PY --- SSOP[Shrink Small Outline Package SO24-7]
    Q --- QSOP[Quarter-size Small Outline Package SO24-8]
  
```

74 -40°C to +85°C

823AT 823CT Bus Interface Register

SO PY Q Small Outline IC (SO24-2)
Shrink Small Outline Package (SO24-7)
Quarter-size Small Outline Package (SO24-8)

