

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(0)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Balanced Output Drivers:  $\pm 24mA$
- Reduced system switching noise
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.6V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull up resistors
- Available in SSOP and TSSOP packages

DESCRIPTION:

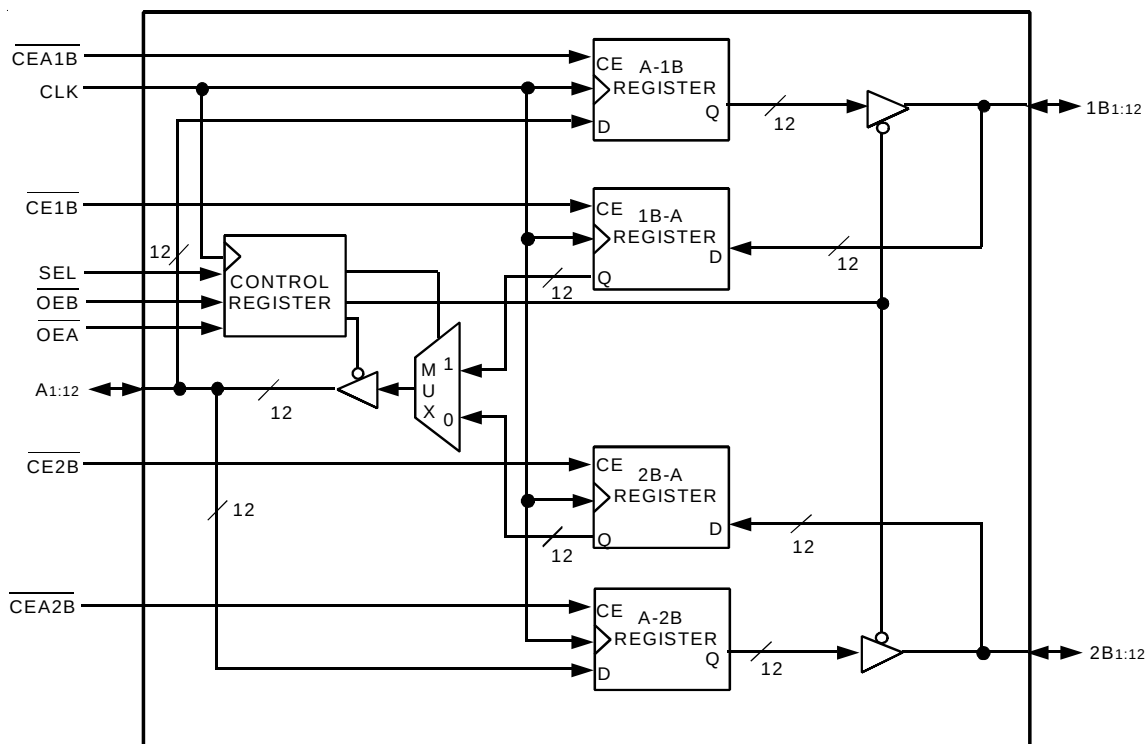
The FCT162H272T synchronous tri-port bus exchangers are high-speed, bidirectional, 12-bit, registered, bus multiplexers for use in synchronous memory interleaving applications. All registers have a common clock and use a clock enable ( $\overline{CE}_{xxx}$ ) on each data register to control data sequencing. The output enables and mux select ( $\overline{OE}_A$ ,  $\overline{OE}_B$  and SEL) are also under synchronous control allowing direction changes to be edge triggered events.

The tri-port bus exchanger has three 12-bit ports. Data may be transferred between the A port and either/both of the B ports. The clock enable ( $\overline{\text{CE1B}}$ ,  $\overline{\text{CE2B}}$ ,  $\overline{\text{CEA1B}}$  and  $\overline{\text{CEA2B}}$ ) inputs control the data storage. Both B ports have a common output enable ( $\overline{\text{OEB}}$ ) to aid in synchronously loading the B registers from the B port.

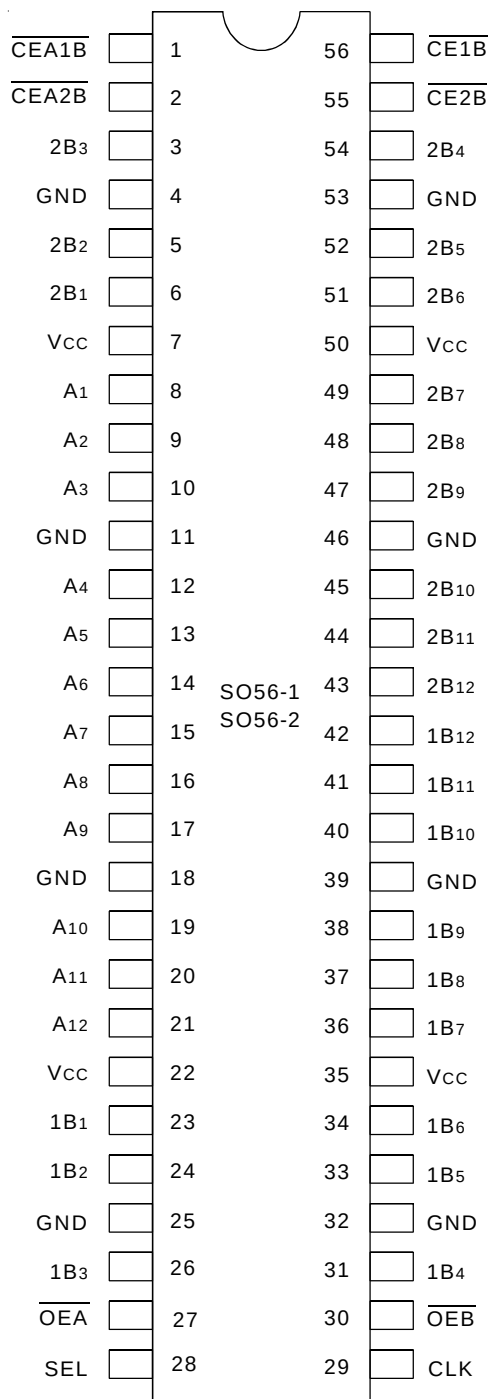
The FCT162H272T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

The FCT162H272T has "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                           | Description                          | Max                          | Unit |
|----------------------------------|--------------------------------------|------------------------------|------|
| V <sub>TERM</sub> <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to 7                    | V    |
| V <sub>TERM</sub> <sup>(3)</sup> | Terminal Voltage with Respect to GND | -0.5 to V <sub>CC</sub> +0.5 | V    |
| T <sub>STG</sub>                 | Storage Temperature                  | -65 to +150                  | °C   |
| I <sub>OUT</sub>                 | DC Output Current                    | -60 to +120                  | mA   |

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 3.5  | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 3.5  | 8    | pF   |

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

| Signal                    | I/O | Description                                                                                                                                                                                                   |
|---------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A(1:12)                   | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. <sup>(1)</sup>                                                                                                                    |
| 1B(1:12)                  | I/O | Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. <sup>(1)</sup>                                                                                                         |
| 2B(1:12)                  | I/O | Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. <sup>(1)</sup>                                                                                                           |
| CLK                       | I   | Clock Input                                                                                                                                                                                                   |
| $\overline{\text{CEA1B}}$ | I   | Clock Enable Input for the A-1B Register. If CEA1B is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).                                                                |
| $\overline{\text{CEA2B}}$ | I   | Clock Enable Input for the A-2B Register. If CEA2B is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).                                                                |
| $\overline{\text{CE1B}}$  | I   | Clock Enable Input for the 1B-A Register. If CE1B is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).                                                                 |
| $\overline{\text{CE2B}}$  | I   | Clock Enable Input for the 2B-A Register. If CE2B is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).                                                                 |
| SEL                       | I   | 1B or 2B Path Selection. When HIGH during the rising edge of CLK, SEL enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, SEL enables data transfer from 2B Port to A Port. |
| $\overline{\text{OE A}}$  | I   | Synchronous Output Enable for A Port (Active LOW).                                                                                                                                                            |
| $\overline{\text{OE B}}$  | I   | Synchronous Output Enable for 1B Port and 2B Port (Active LOW).                                                                                                                                               |

### NOTE:

1. On FCT162H272T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

## FUNCTION TABLES<sup>(2)</sup>

| Inputs |    |     |                          |                          |                          |     | Output           |
|--------|----|-----|--------------------------|--------------------------|--------------------------|-----|------------------|
| 1B     | 2B | SEL | $\overline{\text{CE1B}}$ | $\overline{\text{CE2B}}$ | $\overline{\text{OE A}}$ | CLK | A                |
| H      | X  | H   | L                        | X                        | L                        | ↑   | H                |
| L      | X  | H   | L                        | X                        | L                        | ↑   | L                |
| X      | X  | H   | H                        | X                        | L                        | ↑   | A <sup>(1)</sup> |
| X      | H  | L   | X                        | L                        | L                        | ↑   | H                |
| X      | L  | L   | X                        | L                        | L                        | ↑   | L                |
| X      | X  | L   | X                        | H                        | L                        | ↑   | A <sup>(1)</sup> |
| X      | X  | X   | X                        | X                        | H                        | ↑   | Z                |

| Inputs |                           |                           |                          |     | Outputs          |                  |
|--------|---------------------------|---------------------------|--------------------------|-----|------------------|------------------|
| A      | $\overline{\text{CEA1B}}$ | $\overline{\text{CEA2B}}$ | $\overline{\text{OE B}}$ | CLK | 1B               | 2B               |
| H      | L                         | L                         | L                        | ↑   | H                | H                |
| L      | L                         | L                         | L                        | ↑   | L                | L                |
| H      | L                         | H                         | L                        | ↑   | H                | B <sup>(1)</sup> |
| L      | L                         | H                         | L                        | ↑   | L                | B <sup>(1)</sup> |
| H      | H                         | L                         | L                        | ↑   | B <sup>(1)</sup> | H                |
| L      | H                         | L                         | L                        | ↑   | B <sup>(1)</sup> | L                |
| X      | H                         | H                         | L                        | ↑   | B <sup>(1)</sup> | B <sup>(1)</sup> |
| X      | X                         | X                         | H                        | ↑   | Z                | Z                |
| X      | X                         | X                         | L                        | ↑   | Active           | Active           |

### NOTES:

1. Output level before the indicated steady-state input conditions were established.

2. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Z = High-Impedance

↑ = LOW-to-HIGH Transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol                                                   | Parameter                                                                |                               | Test Conditions <sup>(1)</sup>                                     |                                  | Min. | Typ. <sup>(2)</sup> | Max. | Unit |
|----------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------|--------------------------------------------------------------------|----------------------------------|------|---------------------|------|------|
| V <sub>IH</sub>                                          | Input HIGH Level                                                         |                               | Guaranteed Logic HIGH Level                                        |                                  | 2    | —                   | —    | V    |
| V <sub>IL</sub>                                          | Input LOW Level                                                          |                               | Guaranteed Logic LOW Level                                         |                                  | —    | —                   | 0.8  | V    |
| I <sub>IH</sub>                                          | Input<br>HIGH<br>Current <sup>(4)</sup>                                  | Standard Input <sup>(5)</sup> | V <sub>CC</sub> = Max.                                             | V <sub>I</sub> = V <sub>CC</sub> | —    | —                   | ±1   | μA   |
|                                                          |                                                                          | Standard I/O <sup>(5)</sup>   |                                                                    |                                  | —    | —                   | ±1   |      |
|                                                          |                                                                          | Bus-hold Input                |                                                                    |                                  | —    | —                   | ±100 |      |
|                                                          |                                                                          | Bus-hold I/O                  |                                                                    |                                  | —    | —                   | ±100 |      |
| I <sub>IL</sub>                                          | Input<br>LOW<br>Current <sup>(4)</sup>                                   | Standard Input <sup>(5)</sup> |                                                                    | V <sub>I</sub> = GND             | —    | —                   | ±1   |      |
|                                                          |                                                                          | Standard I/O <sup>(5)</sup>   |                                                                    |                                  | —    | —                   | ±1   |      |
|                                                          |                                                                          | Bus-hold Input                |                                                                    |                                  | —    | —                   | ±100 |      |
|                                                          |                                                                          | Bus-hold I/O                  |                                                                    |                                  | —    | —                   | ±100 |      |
| I <sub>BHH</sub><br>I <sub>BHL</sub>                     | Bus-hold Sustain<br>Current <sup>(4)</sup>                               | Bus-hold Input                | V <sub>CC</sub> = Min.                                             | V <sub>I</sub> = 2V              | −50  | —                   | —    | μA   |
|                                                          |                                                                          | V <sub>I</sub> = 0.8V         |                                                                    | 50                               | —    | —                   |      |      |
| I <sub>OZH</sub>                                         | High Impedance Output Current<br>(3-State Output pins) <sup>(5, 6)</sup> |                               | V <sub>CC</sub> = Max.                                             | V <sub>O</sub> = 2.7V            | —    | —                   | ±1   | μA   |
| I <sub>OZL</sub>                                         |                                                                          |                               |                                                                    | V <sub>O</sub> = 0.5V            | —    | —                   | ±1   |      |
| V <sub>IK</sub>                                          | Clamp Diode Voltage                                                      |                               | V <sub>CC</sub> = Min., I <sub>IN</sub> = −18mA                    |                                  | —    | −0.7                | −1.2 | V    |
| I <sub>OS</sub>                                          | Short Circuit Current                                                    |                               | V <sub>CC</sub> = Max., V <sub>O</sub> = GND <sup>(3)</sup>        |                                  | −80  | −140                | −250 | mA   |
| V <sub>H</sub>                                           | Input Hysteresis                                                         |                               | —                                                                  |                                  | —    | 100                 | —    | mV   |
| I <sub>CCL</sub><br>I <sub>CCH</sub><br>I <sub>CCZ</sub> | Quiescent Power Supply Current                                           |                               | V <sub>CC</sub> = Max.<br>V <sub>IN</sub> = GND or V <sub>CC</sub> |                                  | —    | 5                   | 500  | μA   |

## OUTPUT DRIVE CHARACTERISTICS

| Symbol    | Parameter           | Test Conditions <sup>(1)</sup>                                                    |                         | Min. | Typ. <sup>(2)</sup> | Max. | Unit |
|-----------|---------------------|-----------------------------------------------------------------------------------|-------------------------|------|---------------------|------|------|
| $I_{ODL}$ | Output LOW Current  | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$ |                         | 60   | 115                 | 200  | mA   |
| $I_{ODH}$ | Output HIGH Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$ |                         | −60  | −115                | −200 | mA   |
| $V_{OH}$  | Output HIGH Voltage | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$                    | $I_{OH} = -24\text{mA}$ | 2.4  | 3.3                 | —    | V    |
| $V_{OL}$  | Output LOW Voltage  | $V_{CC} = \text{Min.}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$                    | $I_{OH} = 24\text{mA}$  | —    | 0.3                 | 0.55 | V    |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- This test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .
- Does not include Bus-Hold I/O pins.

## POWER SUPPLY CHARACTERISTICS

| Symbol          | Parameter                                         | Test Conditions <sup>(1)</sup>                                                                                                                                                                                                                     |                                            | Min. | Typ. <sup>(2)</sup> | Max.                | Unit                 |
|-----------------|---------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------|---------------------|---------------------|----------------------|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC} = \text{Max.}$<br>$V_{IN} = 3.4V^{(3)}$                                                                                                                                                                                                    |                                            | —    | 0.5                 | 1.5                 | mA                   |
| $I_{CCD}$       | Dynamic Power Supply Current <sup>(4)</sup>       | $V_{CC} = \text{Max.}$<br>Outputs Open<br>One Output Port Enabled<br>$\overline{CE}_{xx} = \text{GND}$<br>One Input Bit Toggling<br>One Output Bit Toggling<br>50% Duty Cycle                                                                      | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 60                  | 100                 | $\mu A / \text{MHz}$ |
| $I_C$           | Total Power Supply Current <sup>(6)</sup>         | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{OE}_x = \overline{CE}_{xx} = \text{GND}$<br>One Input Bit Toggling<br>One Output Bit Toggling<br>$f_i = 5\text{MHz}$<br>50% Duty Cycle           | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 0.6                 | 1                   | mA                   |
|                 |                                                   |                                                                                                                                                                                                                                                    | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 1.1                 | 2.5                 |                      |
|                 |                                                   | $V_{CC} = \text{Max.}$<br>Outputs Open<br>$f_{CP} = 10\text{MHz}$<br>50% Duty Cycle<br>$\overline{OE}_x = \overline{CE}_{xx} = \text{GND}$<br>Twelve Input Bits Toggling<br>Twelve Output Bits Toggling<br>$f_i = 2.5\text{MHz}$<br>50% Duty Cycle | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 2.1                 | 3.5 <sup>(5)</sup>  |                      |
|                 |                                                   |                                                                                                                                                                                                                                                    | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 5.4                 | 13.3 <sup>(5)</sup> |                      |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

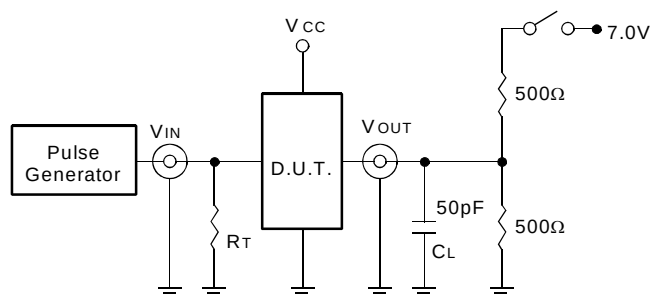
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol                               | Parameter                                                                                                             |                                            | Condition <sup>(1)</sup> | FCT162H272AT        |      | FCT162H272CT        |      | Unit |
|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------------------|--------------------------|---------------------|------|---------------------|------|------|
|                                      |                                                                                                                       |                                            |                          | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CLK to 1Bx or CLK to 2Bx                                                                         |                                            | CL = 50pF<br>RL = 500Ω   | 1.5                 | 5.8  | 1.5                 | 5.2  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>CLK to Ax                                                                                        | SEL Stable<br>CE <sub>ExB</sub> Enabled    |                          | 1.5                 | 6    | 1.5                 | 5.4  | ns   |
|                                      |                                                                                                                       | SEL Changing<br>CE <sub>ExB</sub> Disabled |                          | 1.5                 | 6    | 1.5                 | 5.4  | ns   |
|                                      |                                                                                                                       | SEL Changing<br>CE <sub>ExB</sub> Enabled  |                          | 1.5                 | 7.6  | 1.5                 | 6.6  | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>CLK to Ax, CLK to 1Bx, or CLK to 2Bx                                                            |                                            |                          | 1.5                 | 7.7  | 1.5                 | 6.8  | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>CLK to Ax, CLK to 1Bx, or CLK to 2Bx                                                           |                                            |                          | 1.5                 | 6.4  | 1.5                 | 6    | ns   |
| t <sub>SU</sub>                      | Set-Up Time, HIGH or LOW Data to CLK                                                                                  |                                            |                          | 2                   | —    | 2                   | —    | ns   |
| t <sub>SU</sub>                      | Set-Up Time, OE <sub>A</sub> to CLK, OE <sub>B</sub> to CLK                                                           |                                            |                          | 2                   | —    | 2                   | —    | ns   |
| t <sub>SU</sub>                      | Set-Up Time, SEL to CLK                                                                                               |                                            |                          | 2                   | —    | 2                   | —    | ns   |
| t <sub>SU</sub>                      | Set-Up Time, CE <sub>A1B</sub> to CLK, CE <sub>1B</sub> to CLK, CE <sub>2B</sub> to CLK, or CE <sub>A2B</sub> to CLK  |                                            |                          | 2                   | —    | 2                   | —    | ns   |
| t <sub>H</sub>                       | Hold Time, CLK to Data                                                                                                |                                            |                          | 0                   | —    | 0                   | —    | ns   |
| t <sub>H</sub>                       | Hold Time, CLK to OE <sub>A</sub> ,<br>CLK to OE <sub>B</sub> , CLK to SEL                                            |                                            |                          | 0.5                 | —    | 0.5                 | —    | ns   |
| t <sub>H</sub>                       | Hold Time, CLK to CE <sub>A1B</sub> , CLK to CE <sub>1B</sub> ,<br>CLK to CE <sub>2B</sub> , CLK to CE <sub>A2B</sub> |                                            |                          | 0                   | —    | 0                   | —    | ns   |
| t <sub>w</sub>                       | Pulse Width, CLK HIGH <sup>(3)</sup>                                                                                  |                                            |                          | 3                   | —    | 3                   | —    | ns   |
| t <sub>SK(o)</sub>                   | Output Skew <sup>(4)</sup>                                                                                            |                                            |                          | —                   | 0.5  | —                   | 0.5  | ns   |

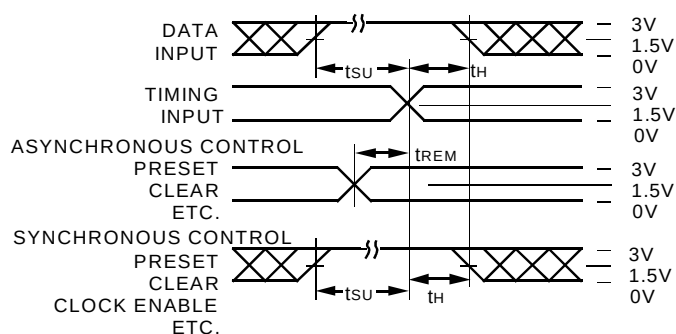
### NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

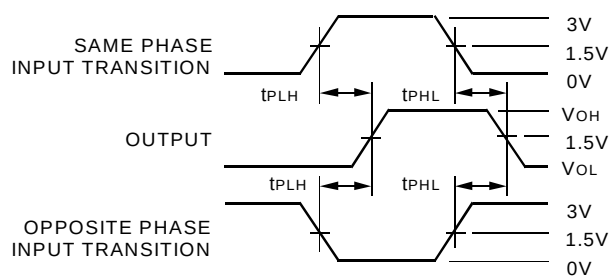
## TEST CIRCUITS AND WAVEFORMS



**Test Circuits for All Outputs**



**Set-up, Hold, and Release Times**



**Propagation Delay**

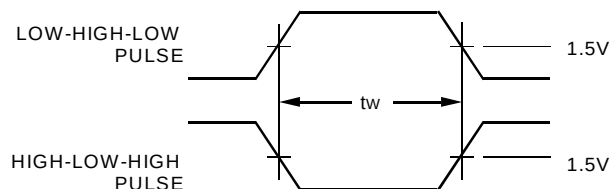
## SWITCH POSITION

| Test                                    | Switch |
|-----------------------------------------|--------|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests                         | Open   |

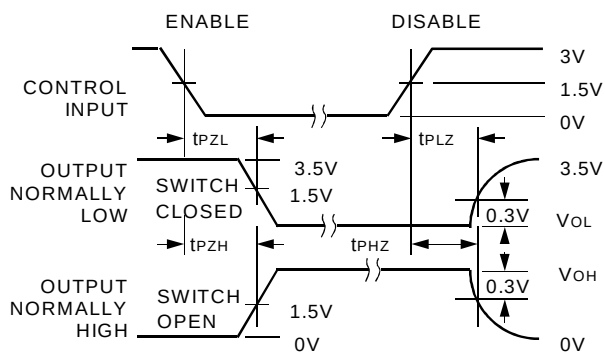
### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



**Pulse Width**

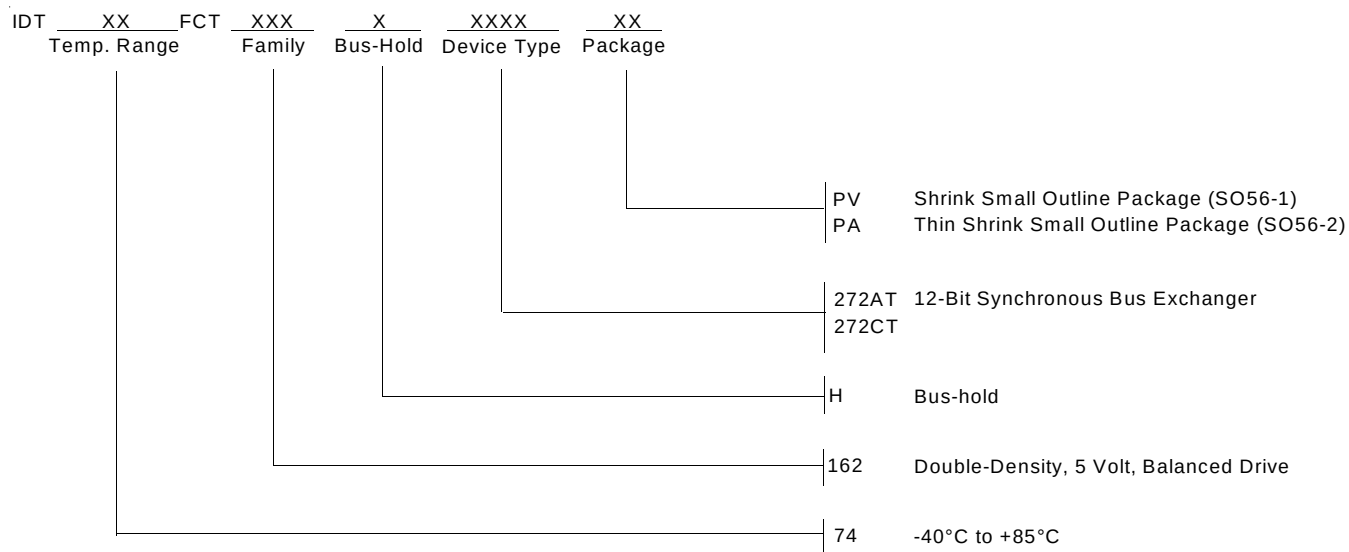


**Enable and Disable Times**

### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



### CORPORATE HEADQUARTERS

2975 Stender Way  
Santa Clara, CA 95054

### for SALES:

800-345-7015 or 408-727-6116  
fax: 408-492-8674  
www.idt.com

### for Tech Support:

logichelp@idt.com  
(408) 654-6459