



FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVER

IDT74FCT162H245AT/CT

FEATURES:

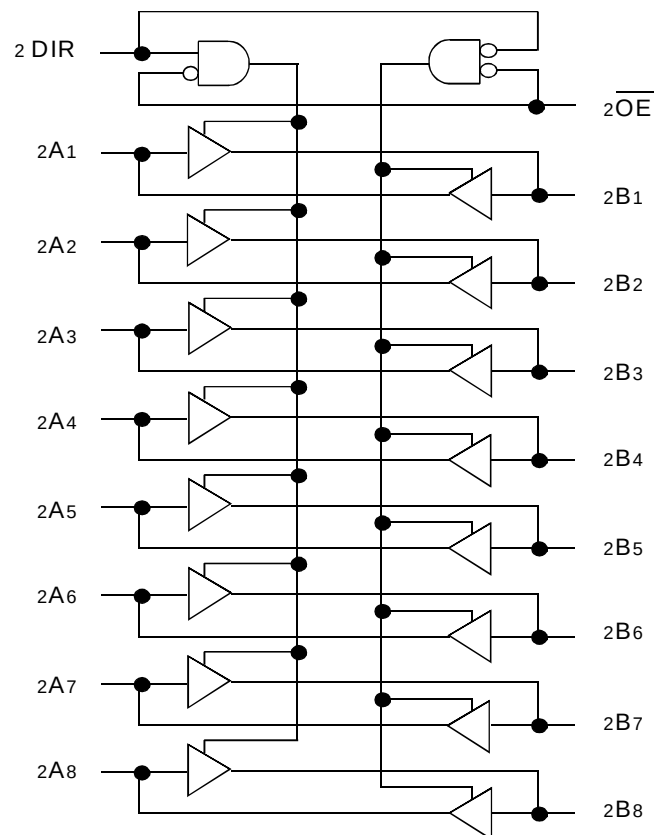
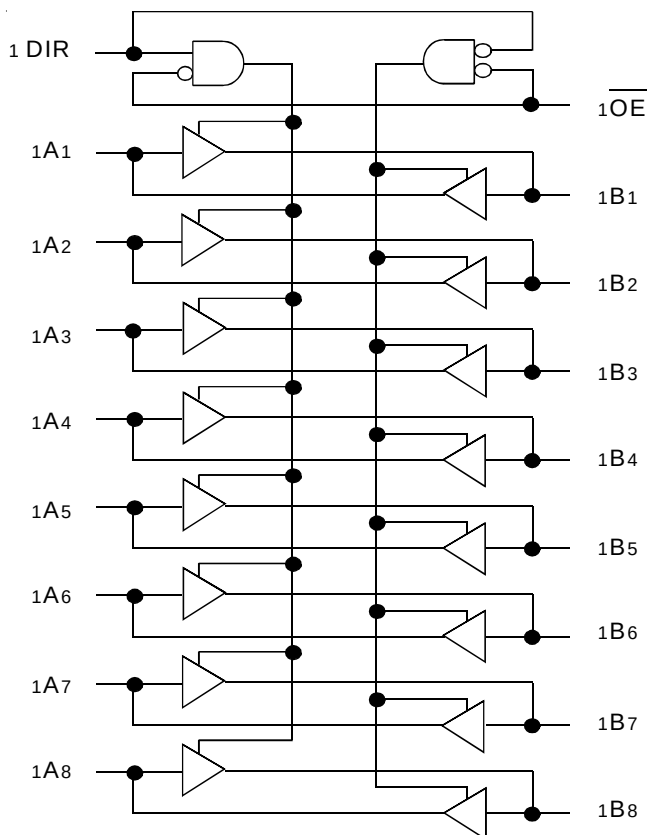
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull up resistors
- Available in SSOP and TSSOP packages

DESCRIPTION:

The FCT162H245T 16-bit transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin ($\overline{xOE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

The FCT162H245T has "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

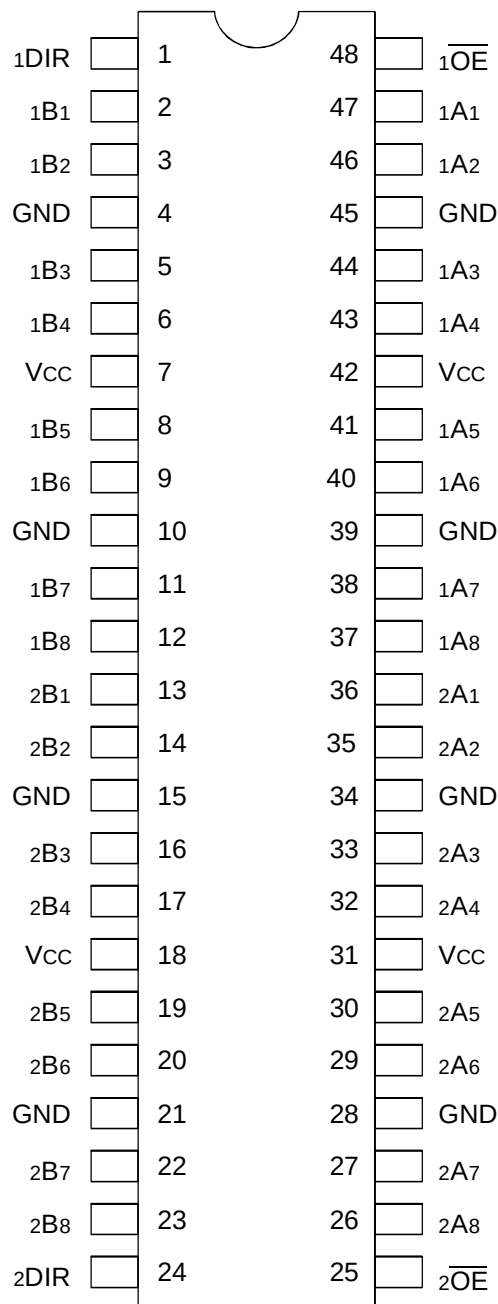


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INDUSTRIAL TEMPERATURE RANGE

NOVEMBER 2002

PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to 7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT and FCT166XXXT (A-Port) Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT and FCT166XXXT (A-Port).

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
x $\overline{OE}$	Outputs Enable Input (Active LOW)
xDIR	Direction Control Inputs
x A x	Side A Inputs or 3-State Outputs ⁽¹⁾
x B x	Side B Inputs or 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE⁽¹⁾

Inputs		Output
x $\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2	—	—	V
V _{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I _{IL}	Input LOW Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _I = GND	—	—	±1		
		Standard I/O ⁽⁵⁾		—	—	±1		
		Bus-hold Input		—	—	±100		
		Bus-hold I/O		—	—	±100		
I _{BHH}	Bus-hold Sustain	Bus-hold Input	V _{CC} = Min.	V _I = 2V	−50	—	—	μA
I _{BHL}	Current ⁽⁴⁾			V _I = 0.8V	50	—	—	
I _{OZH}	High Impedance Output Current (3-State Output pins) ^(5, 6)		V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}				V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage		V _{CC} = Min., I _{IN} = −18mA		—	−0.7	−1.2	V
I _{OS}	Short Circuit Current		V _{CC} = Max., V _O = GND ⁽³⁾		−80	−140	−250	mA
V _H	Input Hysteresis		—		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current		V _{CC} = Max. V _{IN} = GND or V _{CC}		—	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -24\text{mA}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = 24\text{mA}$	—	0.3	0.55	V

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Pins with Bus-hold are identified in the pin description.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
- Does not include Bus-hold I/O pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = xDIR = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

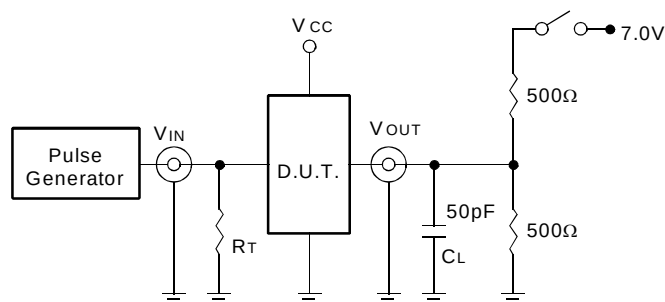
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT162H245AT		FCT162H245CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	4.6	1.5	3.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{xOE}$ to A or B		1.5	6.2	1.5	4.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{xOE}$ to A or B		1.5	5	1.5	4	ns
t_{PZH} t_{PZL}	Output Enable Time $xDIR$ to A or B ⁽³⁾		1.5	6.2	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $xDIR$ to A or B ⁽³⁾		1.5	5	1.5	4	ns
$t_{SK(0)}$	Output Skew ⁽⁴⁾		—	0.5	—	0.5	ns

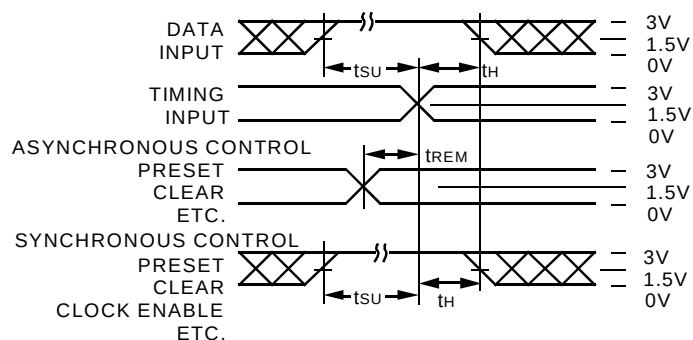
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This parameter is guaranteed but not tested.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

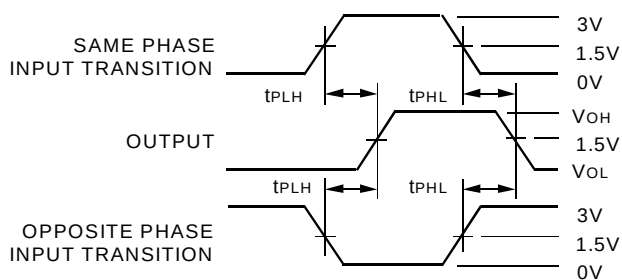
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

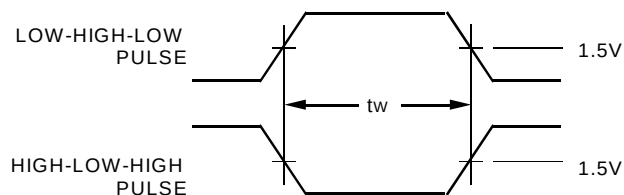
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

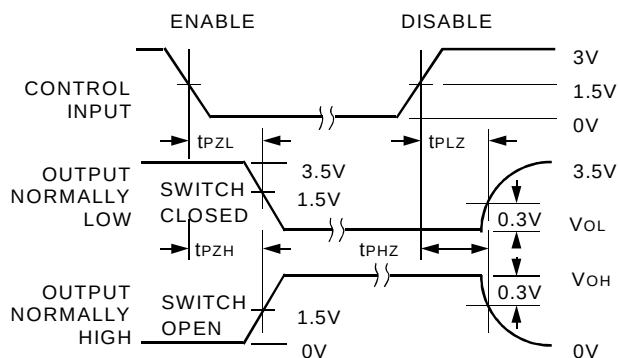
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



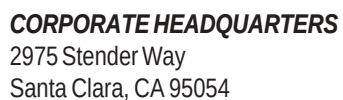
Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

IDT	XX	FCT	XXX	X	XXXX	XX		
Temp. Range	Drive	Bus Hold	Device Type	Package				
						PV PA	Shrink Small Outline Package Thin Shrink Small Outline Package	
						245AT 245CT	16-Bit Bidirectional Transceiver	
						H	Bus-Hold	
						162	Double-Density, 5 Volt, Balanced Drive	
						74	−40°C to +85°C	

4/11/2002	Removed blank speed option
5/22/2002	Removed TVSOP package



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