



FAST CMOS OCTAL TRANSCIVER/ REGISTERS (3-STATE)

IDT74FCT2652AT/CT

FEATURES:

- A and C grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- Resistor outputs (-15mA I_{OH} , 12mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Reduced system switching noise
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

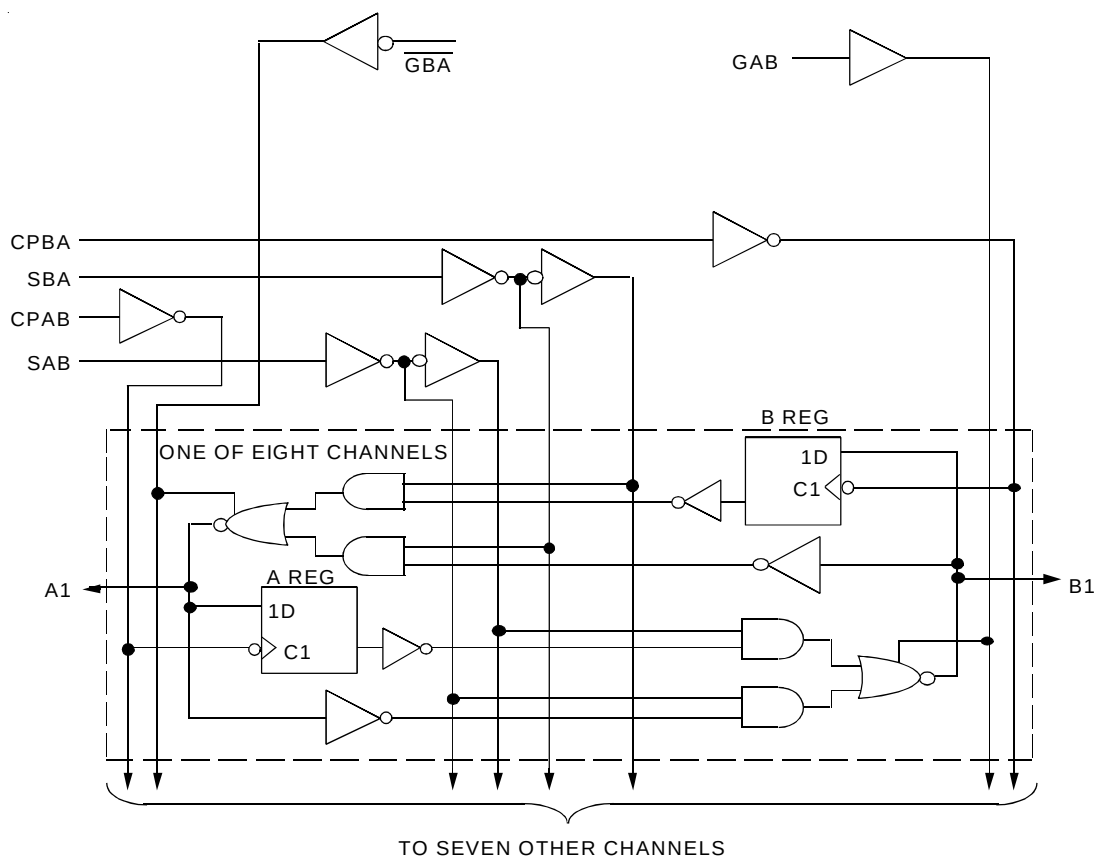
The FCT2652T consists of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The FCT2652T utilizes GAB and $\overline{\text{GBA}}$ signals to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

The FCT2652T have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2652T parts are plug-in replacements for FCT652T parts.

FUNCTIONAL BLOCK DIAGRAM

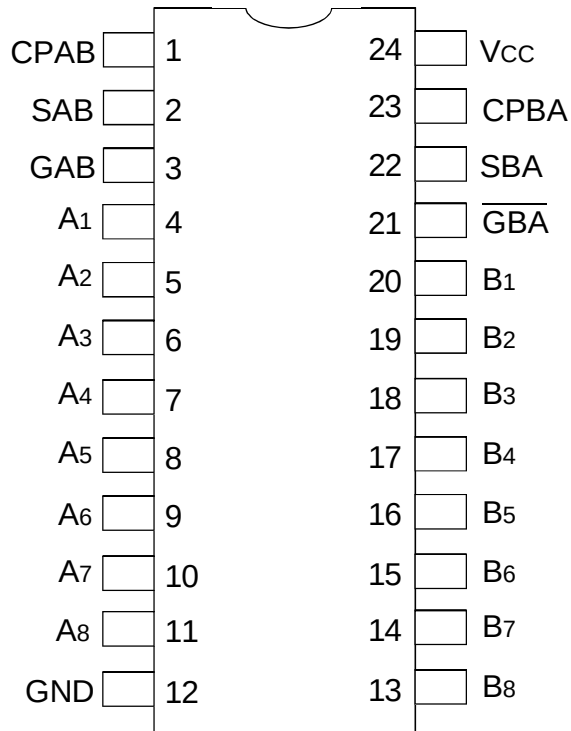


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INDUSTRIAL TEMPERATURE RANGE

AUGUST 2000

PIN CONFIGURATION



SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
A1 - A8	Data Register A Inputs Data Register B Output
B1 - B8	Data Register B Inputs Data Register A Output
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
GAB, GBA	Output Enable Inputs

FUNCTION TABLE (1)

Inputs						Data I/O		Operation
GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA	A1 - A8	B1 - B8	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified ⁽²⁾	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified ⁽²⁾	Input	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus Stored B Data to A Bus

NOTES:

1. H = HIGH

L = LOW

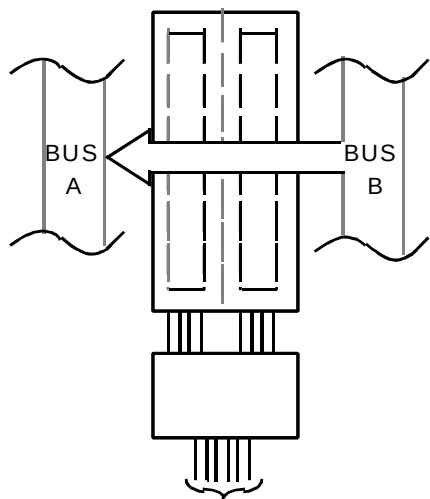
X = Don't Care

↑ = LOW-to-HIGH transition.

Select control = L: clocks can occur simultaneously.

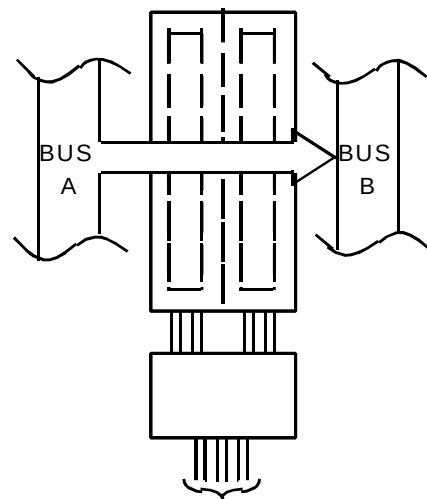
Select control = H: clocks must be staggered in order to load both registers.

2. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{\text{GBA}}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.



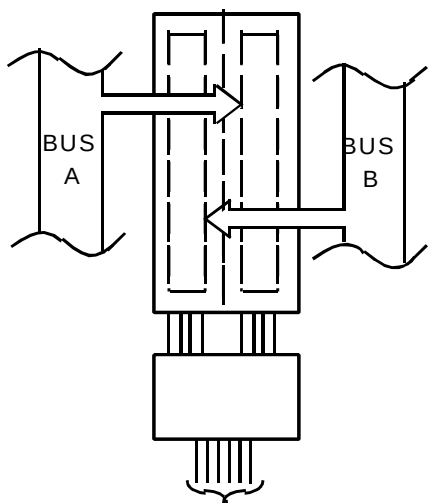
GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer Bus B to A



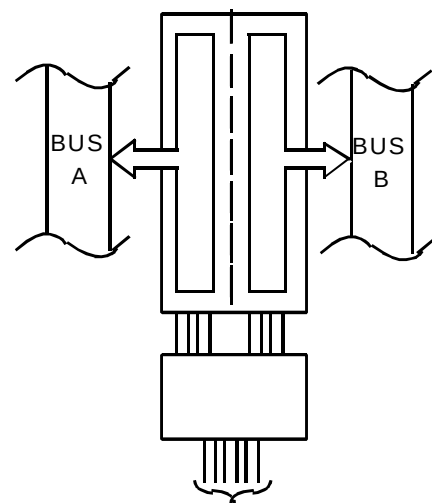
GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Real-Time Transfer Bus A to B



GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Storage From A and/or B



GAB	$\overline{\text{GBA}}$	CPAB	CPBA	SAB	SBA
H	L	H or	H or	H	H

Transfer Stored Data to A and/or B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current (3-State output pins) ⁽⁴⁾	$V_{CC} = \text{Max}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		16	48	—	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$		-16	-48	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -15\text{mA}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12\text{mA}$	—	0.3	0.5	V

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $GAB = \overline{GBA} = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.06	0.12	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $GAB = \overline{GBA} = GND$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.6	2.2	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	1.1	4.2	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $GAB = \overline{GBA} = GND$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	1.5	4 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	3.8	13 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input; ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$f_i = \text{Output Frequency}$

$N_i = \text{Number of Outputs at } f_i$

All currents are in milliamps and all frequencies are in megahertz.

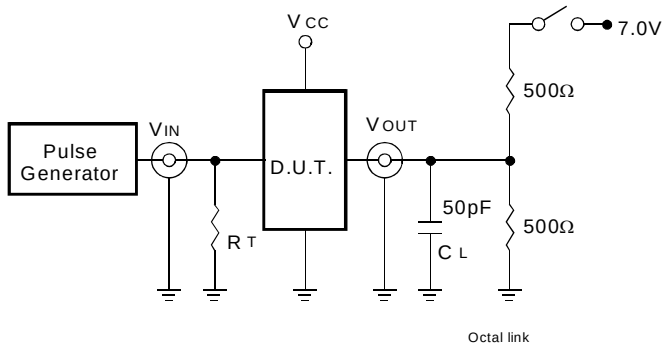
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT2652AT		FCT2652CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	C _L = 50pF R _L = 500Ω	2	6.3	1.5	5.4	ns
t _{PZH} t _{PZL}	Output Enable Time GAB, $\overline{\text{GBA}}$ to Bus		2	9.8	1.5	7.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time GAB, $\overline{\text{GBA}}$ to Bus		2	6.3	1.5	6.3	ns
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus		2	6.3	1.5	5.7	ns
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to Bus		2	7.7	1.5	6.2	ns
t _{SU}	Set-up Time, HIGH or LOW Bus to Clock		2	—	2	—	ns
t _H	Hold Time, HIGH or LOW Bus to Clock		1.5	—	1.5	—	ns
t _W	Clock Pulse Width HIGH or LOW ⁽³⁾		5	—	5	—	ns

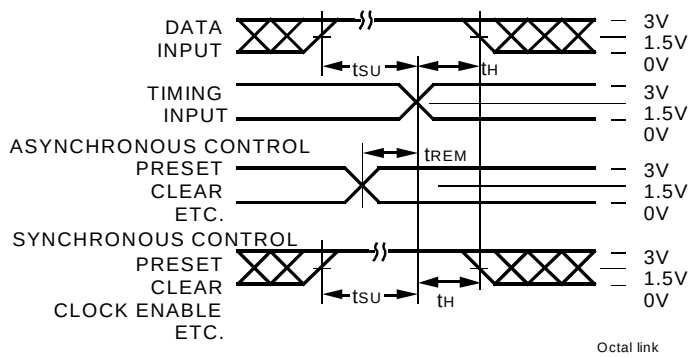
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

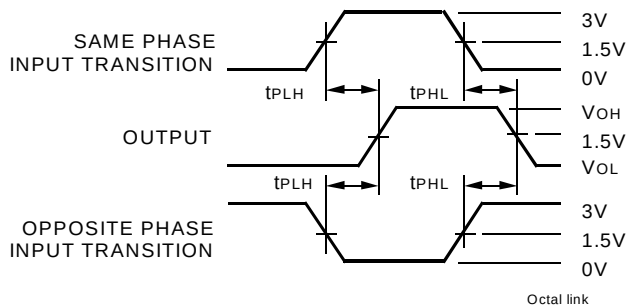
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



Propagation Delay

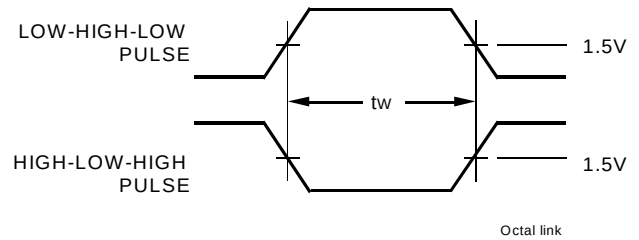
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

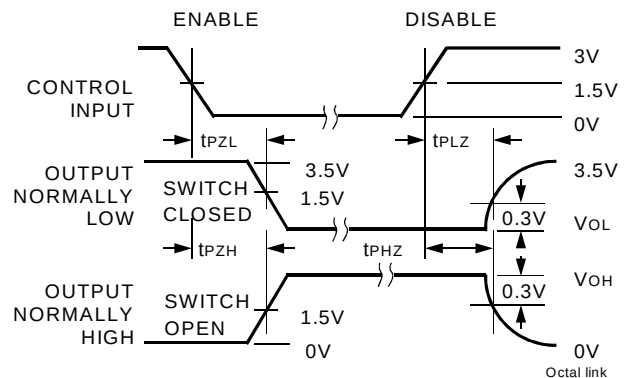
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

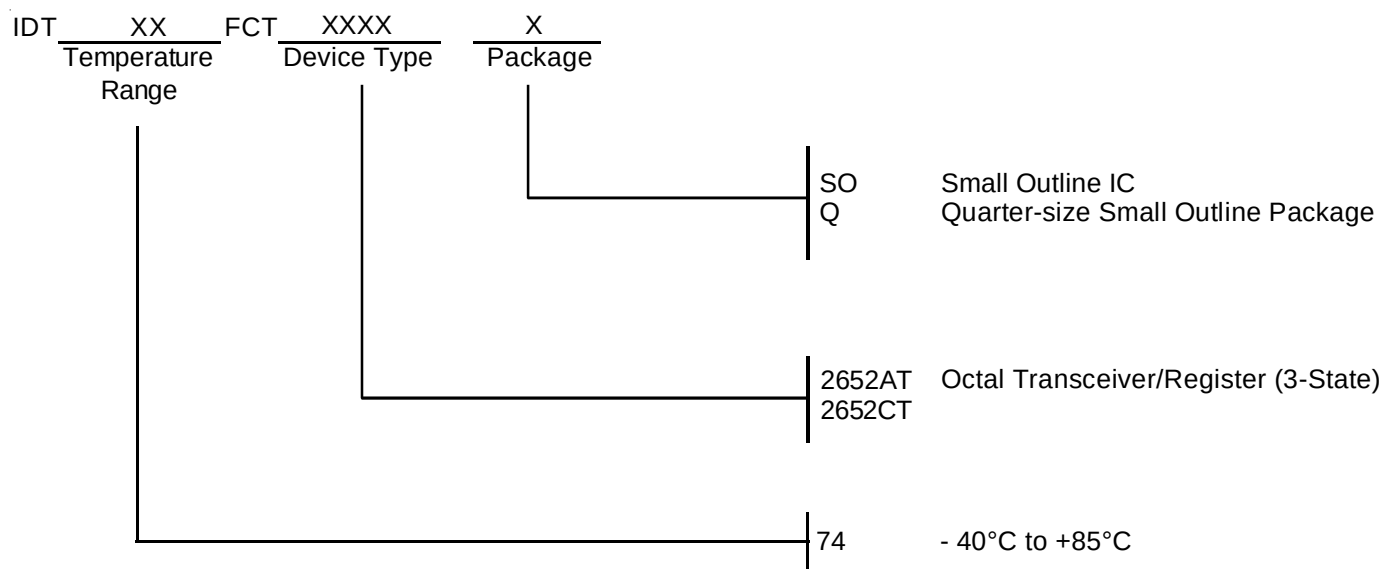


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION



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