



## FAST CMOS OCTAL LATCHED TRANSCEIVER

**IDT74FCT2543AT/CT**

### FEATURES:

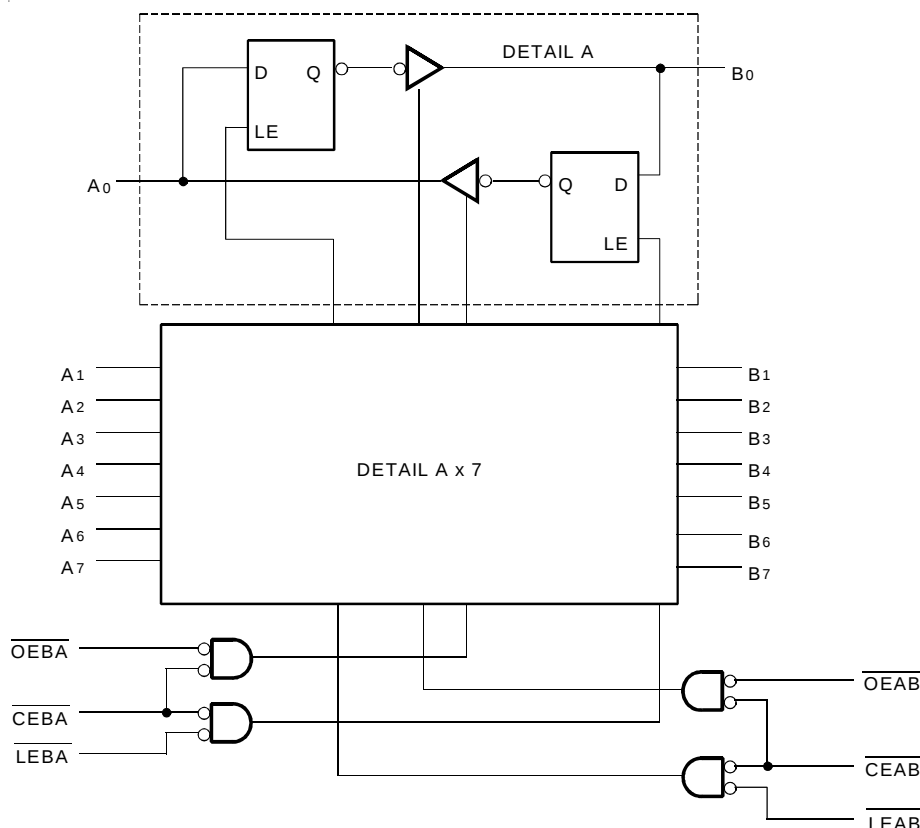
- A and C grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - $V_{OH} = 3.3V$  (typ.)
  - $V_{OL} = 0.3V$  (typ.)
- Resistor outputs (-15mA  $I_{OH}$ , 12mA  $I_{OL}$ )
- Meets or exceeds JEDEC standard 18 specifications
- Reduced system switching noise
- Available in SOIC and QSOP packages

### DESCRIPTION:

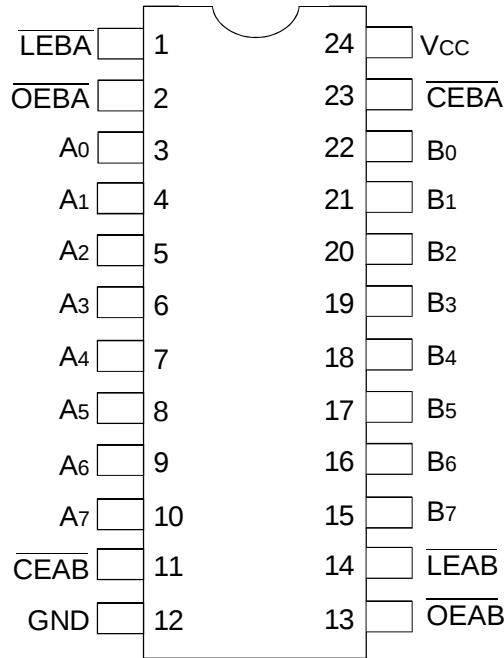
The FCT2543T is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. This device contains two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}$ ) input must be low in order to enter data from  $A_0$ – $A_7$  or to take data from  $B_0$ – $B_7$ , as indicated in the Function Table. With  $\overline{CEAB}$  low, a low signal on the A-to-B Latch Enable ( $\overline{LEAB}$ ) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both low, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  inputs.

The FCT2543T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2543T parts are plug-in replacements for FCT543T parts.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



SOIC/ QSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol               | Description                          | Max             | Unit |
|----------------------|--------------------------------------|-----------------|------|
| VTERM <sup>(2)</sup> | Terminal Voltage with Respect to GND | −0.5 to +7      | V    |
| VTERM <sup>(3)</sup> | Terminal Voltage with Respect to GND | −0.5 to Vcc+0.5 | V    |
| TSTG                 | Storage Temperature                  | −65 to +150     | °C   |
| IOUT                 | DC Output Current                    | −60 to +120     | mA   |

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Inputs and Vcc terminals only.
- Output and I/O terminals only.

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

| Symbol | Parameter <sup>(1)</sup> | Conditions | Typ. | Max. | Unit |
|--------|--------------------------|------------|------|------|------|
| CIN    | Input Capacitance        | VIN = 0V   | 6    | 10   | pF   |
| COUT   | Output Capacitance       | VOU = 0V   | 8    | 12   | pF   |

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

| Pin Names         | Description                                  |
|-------------------|----------------------------------------------|
| $\overline{OEAB}$ | A-to-B Output Enable Input (Active LOW)      |
| $\overline{OEBA}$ | B-to-A Output Enable Input (Active LOW)      |
| $\overline{CEAB}$ | A-to-B Enable Input (Active LOW)             |
| $\overline{CEBA}$ | B-to-A Enable Input (Active LOW)             |
| $\overline{LEAB}$ | A-to-B Latch Enable Input (Active LOW)       |
| $\overline{LEBA}$ | B-to-A Latch Enable Input (Active LOW)       |
| A0–A7             | A-to-B Data Inputs or B-to-A 3-State Outputs |
| B0–B7             | B-to-A Data Inputs or A-to-B 3-State Outputs |

## FUNCTION TABLE<sup>(1, 2)</sup>

For A-to-B (Symmetric with B-to-A)

| Inputs            |                   |                   | Latch Status | Output Buffers     |
|-------------------|-------------------|-------------------|--------------|--------------------|
| $\overline{CEAB}$ | $\overline{LEAB}$ | $\overline{OEAB}$ | A-to-B       | B0–B7              |
| H                 | X                 | X                 | Storing      | High Z             |
| X                 | H                 | X                 | Storing      | X                  |
| X                 | X                 | H                 | X            | High Z             |
| L                 | L                 | L                 | Transparent  | Current A Inputs   |
| L                 | H                 | L                 | Storing      | Previous* A Inputs |

### NOTES:

- \* Before  $\overline{LEAB}$  LOW-to-HIGH Transition  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care
- A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$ .

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

| Symbol    | Parameter                                                             | Test Conditions <sup>(1)</sup>                         |                     | Min. | Typ. <sup>(2)</sup> | Max.    | Unit          |
|-----------|-----------------------------------------------------------------------|--------------------------------------------------------|---------------------|------|---------------------|---------|---------------|
| $V_{IH}$  | Input HIGH Level                                                      | Guaranteed Logic HIGH Level                            |                     | 2    | —                   | —       | V             |
| $V_{IL}$  | Input LOW Level                                                       | Guaranteed Logic LOW Level                             |                     | —    | —                   | 0.8     | V             |
| $I_{IH}$  | Input HIGH Current <sup>(4)</sup>                                     | $V_{CC} = \text{Max.}$                                 | $V_I = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{IL}$  | Input LOW Current <sup>(4)</sup>                                      | $V_{CC} = \text{Max.}$                                 | $V_I = 0.5\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZH}$ | High Impedance Output Current<br>(3-State output pins) <sup>(4)</sup> | $V_{CC} = \text{Max}$                                  | $V_O = 2.7\text{V}$ | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $I_{OZL}$ |                                                                       |                                                        | $V_O = 0.5\text{V}$ | —    | —                   | $\pm 1$ |               |
| $I_I$     | Input HIGH Current <sup>(4)</sup>                                     | $V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$     |                     | —    | —                   | $\pm 1$ | $\mu\text{A}$ |
| $V_{IK}$  | Clamp Diode Voltage                                                   | $V_{CC} = \text{Min}, I_{IN} = -18\text{mA}$           |                     | —    | -0.7                | -1.2    | V             |
| $V_H$     | Input Hysteresis                                                      | —                                                      |                     | —    | 200                 | —       | mV            |
| $I_{CC}$  | Quiescent Power Supply Current                                        | $V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$ |                     | —    | 0.01                | 1       | mA            |

## OUTPUT DRIVE CHARACTERISTICS

| Symbol    | Parameter           | Test Conditions <sup>(1)</sup>                                                        |                         | Min. | Typ. <sup>(2)</sup> | Max. | Unit |
|-----------|---------------------|---------------------------------------------------------------------------------------|-------------------------|------|---------------------|------|------|
| $I_{ODL}$ | Output LOW Current  | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$ |                         | 16   | 48                  | —    | mA   |
| $I_{ODH}$ | Output HIGH Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$ |                         | -16  | -48                 | —    | mA   |
| $V_{OH}$  | Output HIGH Voltage | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$                         | $I_{OH} = -15\text{mA}$ | 2.4  | 3.3                 | —    | V    |
| $V_{OL}$  | Output LOW Voltage  | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH} \text{ or } V_{IL}$                         | $I_{OL} = 12\text{mA}$  | —    | 0.3                 | 0.5  | V    |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

| Symbol          | Parameter                                         | Test Conditions <sup>(1)</sup>                                                                                                                                                                                                                                      |                                            | Min. | Typ. <sup>(2)</sup> | Max.              | Unit       |
|-----------------|---------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------|---------------------|-------------------|------------|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC} = \text{Max.}$<br>$V_{IN} = 3.4V^{(3)}$                                                                                                                                                                                                                     |                                            | —    | 0.5                 | 2                 | mA         |
| $I_{CCD}$       | Dynamic Power Supply<br>Current <sup>(4)</sup>    | $V_{CC} = \text{Max.}$<br>$\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$<br>$\overline{CEBA} = V_{CC}$<br>One Input Toggling<br>50% Duty Cycle                                                                                                                | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 0.06                | 0.12              | mA/<br>MHz |
| $I_C$           | Total Power Supply Current <sup>(6)</sup>         | $V_{CC} = \text{Max.}$ , Outputs Open<br>$f_{CP} = 10\text{MHz}$ ( $\overline{LEAB}$ )<br>50% Duty Cycle<br>$\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$<br>$\overline{CEBA} = V_{CC}$<br>One Bit Toggling<br>at $f_i = 5\text{MHz}$<br>50% Duty Cycle      | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 0.6                 | 2.2               | mA         |
|                 |                                                   |                                                                                                                                                                                                                                                                     | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 1.1                 | 4.2               |            |
|                 |                                                   | $V_{CC} = \text{Max.}$ , Outputs Open<br>$f_{CP} = 10\text{MHz}$ ( $\overline{LEAB}$ )<br>50% Duty Cycle<br>$\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$<br>$\overline{CEBA} = V_{CC}$<br>Eight Bits Toggling<br>at $f_i = 2.5\text{MHz}$<br>50% Duty Cycle | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$ | —    | 1.5                 | 4 <sup>(5)</sup>  |            |
|                 |                                                   |                                                                                                                                                                                                                                                                     | $V_{IN} = 3.4V$<br>$V_{IN} = \text{GND}$   | —    | 3.8                 | 13 <sup>(5)</sup> |            |

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
  - Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
  - Per TTL driven input; ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
  - This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
  - Values for these conditions are examples of  $\Delta I_{CC}$  formula. These limits are guaranteed but not tested.
  - $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Output Frequency}$   
 $N_i = \text{Number of Outputs at } f_i$
- All currents are in milliamps and all frequencies are in megahertz.

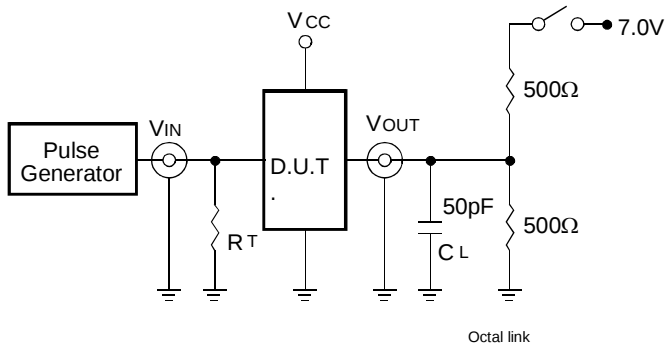
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol                               | Parameter                                                                                                                                                   | Condition <sup>(1)</sup>                       | FCT2543AT           |      | FCT2543CT           |      | Unit |
|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|---------------------|------|---------------------|------|------|
|                                      |                                                                                                                                                             |                                                | Min. <sup>(2)</sup> | Max. | Min. <sup>(2)</sup> | Max. |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>Transparent Mode<br>Ax to Bx or Bx to Ax                                                                                               | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 1.5                 | 6.5  | 1.5                 | 5.3  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>$\overline{\text{LEBA}}$ to Ax, $\overline{\text{LEAB}}$ to Bx                                                                         |                                                | 1.5                 | 8    | 1.5                 | 7    | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time<br>$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to Ax or Bx<br>$\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to Ax or Bx  |                                                | 1.5                 | 9    | 1.5                 | 8    | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time<br>$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to Ax or Bx<br>$\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to Ax or Bx |                                                | 1.5                 | 7.5  | 1.5                 | 6.5  | ns   |
| t <sub>SU</sub>                      | Set-up Time, HIGH or LOW<br>Ax or Bx to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$                                                                |                                                | 2                   | —    | 2                   | —    | ns   |
| t <sub>H</sub>                       | Hold Time, HIGH or LOW<br>Ax or Bx to $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$                                                                  |                                                | 2                   | —    | 2                   | —    | ns   |
| t <sub>H</sub>                       | $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$ Pulse Width LOW                                                                                        |                                                | 5                   | —    | 5                   | —    | ns   |

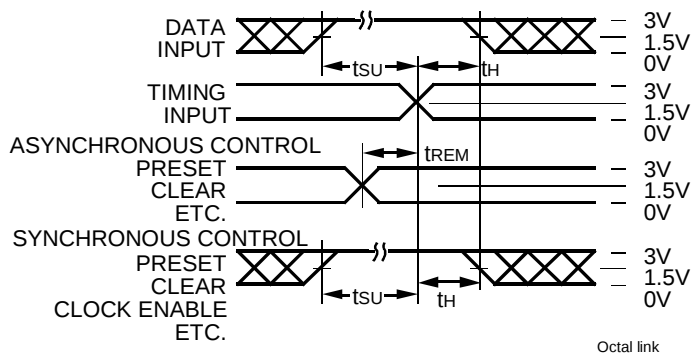
### NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

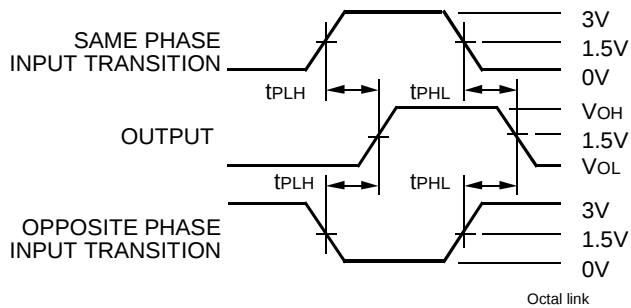
## TEST CIRCUITS AND WAVEFORMS



**Test Circuits for All Outputs**



**Set-Up, Hold, and Release Times**



**Propagation Delay**

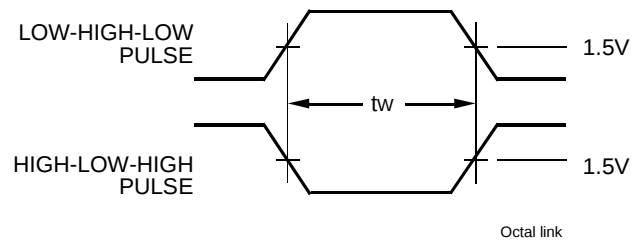
## SWITCH POSITION

| Test                                    | Switch |
|-----------------------------------------|--------|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests                         | Open   |

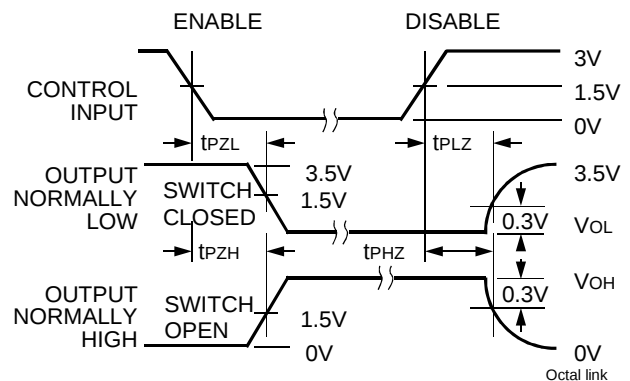
### DEFINITIONS:

$C_L$  = Load capacitance: includes jig and probe capacitance.

$R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.



**Pulse Width**



**Enable and Disable Times**

### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

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graph LR
    Root[2543AT74] --- Temp[Temperature Range]
    Root --- Device[Device Type]
    Root --- Package[Package]
    Temp --- TempVal[74]
    TempVal --- TempDesc["- 40° to +85°C"]
    Device --- DeviceVal[2543AT  
2543CT]
    DeviceVal --- DeviceDesc[Octal Latched Transceiver]
    Package --- PackageVal[SO  
Q]
    PackageVal --- PackageDesc[Small Outline IC  
Quarter-size Small Outline Package]
  
```

2543AT74

Temperature Range

74

- 40° to +85°C

Device Type

2543AT  
2543CT

Octal Latched Transceiver

Package

SO  
Q

Small Outline IC  
Quarter-size Small Outline Package

