FAST CMOS
20-BIT
TRANSPARENT LATCH

IDT74FCT16841AT/CT

FEATURES:

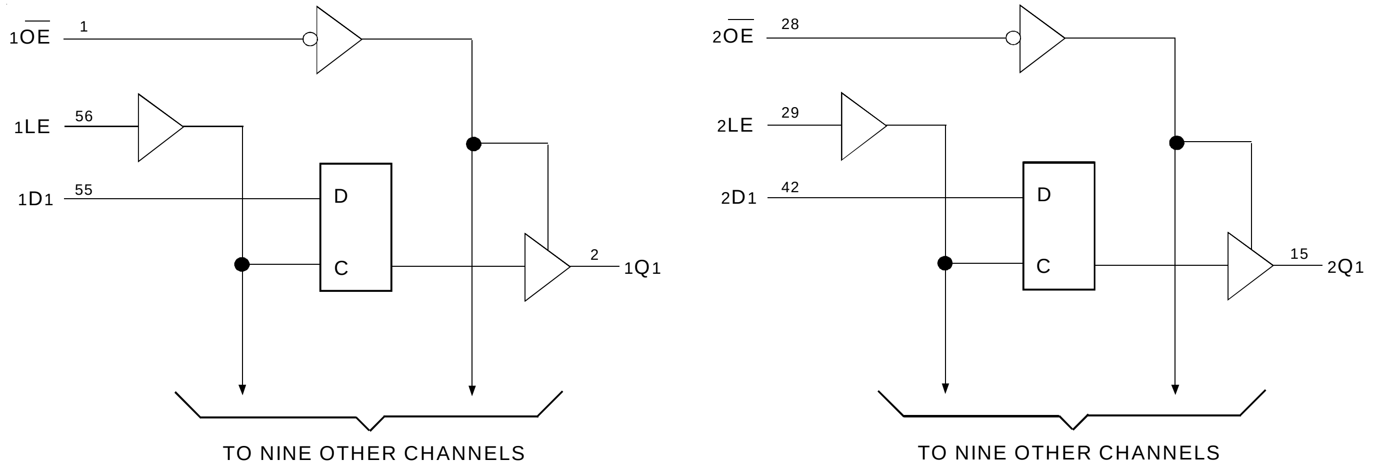
- **0.5 MICRON CMOS Technology**
- **High-speed, low-power CMOS replacement for ABT functions**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤1µA (max.)**
- **V_{CC} = 5V ±10%**
- **High drive outputs (–32mA I_{OH}, 64mA I_{OL})**
- **Power off disable outputs permit “live insertion”**
- **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **Available in SSOP and TSSOP packages**

DESCRIPTION:

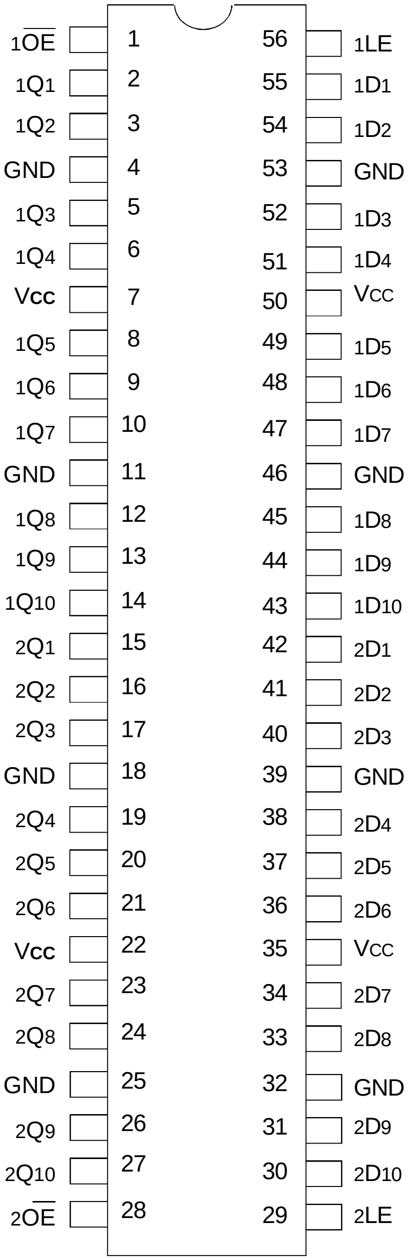
The FCT16841T 20-bit transparent D-type latch is built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary data storage. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable ($\overline{OE}$) and Latch Enable (LE) controls are organized to operate each device as two 10-bit latches or one 20-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16841T is ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX Output and I/O terminals.
3. Outputs and I/O terminals for FCT162XXX.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Inputs (Active HIGH)
x$\overline{\text{OE}}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

FUNCTION TABLE(1)

Inputs			Outputs
xDx	xLE	x$\overline{\text{OE}}$	xQx
H	H	L	H
L	H	L	L
X	L	L	Q(2)
X	X	H	Z

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
2. Output Level before xLE HIGH-to-LOW transition.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max V_{IN} = GND or V_{CC}		—	5	500	µA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V(3)		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.5	3.5	—	V
			I_{OH} = –15mA	2.4	3.5	—	V
			I_{OH} = –32mA(4)	2	3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = 64mA	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. This test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open x$\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current(6)	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle x$\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3	5.5(5)	
		50% Duty Cycle x$\overline{OE}$ = GND xLE = V_{CC} Twenty Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8	20.5(5)	

NOTES:

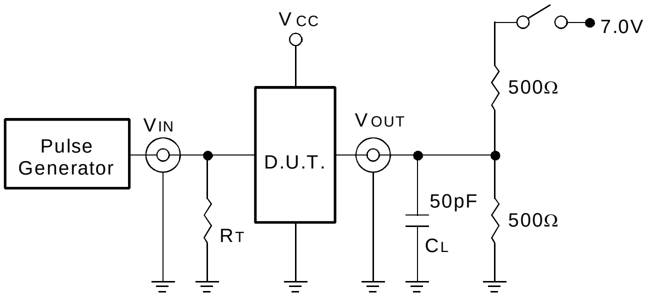
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}\ (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			74FCT16841AT		74FCT16841CT		
Symbol	**Parameter**	**Condition[1]**	**Min.[2]**	**Max.**	**Min.[2]**	**Max.**	**Unit**
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	9	1.5	3.8	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	13	1.5	7.5	
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	C_L = 50pF R_L = 500Ω	1.5	12	1.5	3.8	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	16	1.5	7.5	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	4.6	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	23	1.5	9	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	C_L = 5pF[3] R_L = 500Ω	1.5	7	1.5	3.6	ns
		C_L = 50pF R_L = 500Ω	1.5	8	1.5	3.6	
t_{SU}	Set-Up Time HIGH or LOW, xDx to xLE	C_L = 50pF R_L = 500Ω	2.5	—	1	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	1	—	ns
t_W	xLE Pulse Width HIGH		4[5]	—	3[5]	—	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This condition is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
5. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

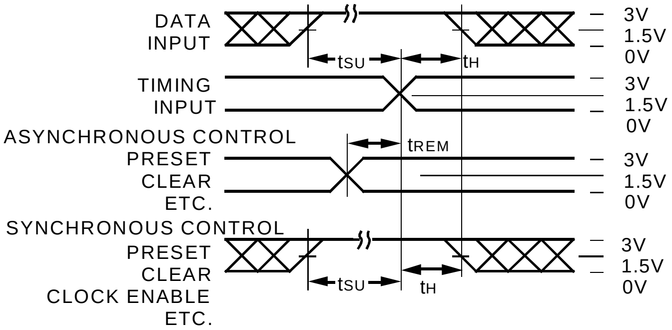


Test Circuits for All Outputs

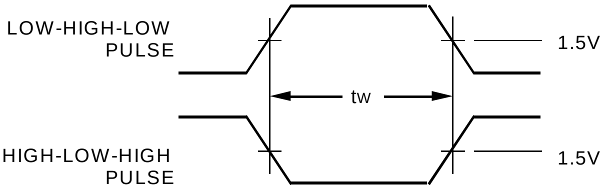
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

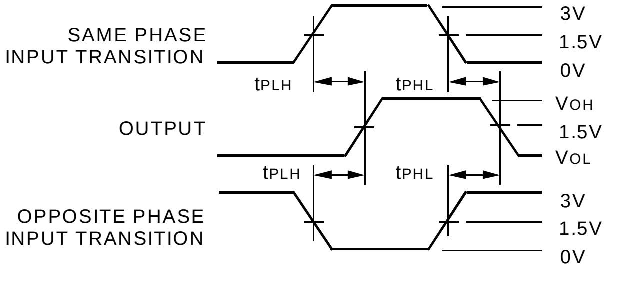
DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



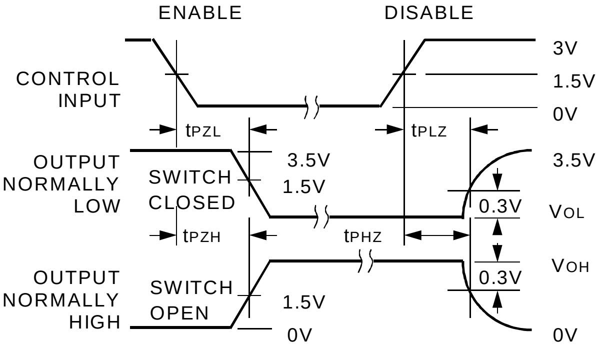
Set-up, Hold, and Release Times



Pulse Width



Propagation Delay



Enable and Disable Times

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION

IDT XX FCT XXX XXXX XX

XX	Temp. Range	74	– 40°C to +85°C
XXX	Family	16	Double-Density, 5 Volt, High Drive
XXXX	Device Type	841AT 841CT	20-Bit Transparent Latch
XX	Package	PV PA	Shrink Small Outline Package Thin Shrink Small Outline Package

DATA SHEET DOCUMENT HISTORY

6/24/2002 Updated as per PDNs Logic-00-07 and Logic-01-04

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