



2.5V TO 3.3V HIGH PERFORMANCE CLOCK BUFFER

IDT5V2305

FEATURES:

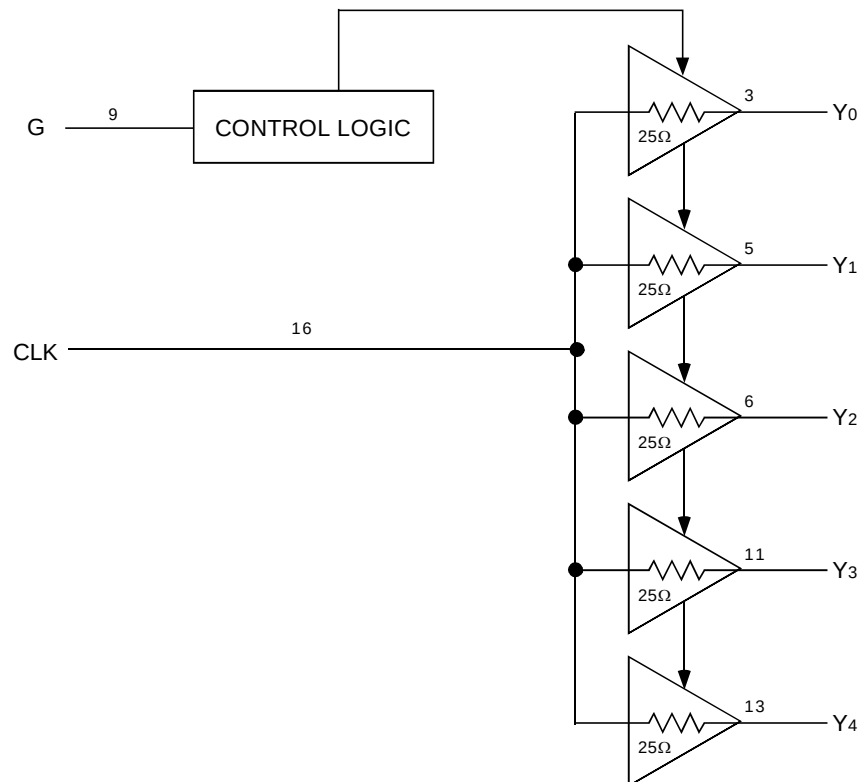
- High performance 1:5 clock driver for general purpose applications
- Operates up to 170MHz at $V_{DD} = 2.5V$
- Operates up to 200MHz at $V_{DD} = 3.3V$
- Pin-to-pin skew < 50ps
- V_{DD} range: 2.3V to 3.6V
- Output enable glitch suppression
- 25 Ω on-chip series dampening resistors
- Available in TSSOP and VFQFPN packages

DESCRIPTION:

The IDT5V2305 is a high performance, low skew clock buffer that operates up to 200MHz. One bank of five outputs provides low skew copies of CLK. Through the use of control pin G, the outputs of bank Y(0:4) can be placed in a low state regardless of CLK input. The device operates in 2.5V and 3.3V environments. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The IDT5V2305 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

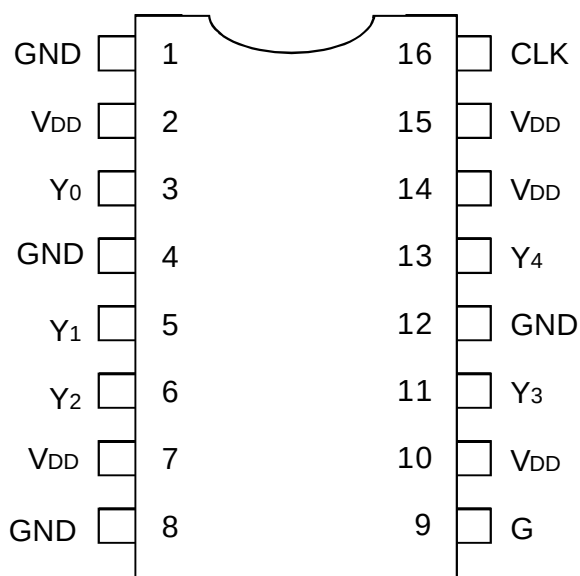


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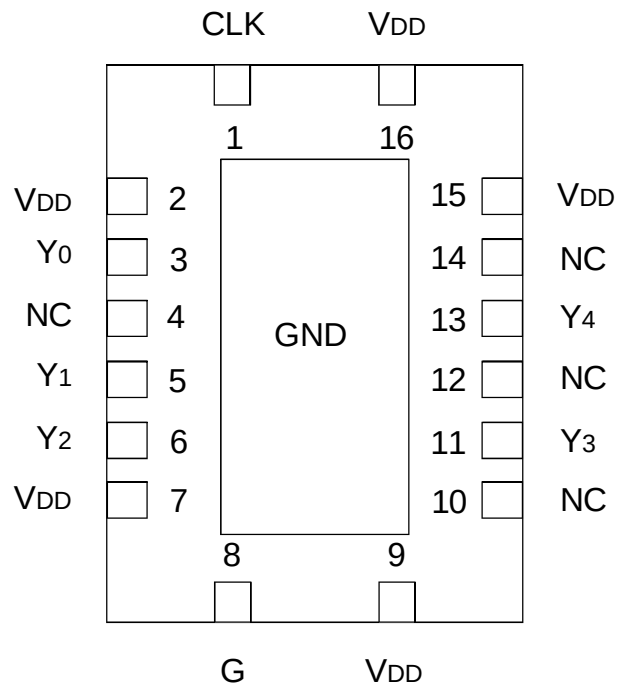
INDUSTRIAL TEMPERATURE RANGE

SEPTEMBER 2003

PIN CONFIGURATION



**TSSOP
TOP VIEW**



**VFQFPN
TOP VIEW**

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{DD}	Power Supply Voltage	−0.5 to +4.6	V
V _I	Input Voltage ⁽²⁾	−0.5 to V _{DD} +0.5	V
V _O	Output Voltage ⁽²⁾	−0.5 to V _{DD} +0.5	V
I _{IK}	Input Clamp Current V _I < 0 or V _I > V _{DD}	±50	mA
I _{OK}	Output Clamp Current V _O < 0 or V _O > V _{DD}	±50	mA
I _O	Continuous Total Output Current V _O < 0 to V _{DD}	±50	mA
T _{STG}	Storage Temperature	−65 to +150	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Not to exceed 4.6V.

CAPACITANCE⁽¹⁾ (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Min.	Typ.	Max.	Unit
C _{IN}	Input Capacitance V _I = 0V or V _{DD}	—	2.5	—	pF

FUNCTION TABLE⁽¹⁾

Inputs		Output
G	CLK	Y(0:4)
L	X	L
H	H	H

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

PIN DESCRIPTION

TERMINAL		Description
Symbol	I/O	
G	I	Output Enable Control for Y(0:4) Outputs. This output enable is active HIGH. If this pin is Logic HIGH, the Y(0:4) clock outputs will follow the input clock (CLK). If this pin is logic LOW, the Y(0:4) outputs will drive low independent of the state of CLK.
Y(0:4)	O	Buffered Output Clocks
CLK	I	Input Reference Frequency
GND		Ground
V _{DD}	PWR	DC Power Supply, 2.3V to 3.6V

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DD}	Internal Power Supply Voltage	2.3	2.5		V
			3.3	3.6	
V _{IL}	Input Voltage LOW	V _{DD} = 3V to 3.6V		0.8	V
		V _{DD} = 2.3V to 2.7V		0.7	
V _{IH}	Input Voltage HIGH	V _{DD} = 3V to 3.6V			V
		V _{DD} = 2.3V to 2.7V			
V _I	Input Voltage	0		V _{DD}	V
I _{OH}	Output Current HIGH	V _{DD} = 3V to 3.6V		-12	mA
		V _{DD} = 2.3V to 2.7V		-6	
I _{OL}	Output Current LOW	V _{DD} = 3V to 3.6V		12	mA
		V _{DD} = 2.3V to 2.7V		6	
T _A	Ambient Operating Temperature	-40		+85	°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V _{IK}	Input Voltage	V _{DD} = 3V, I _{IN} = -18mA			-1.2	V
I _{IN}	Input Current	V _I = 0V or V _{DD}			±5	μA
I _{DD}	Static Device Current ⁽¹⁾	CLK = 0V or V _{DD} , I _O = 0mA, V _{DD} = 3.3V			25	μA

NOTE:

1. For I_{DD} over frequency, see TEST CIRCUIT AND WAVEFORMS.

DC ELECTRICAL CHARACTERISTICS - V_{DD} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max	Unit
V _{OH}	HIGH level Output Voltage	V _{DD} = Min. to Max.	I _{OH} = -100μA	V _{DD} - 0.2			V
		V _{DD} = 3V	I _{OH} = -12mA	2.1			
			I _{OH} = -6mA	2.4			
V _{OL}	LOW level Output Voltage	V _{DD} = Min. to Max.	I _{OH} = 100μA			0.2	V
		V _{DD} = 3V	I _{OH} = 12mA			0.8	
			I _{OH} = 6mA			0.55	
I _{OH}	HIGH level Output Current	V _{DD} = 3V	V _O = 1V	-28			mA
		V _{DD} = 3.3V	V _O = 1.65V		-36		
		V _{DD} = 3.6V	V _O = 3.135V			-14	
I _{OL}	LOW level Output Current	V _{DD} = 3V	V _O = 1.95V	28			mA
		V _{DD} = 3.3V	V _O = 1.65V		36		
		V _{DD} = 3.6V	V _O = 0.4V			14	

NOTE:

1. All typical values are at respective nominal V_{DD}.

DC ELECTRICAL CHARACTERISTICS - $V_{DD} = 2.5V \pm 0.2V$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max	Unit
V _{OH}	HIGH level Output Voltage	V _{DD} = Min. to Max.	I _{OH} = -100μA	V _{DD} - 0.2			V
		V _{DD} = 2.3V	I _{OH} = -6mA	1.8			
V _{OL}	LOW level Output Voltage	V _{DD} = Min. to Max.	I _{OH} = 100μA			0.2	V
		V _{DD} = 2.3V	I _{OH} = 6mA			0.55	
I _{OH}	HIGH level Output Current	V _{DD} = 2.3V	V _O = 1V	-17			mA
		V _{DD} = 2.5V	V _O = 1.25V		-25		
		V _{DD} = 2.7V	V _O = 2.375V			-10	
I _{OL}	LOW level Output Current	V _{DD} = 2.3V	V _O = 1.2V	17			mA
		V _{DD} = 2.5V	V _O = 1.25V		25		
		V _{DD} = 2.7V	V _O = 0.3V			10	

NOTE:

1. All typical values are at respective nominal V_{DD}.

TIMING REQUIREMENTS OVER RECOMMENDED RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
f _{CLK}	Clock Frequency	V _{DD} = 3V to 3.6V	0		200	MHz
		V _{DD} = 2.3V to 2.7V	0		170	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE -

$$V_{DD} = 3.3V \pm 0.3V^{(1)}$$

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max	Unit
t _{PLH} t _{PHL}	CLK to Yx	f = 0MHz to 200MHz, C _L = 25pF	1.3		2.6	ns
tsk(o) ⁽²⁾	Output Skew, Yx to Yx				50	ps
tsk(p)	Pulse Skew				300	ps
tsk(pp)	Part-to-Part Skew				500	ps
t _R	Rise Time	V _O = 0.4V to 2V	0.7		2	V/ns
t _F	Fall Time	V _O = 2V to 0.4V	0.7		2	V/ns
tsu	G before CLK↓	V _(THRESHOLD) = V _{DD} /2	0.1			ns
t _H	G after CLK↓		0.4			

NOTES:

1. All typical values are at respective nominal V_{DD}.
2. This specification is only valid for equal loading of all outputs.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE -

$$V_{DD} = 2.5V \pm 0.2V^{(1)}$$

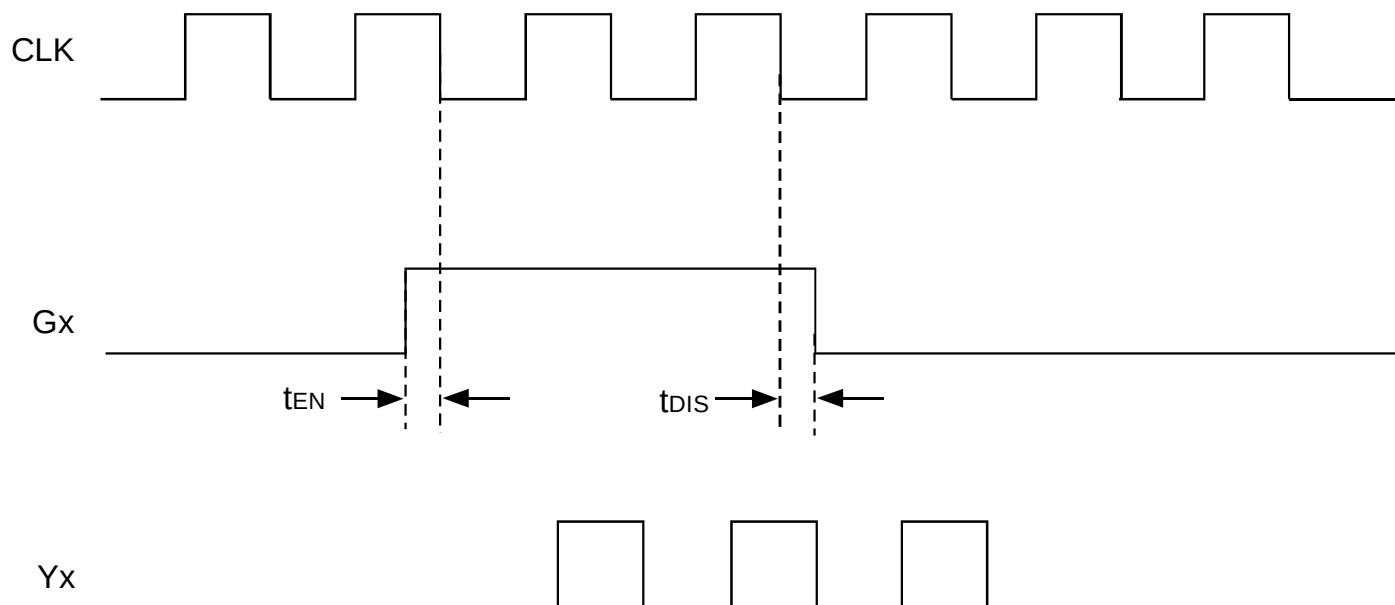
Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max	Unit
t _{PLH} t _{PHL}	CLK to Yx	f = 0MHz to 170MHz, C _L = 25pF	1.5		3.5	ns
tsk(o) ⁽²⁾	Output Skew, Yx to Yx				75	ps
tsk(p)	Pulse Skew				700	ps
tsk(pp)	Part-to-Part Skew				600	ps
t _R	Rise Time	V _O = 0.4V to 1.7V	0.4		1.4	V/ns
t _F	Fall Time	V _O = 1.7V to 0.4V	0.4		1.4	V/ns
tsu	G before CLK↓	V _(THRESHOLD) = V _{DD} /2	0.1			ns
t _H	G after CLK↓		0.4			

NOTES:

1. All typical values are at respective nominal V_{DD}.
2. This specification is only valid for equal loading of all outputs.

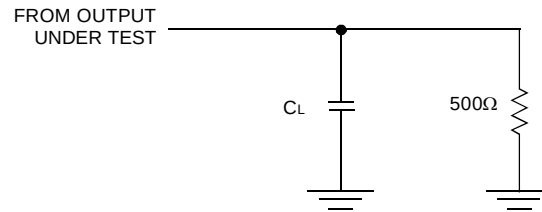
OUTPUT ENABLE GLITCH SUPPRESSION CIRCUIT

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer will be enabled on the next full period of the input clock (negative edge triggered by the input clock). The G input must be stable one t_{EN} - time prior to the falling edge of the CLK for predictable operation.



G (t_{EN} , t_{DIS}) Relative to CLK↓

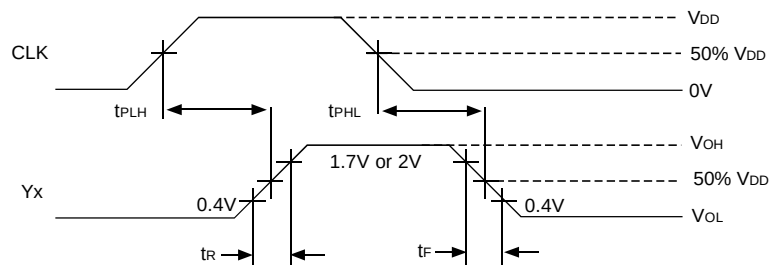
TEST CIRCUITS AND WAVEFORMS



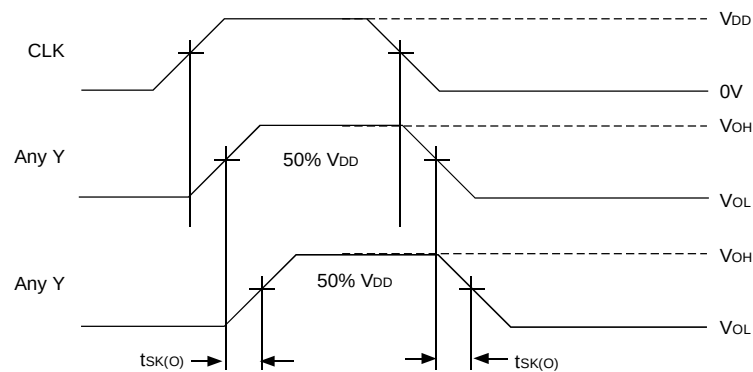
NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 200\text{MHz}$; $Z_o = 50\Omega$; $t_R < 1.2\text{ns}$; $t_F < 1.2\text{ns}$.

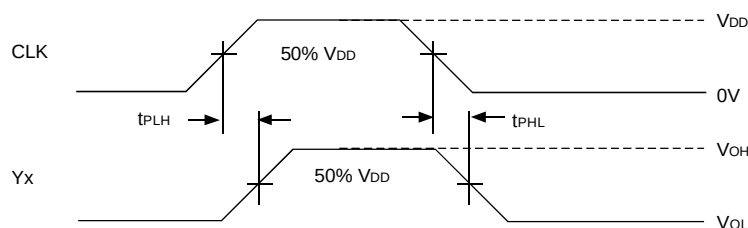
Test Load Circuit



Voltage Waveforms Propagation Delay Times



Output Skew



$$t_{SK(P)} = |t_{PLH} - t_{PHL}|$$

Pulse Skew

ORDERING INFORMATION

IDT	XXXXX	XX	X		
Device Type	Package	Package			
			I		-40°C to +85°C (Industrial)
			PG NR		Thin Shrink Small Outline Package Thermally Enhanced Plastic Very Fine Pitch Quad Flat No Lead Package
			5V2305		2.5V to 3.3V High Performance Clock Buffer



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