# 18Mb Pipelined QDR™II SRAM Burst of 2

*Advance Information*
*IDT71P72204*
*IDT71P72104*
*IDT71P72804*
*IDT71P72604*

## Features

- 18Mb Density (2Mx8, 2Mx9, 1Mx18, 512kx36)
- Separate, Independent Read and Write Data Ports
  - Supports concurrent transactions
- Dual Echo Clock Output
- 2-Word Burst on all SRAM accesses
- DDR (Double Data Rate) Multiplexed Address Bus
  - One Read and One Write request per clock cycle
- DDR (Double Data Rate) Data Buses
  - Two word burst data per clock on each port
  - Four word transfers per clock cycle (2 word bursts on 2 ports)
- Depth expansion through Control Logic
- HSTL (1.5V) inputs that can be scaled to receive signals from 1.4V to 1.9V.
- Scalable output drivers
  - Can drive HSTL, 1.8V TTL or any voltage level from 1.4V to 1.9V.
  - Output Impedance adjustable from 35 ohms to 70 ohms
- 1.8V Core Voltage (VDD)
- 165-ball, 1.0mm pitch, 15mm x 17mm fBGA Package
- JTAG Interface

## Description

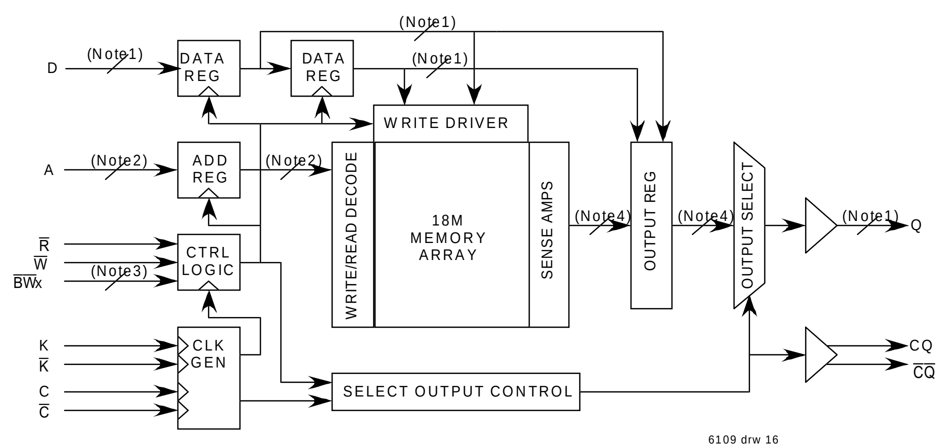
The IDT QDRII™ Burst of two SRAMs are high-speed synchronous memories with independent, double-data-rate (DDR), read and write data ports. This scheme allows simultaneous read and write access for the maximum device throughput, with two data items passed with each read or write. Four data word transfers occur per clock cycle, providing quad-data-rate (QDR) performance. Comparing this with standard SRAM common I/O (CIO), single data rate (SDR) devices, a four to one increase in data access is achieved at equivalent clock speeds. Considering that QDRII allows clock speeds in excess of standard SRAM devices, the throughput can be increased well beyond four to one in most applications.

Using independent ports for read and write data access, simplifies system design by eliminating the need for bi-directional buses. All buses associated with the QDRII are unidirectional and can be optimized for signal integrity at very high bus speeds. The QDRII has scalable output impedance on its data output bus and echo clocks, allowing the user to tune the bus for low noise and high performance.

The QDRII has a single DDR address bus with multiplexed read and write addresses. All read addresses are received on the first half of the clock cycle and all write addresses are received on the second half of the clock cycle. The read and write enables are received on the first half of the clock cycle. The byte and nibble write signals are received on both halves of the clock cycle simultaneously with the data they are controlling on the data input bus.

The QDRII has echo clocks, which provide the user with a clock

## Functional Block Diagram




Notes
1) Represents 8 data signal lines for x8, 9 signal lines for x9, 18 signal lines for x18, and 36 signal lines for x36
2) Represents 20 address signal lines for x8 and x9, 19 address signal lines for x18, and 18 address signal lines for x36.
3) Represents 1 signal line for x9, 2 signal lines for x18, and four signal lines for x36. On x8 parts, the BW is a "nibble write" and there are 2 signal lines.
4) Represents 16 data signal lines for x8, 18 signal lines for x9, 36 signal lines for x18, and 72 signal lines for x36.

**AUGUST 2003**

that is precisely timed to the data output, and tuned with matching impedance and signal quality. The user can use the echo clock for downstream clocking of the data. Echo clocks eliminate the need for the user to produce alternate clocks with precise timing, positioning, and signal qualities to guarantee data capture. Since the echo clocks are generated by the same source that drives the data output, the relationship to the data is not significantly affected by voltage, temperature and process, as would be the case if the clock were generated by an outside source.

All interfaces of the QDRII SRAM are HSTL, allowing speeds beyond SRAM devices that use any form of TTL interface. The interface can be scaled to higher voltages (up to 1.9V) to interface with 1.8V systems if necessary. The device has a $V_{DDQ}$ and a separate Vref, allowing the user to designate the interface operational voltage, independent of the device core voltage of 1.8V $V_{DD}$. The output impedance control allows the user to adjust the drive strength to adapt to a wide range of loads and transmission lines.

The device is capable of sustaining full bandwidth on both the input and output ports simultaneously. All data is in two word bursts, with addressing capability to the burst level.

## Clocking

The QDRII SRAM has two sets of input clocks, namely the K, $\overline{K}$ clocks and the C, $\overline{C}$ clocks. In addition, the QDRII has an output "echo" clock, CQ, $\overline{CQ}$.

The K and $\overline{K}$ clocks are the primary device input clocks. The K clock is, used to clock in the control signals ($\overline{R}$, $\overline{W}$ and $\overline{BW}$x or $\overline{NW}$x), the read address, and the first word of the data burst during a write operation. The $\overline{K}$ clock is used to clock in the control signals ($\overline{BW}$x or $\overline{NW}$x), write address and the second word of the data burst during a write operation. The K and $\overline{K}$ clocks are also used internally by the SRAM. In the event that the user disables the C and $\overline{C}$ clocks, the K and $\overline{K}$ clocks will also be used to clock the data out of the output register and generate the echo clocks.

The C and $\overline{C}$ clocks may be used to clock the data out of the output register during read operations and to generate the echo clocks. C and $\overline{C}$ must be presented to the SRAM within the timing tolerances. The output data from the QDRII will be closely aligned to the C and $\overline{C}$ input, through the use of an internal DLL. When C is presented to the QDRII SRAM, the DLL will have already internally clocked the data to arrive at the device output simultaneously with the arrival of the C clock. The $\overline{C}$ and second data item of the burst will also correspond.

## Single Clock Mode

The QDRII SRAM may be operated with a single clock pair. C and $\overline{C}$ may be disabled by tying both signals high, forcing the outputs and echo clocks to be controlled instead by the K and $\overline{K}$ clocks.

## DLL Operation

The DLL in the output structure of the QDRII SRAM can be used to closely align the incoming clocks C and $\overline{C}$ with the output of the data, generating very tight tolerances between the two. The user may disable the DLL by holding $\overline{Doff}$ low. With the DLL off, the C and $\overline{C}$ (or K and $\overline{K}$ if C and $\overline{C}$ are not used) will directly clock the output register of the SRAM. With the DLL off, there will be a propagation delay from the time the clock enters the device until the data appears at the output.

## Echo Clock

The echo clocks, CQ and $\overline{CQ}$, are generated by the C and $\overline{C}$ clocks (or K, $\overline{K}$ if C, $\overline{C}$ are disabled). The rising edge of C generates the rising edge of CQ, and the falling edge of $\overline{CQ}$. The rising edge of $\overline{C}$ generates the rising edge of $\overline{CQ}$ and the falling edge of CQ. This scheme improves the correlation of the rising and falling edges of the echo clock and will improve the duty cycle of the individual signals.

The echo clock is very closely aligned with the data, guaranteeing that the echo clock will remain closely correlated with the data, within the tolerances designated.

## Read and Write Operations

QDRII devices internally store the two words of the burst as a single, wide word and will retain their order in the burst. There is no ability to address to the single word level or reverse the burst order; however, the byte and nibble write signals can be used to prevent writing any individual bytes, or combined to prevent writing one word of the burst.

Read operations are initiated by holding the read port select ($\overline{R}$) low, and presenting the read address to the address port during the rising edge of K which will latch the address. The data will then be read and will appear at the device output at the designated time in correspondence with the C and $\overline{C}$ clocks.

Write operations are initiated by holding the write port select ($\overline{W}$) low and designating with the Byte Write inputs ($\overline{BW}$x) which bytes are to be written (or $\overline{NW}$x on x8 devices). The first word of the data must also be present on the data input bus D[X:0]. Upon the rising edge of K the first word of the burst will be latched into the input register. After K has risen, and the designated hold times observed, the second half of the clock cycle is initiated by presenting the write address to the address bus A[X:0], the $\overline{BW}$x (or $\overline{NW}$x) inputs for the second data word of the burst, and the second data item of the burst to the data bus D[X:0]. Upon the rising edge of $\overline{K}$, the second word of the burst will be latched, along with the designated address. Both the first and second words of the burst will then be written into memory as designated by the address and byte write enables.

## Output Enables

The QDRII SRAM automatically enables and disables the Q[X:0] outputs. When a valid read is in progress, and data is present at the output, the output will be enabled. If no valid data is present at the output (read not active), the output will be disabled (high impedance). The echo clocks will remain valid at all times and cannot be disabled or turned off. During power-up the Q outputs will come up in a high impedance state.

## Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and Vss to allow the SRAM to adjust its output drive impedance. The value of RQ must be 5X the value of the intended drive impedance of the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of +/- 10% is between 175 ohms and 350 ohms, with $V_{DDQ}$ = 1.5V. The output impedance is adjusted every 1024 clock cycles to correct for drifts in supply voltage and temperature. If the user wishes to drive the output impedance of the SRAM to it's lowest value, the ZQ pin may be tied to $V_{DDQ}$.

# Pin Definitions

| Symbol | Pin Function | Description |
|---|---|---|
| D[X:0] | Input Synchronous | Data input signals, sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations<br>2M x 8 -- D[7:0]<br>2M x 9 -- D[8:0]<br>1M x 18 -- D[17:0]<br>512K x 36 -- D[35:0] |
| $\overline{BW_0}$, $\overline{BW_1}$<br>$\overline{BW_2}$, $\overline{BW_3}$ | Input Synchronous | Byte Write Select 0, 1, 2, and 3 are active LOW. Sampled on the rising edge of the K and again on the rising edge of $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. All the byte writes are sampled on the same edge as the data. Deselecting a Byte Write Select will cause the corresponding byte of data to be ignored and not written in to the device.<br>2M x 9 -- $\overline{BW_0}$ controls D[8:0]<br>1M x 18 -- $\overline{BW_0}$ controls D[8:0] and $\overline{BW_1}$ controls D[17:9]<br>512K x 36 -- $\overline{BW_0}$ controls D[8:0], $\overline{BW_1}$ controls D[17:9], $\overline{BW_2}$ controls D[26:18] and $\overline{BW_3}$ controls D[35:27] |
| $\overline{NW0}$ $\overline{NW1}$ | Input Synchronous | Nibble Write Select 0 and 1 are active LOW. Available only on x8 bit parts instead of Byte Write Selects. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which nibble is written into the device during the current portion of the write operations. Nibbles not written remain unaltered. All the nibble writes are sampled on the same edge as the data. Deselecting a Nibble Write Select will cause the corresponding nibble of data to be ignored and not written in to the device. |
| A | Input Synchronous | Address Inputs. Read addresses are sampled on the rising edge of K clock during active read operations. Write addresses are sampled on the rising edge of $\overline{K}$ clock during active write operations. These address inputs are multiplxed, so that both a read and write operation can occur on the same clock cycle. These inputs are ignored when the appropriate port is deselected. |
| Q[X:0] | Output Synchronous | Data Output signals. These pins drive out the requested data during a Read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during Read operations or K and $\overline{K}$ when operating in single clock mode. When the Read port is deselected, Q[X:0] are automatically three-stated. |
| $\overline{W}$ | Input Synchronous | Write Control Logic active Low. Sampled on the rising edge of the positive input clock (K). When asserted active, a write operation in initiated. Deasserting will deselect the Write port. Deselecting the Write port will cause D[X:0] to be ignored. |
| $\overline{R}$ | Input Synchronous | Read Control Logic, active LOW. Sampled on the rising edge of Positive Input Clock (K). When active, a Read operation is initiated. Deasserting will cause the Read port to be deselected. When deselected, the pending access is allowed to complete and the output drivers are automatically three-stated following the next rising edge of the C clock. Each read access consists of a burst of two sequential transfer. |
| C | Input Clock | Positive Output Clock Input. C is used in conjunction with $\overline{C}$ to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details. |
| $\overline{C}$ | Input Clock | Negative Output Clock Input. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details. |
| K | Input Clock | Positive Input Clock Input. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through Q[X:0] when in single clock mode. All accesses are initiated on the rising edge of K. |
| $\overline{K}$ | Input Clock | Negative Input Clock Input. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through Q[X:0] when in single clock mode. |
| CQ, $\overline{CQ}$ | Output Clock | Synchronous Echo clock outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals are free running and do not stop when the output data is tri-stated. |
| ZQ | Input | Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. Q[X:0] output impedance is set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to $V_{DDQ}$, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected. |

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# Pin Definitions continued

| Symbol | Pin Function | Description |
|---|---|---|
| $\overline{\text{Doff}}$ | Input | DLL Turn Off. When low this input will turn off the DLL inside the device. The AC timings with the DLL turned off will be different from those listed in this data sheet. There will be an increased propagation delay from the incidence of C and $\overline{C}$ to Q, or K and $\overline{K}$ to Q as configured. The propagation delay is not a tested parameter, but will be similar to the propagation delay of other SRAM devices in this speed grade. |
| TDO | Output | TDO pin for JTAG |
| TCK | Input | TCK pin for JTAG. |
| TDI | Input | TDI pin for JTAG. An internal resistor will pull TDI to $V_{DD}$ when the pin is unconnected. |
| TMS | Input | TMS pin for JTAG. An internal resistor will pull TMS to $V_{DD}$ when the pin is unconnected. |
| NC | | No connects inside the package. Can be tied to any voltage level |
| $V_{REF}$ | Input Reference | Reference Voltage input. Static input used to set the reference level for HSTL inputs and Outputs as well as AC measurement points. |
| $V_{DD}$ | Power Supply | Power supply inputs to the core of the device. Should be connected to a 1.8V power supply. |
| $V_{SS}$ | Ground | Ground for the device. Should be connected to ground of the system. |
| $V_{DDQ}$ | Power Supply | Power supply for the outputs of the device. Should be connected to a 1.5V power supply for HSTL or scaled to the desired output voltage. |

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# Pin Configuration 2M x 8

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | $V_{SS}$ | A | $\overline{W}$ | $\overline{NW_1}$ | $\overline{K}$ | NC | $\overline{R}$ | A | $V_{SS}$ | CQ |
| **B** | NC | NC | NC | A | NC | K | $\overline{NW_0}$ | A | NC | NC | Q3 |
| **C** | NC | NC | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | D3 |
| **D** | NC | D4 | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| **E** | NC | NC | Q4 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | D2 | Q2 |
| **F** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **G** | NC | D5 | Q5 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **H** | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | Q1 | D1 |
| **K** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **L** | NC | Q6 | D6 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | Q0 |
| **M** | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | D0 |
| **N** | NC | D7 | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | NC |
| **P** | NC | NC | Q7 | A | A | C | A | A | NC | NC | NC |
| **R** | TDO | TCK | A | A | A | $\overline{C}$ | A | A | A | TMS | TDI |

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## 165-ball FBGA Pinout
## TOP VIEW

## Pin Configuration 2M x 9

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | $V_{SS}$ | A | $\overline{W}$ | NC | $\overline{K}$ | NC | $\overline{R}$ | A | $V_{SS}$ | CQ |
| **B** | NC | NC | NC | A | NC | K | $\overline{BW}$ | A | NC | NC | Q3 |
| **C** | NC | NC | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | D3 |
| **D** | NC | D4 | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | NC |
| **E** | NC | NC | Q4 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | D2 | Q2 |
| **F** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **G** | NC | D5 | Q5 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **H** | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | Q1 | D1 |
| **K** | NC | NC | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | NC |
| **L** | NC | Q6 | D6 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | Q0 |
| **M** | NC | NC | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | D0 |
| **N** | NC | D7 | NC | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | NC |
| **P** | NC | NC | Q7 | A | A | C | A | A | NC | D8 | Q8 |
| **R** | TDO | TCK | A | A | A | $\overline{C}$ | A | A | A | TMS | TDI |

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**165-ball FBGA Pinout**
**TOP VIEW**

# Pin Configuration 1M x 18

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | $V_{SS}$ | NC | $\overline{W}$ | $\overline{BW1}$ | $\overline{K}$ | NC | $\overline{R}$ | A | $V_{SS}$ | CQ |
| **B** | NC | Q9 | D9 | A | NC | K | $\overline{BW0}$ | A | NC | NC | Q8 |
| **C** | NC | NC | D10 | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | Q7 | D8 |
| **D** | NC | D11 | Q10 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | NC | D7 |
| **E** | NC | NC | Q11 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | D6 | Q6 |
| **F** | NC | Q12 | D12 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | Q5 |
| **G** | NC | D13 | Q13 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | NC | D5 |
| **H** | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | NC | NC | D14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | Q4 | D4 |
| **K** | NC | NC | Q14 | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | D3 | Q3 |
| **L** | NC | Q15 | D15 | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | NC | Q2 |
| **M** | NC | NC | D16 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | NC | Q1 | D2 |
| **N** | NC | D17 | Q16 | $V_{SS}$ | A | A | A | $V_{SS}$ | NC | NC | D1 |
| **P** | NC | NC | Q17 | A | A | C | A | A | NC | D0 | Q0 |
| **R** | TDO | TCK | A | A | A | $\overline{C}$ | A | A | A | TMS | TDI |

6109 tbl 12b

## 165-ball FBGA Pinout
## TOP VIEW

# Pin Configuration 512K x 36

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $\overline{CQ}$ | $V_{SS}$ | NC | $\overline{W}$ | $\overline{BW_2}$ | $\overline{K}$ | $\overline{BW_1}$ | $\overline{R}$ | NC | $V_{SS}$ | CQ |
| **B** | $Q_{27}$ | $Q_{18}$ | $D_{18}$ | A | $\overline{BW_3}$ | K | $\overline{BW_0}$ | A | $D_{17}$ | $Q_{17}$ | $Q_8$ |
| **C** | $D_{27}$ | $Q_{28}$ | $D_{19}$ | $V_{SS}$ | A | A | A | $V_{SS}$ | $D_{16}$ | $Q_7$ | $D_8$ |
| **D** | $D_{28}$ | $D_{20}$ | $Q_{19}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $Q_{16}$ | $D_{15}$ | $D_7$ |
| **E** | $Q_{29}$ | $D_{29}$ | $Q_{20}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | $Q_{15}$ | $D_6$ | $Q_6$ |
| **F** | $Q_{30}$ | $Q_{21}$ | $D_{21}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $D_{14}$ | $Q_{14}$ | $Q_5$ |
| **G** | $D_{30}$ | $D_{22}$ | $Q_{22}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $Q_{13}$ | $D_{13}$ | $D_5$ |
| **H** | $\overline{Doff}$ | $V_{REF}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DDQ}$ | $V_{REF}$ | ZQ |
| **J** | $D_{31}$ | $Q_{31}$ | $D_{23}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $D_{12}$ | $Q_4$ | $D_4$ |
| **K** | $Q_{32}$ | $D_{32}$ | $Q_{23}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $Q_{12}$ | $D_3$ | $Q_3$ |
| **L** | $Q_{33}$ | $Q_{24}$ | $D_{24}$ | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | $D_{11}$ | $Q_{11}$ | $Q_2$ |
| **M** | $D_{33}$ | $Q_{34}$ | $D_{25}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $D_{10}$ | $Q_1$ | $D_2$ |
| **N** | $D_{34}$ | $D_{26}$ | $Q_{25}$ | $V_{SS}$ | A | A | A | $V_{SS}$ | $Q_{10}$ | $D_9$ | $D_1$ |
| **P** | $Q_{35}$ | $D_{35}$ | $Q_{26}$ | A | A | C | A | A | $Q_9$ | $D_0$ | $Q_0$ |
| **R** | TDO | TCK | A | A | A | $\overline{C}$ | A | A | A | TMS | TDI |

6109 tbl 12c

**165-ball FBGA Pinout**
**TOP VIEW**

## Absolute Maximum Ratings[1]

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Supply Voltage on $V_{DD}$ with Respect to GND | –0.5 to +2.9 | V |
| $V_{TERM}$ | Supply Voltage on $V_{DDQ}$ with Respect to GND | –0.5 to $V_{DD}$+0.3 | V |
| $V_{TERM}$ | Voltage on Input, Output and I/O terminals with respect to GND | –0.5 to $V_{DDQ}$+0.3 | V |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | Continuous Current into Outputs | ± 20 | mA |

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**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Write Descriptions[1,2]

| Signal | $\overline{BW_0}$ | $\overline{BW_1}$ | $\overline{BW_2}$ | $\overline{BW_3}$ | $\overline{NW_0}$ | $\overline{NW_1}$ |
|---|---|---|---|---|---|---|
| Write Byte 0 | L | X | X | X | X | X |
| Write Byte 1 | X | L | X | X | X | X |
| Write Byte 2 | X | X | L | X | X | X |
| Write Byte 3 | X | X | X | L | X | X |
| Write Nibble 0 | X | X | X | X | L | X |
| Write Nibble 1 | X | X | X | X | X | L |

6109 tbl 09

### Notes:
1) All byte write ($\overline{BW}$x) and nibble write ($\overline{NW}$x) signals are sampled on the rising edge of K and again on $\overline{K}$. The data that is present on the data bus in the designated byte/nibble will be latched into the input if the corresponding $\overline{BW}$x or $\overline{NW}$x is held low. The rising edge of K will sample the first byte/nibble of the two word burst and the rising edge of $\overline{K}$ will sample the second byte/ nibble of the two word burst.
2) The availability of the $\overline{BW}$x or $\overline{NW}$x on designated devices is described in the pin description table.
3) The QDRII Burst of two SRAM has data forwarding. A read request that is initiated on the same cycle as a write request to the same address will produce the newly written data in response to the read request.

## Capacitance (TA = +25°C, f = 1.0MHz)[1]

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{DD}$ = 1.8V<br>$V_{DDQ}$ = 1.5V | 5 | pF |
| $C_{CLK}$ | Clock Input Capacitance | | 6 | pF |
| $C_O$ | Output Capacitance | | 7 | pF |

6109 tbl 06

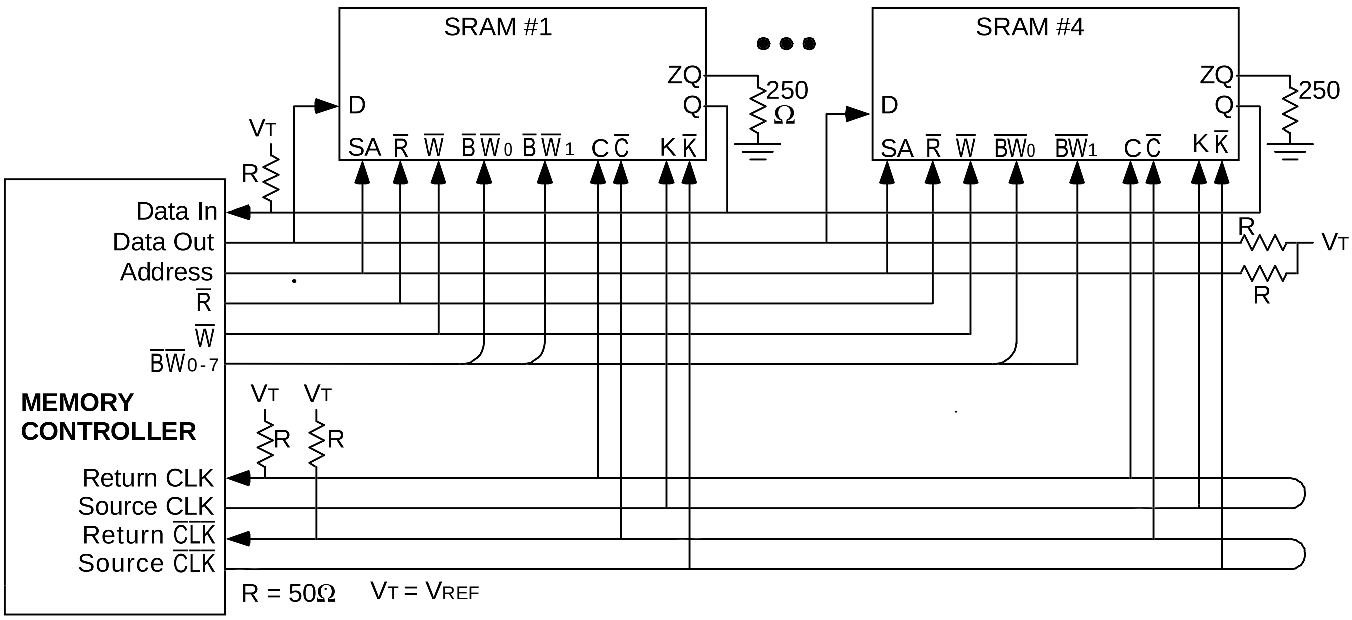
**NOTE:**
1. Tested at characterization and retested after any design or process change that may affect these parameters.

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 1.7 | 1.8 | 1.9 | V |
| $V_{DDQ}$ | I/O Supply Voltage | 1.4 | 1.5 | 1.9 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{REF}$ | Input Reference Voltage | - | $V_{DDQ/2}$ | - | V |
| $V_{IH}$ | Input High Voltage | $V_{REF}$+0.1 | – | $V_{DDQ}$+0.3 | V |
| $V_{IL}$ | Input Low Voltage | –0.3 | – | $V_{REF}$–0.1 | V |
| $T_A$ | Ambient Temperature | 0 | 25 | +70 | °C |

6109 tbl 04

# Application Example




6109 drw 20

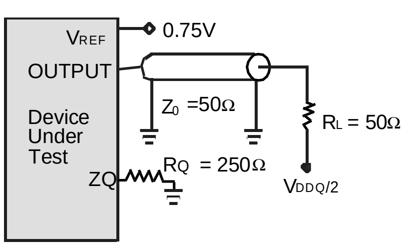
# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD}$ = 1.8 ± 100mV, $V_{DDQ}$ = 1.4V to 1.9V)

| Parameter | Symbol | Test Conditions | | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | $V_{DD}$ = Max $V_{IN}$ = $V_{SS}$ to $V_{DDQ}$ | | -10 | +10 | µA | |
| Output Leakage Current | $I_{OL}$ | Output Disabled | | -10 | +10 | µA | |
| Operating Current (x36,x18,x9,x8) DDR | $I_{DD}$ | $V_{DD}$ = Max, $I_{OUT}$ = 0mA Cycle Time ≥ $t_{KHKH}$ Min | 250MHz | - | TBD | mA | 1,5 |
| | | | 200MHz | - | TBD | | |
| | | | 167MHz | - | TBD | | |
| | | | 133MHz | - | TBD | | |
| Standby Current (NOP): DDR | $I_{SB1}$ | Device Deselected, $I_{OUT}$ = 0mA, f=Max, All Inputs ≤0.2V or > VDD -0.2V | 250MHz | - | TBD | mA | 1,6 |
| | | | 200MHz | - | TBD | | |
| | | | 167MHz | - | TBD | | |
| | | | 133MHz | - | TBD | | |
| Output High Voltage | $V_{OH1}$ | See Note 2 | | $V_{DDQ}$/2-0.12 | $V_{DDQ}$/2+0.12 | V | 2,7 |
| Output Low Voltage | $V_{OL1}$ | See Note 3 | | $V_{DDQ}$/2-0.12 | $V_{DDQ}$/2+0.12 | V | 3,7 |
| Output High Voltage | $V_{OH2}$ | $I_{OH}$ = -0.1mA | | $V_{DDQ}$-0.2 | $V_{DDQ}$ | V | 4 |
| Output Low Voltage | $V_{OL2}$ | $I_{OL}$ = 0.1mA | | $V_{SS}$ | 0.2 | V | 4 |
| Input Low Voltage | $V_{IL}$ | | | -0.3 | $V_{REF}$-0.1 | V | 8,9 |
| Input High Voltage | $V_{IH}$ | | | $V_{REF}$+0.1 | $V_{DDQ}$+0.3 | V | 8,10 |

6109 tbl 10c

**Notes:**
1. Minimum cycle. $I_{OUT}$ = 0mA.
2. $I_{OH}$ = -($V_{DDQ}$/2)/(RQ/5) for 175Ω ≤ RQ < 350Ω.
3. $I_{OL}$ = ($V_{DDQ}$/2)/(RQ/5) for 175Ω ≤ RQ < 350Ω.
4. Minimum Impedance Mode when ZQ pin is connected to $V_{DDQ}$.
5. Operating Current is calculated with 50% read cycles and 50% write cycles.
6. Standby Current is only after all pending read and write burst operations are completed.
7. Programmable Impedance Mode.
8. These are DC test criteria. DC design criteria is $V_{REF}$ ± 50mV. The AC $V_{IH}$/$V_{IL}$ levels are defined separately for measuring timing parameters.
9. $V_{IL}$ (Min) DC = -0.3V, $V_{IL}$ (Min) AC = -1.5V (pulse width ≤3ns).
10. $V_{IH}$ (Max) DC = $V_{DDQ}$+0.3, $V_{IH}$ (Max) AC = $V_{DDQ}$+0.85V (pulse width≤3ns)

# AC Test Loads



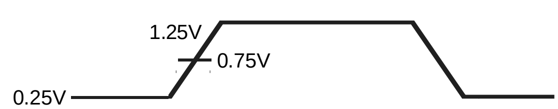

6109 drw 04

# AC Test Conditions

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Core Power Supply Voltage | $V_{DD}$ | 1.7-1.9 | V |
| Output Power Supply Voltage | $V_{DDQ}$ | 1.4-1.9 | V |
| Input High/Low Level | $V_{IH}$/$V_{IL}$ | 1.25/0.25 | V |
| Input Reference Level | VREF | 0.75 | V |
| Input Rise/Fall Time | TR/TF | 0.6/0.6 | ns |
| Output Timing Reference Level | | $V_{DDQ}$/2 | V |

6109tbl 11a

**NOTE:**
1. Parameters are tested with RQ=250Ω




6109 drw 06

# AC Electrical Characteristics ($V_{DD}$ = 1.8 ± 100mV, $V_{DDQ}$ = 1.4V to 1.9V)(3)

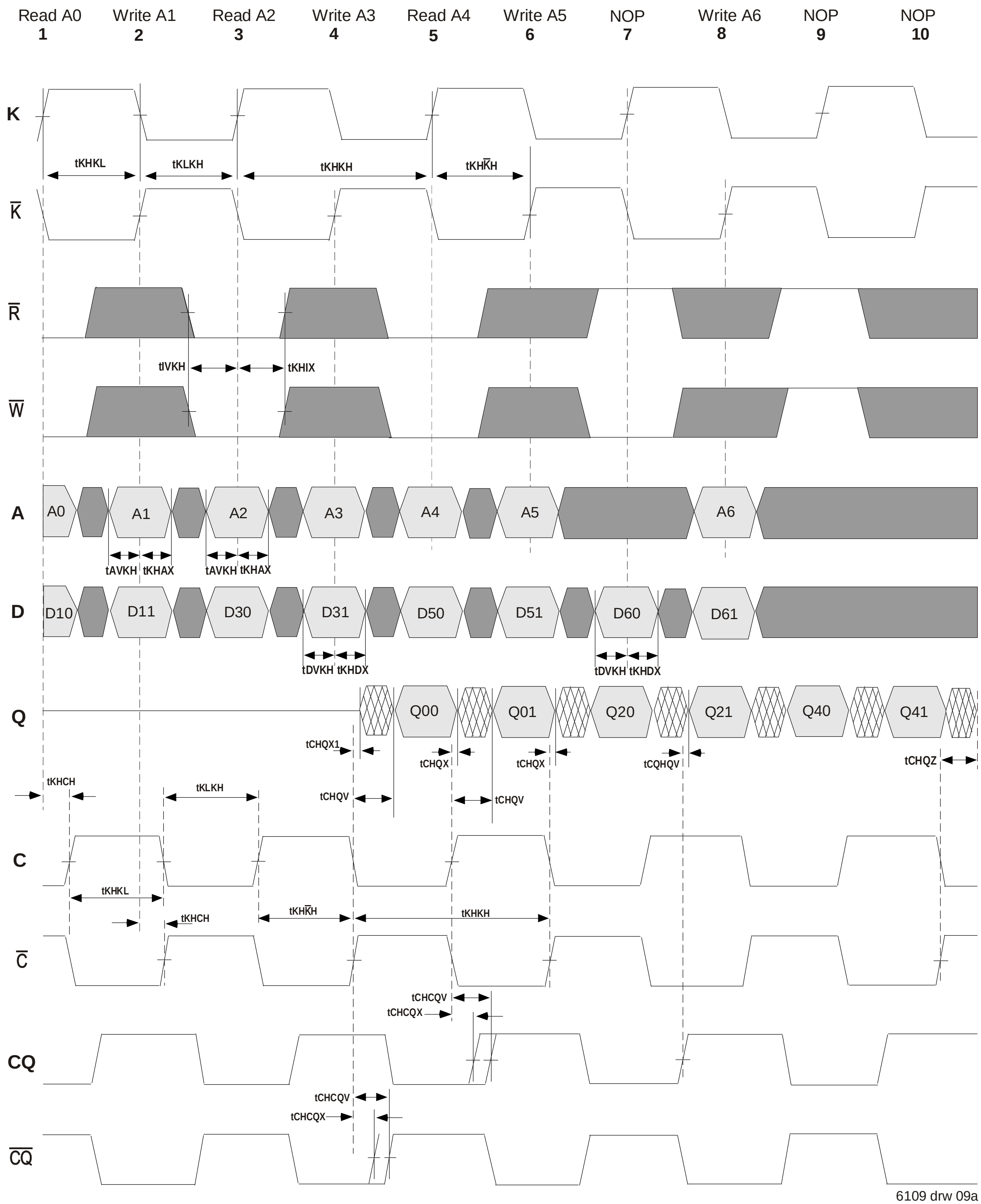
| Symbol | Parameter | 250MHz | | 200MHz | | 167MHz | | 133MHz | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max | Min. | Max | Min. | Max | Min | Max | | |
| **Clock Parameters** | | | | | | | | | | | |
| $t_{KHKH}$ | Average clock cycle time (K,$\overline{K}$,C,C) | 4.00 | 5.25 | 5.00 | 6.30 | 6.00 | 7.88 | 7.50 | 8.40 | ns | |
| $t_{KC\ var}$ | Clock Phase Jitter (K,$\overline{K}$,C,$\overline{C}$) | - | 0.20 | - | 0.20 | - | 0.20 | - | 0.20 | ns | 5 |
| $t_{KHKL}$ | Clock High Time (K,$\overline{K}$,C,$\overline{C}$) | 1.60 | - | 2.00 | - | 2.40 | - | 3.00 | - | ns | |
| $t_{KLKH}$ | Clock LOW Time (K,$\overline{K}$,C,$\overline{C}$) | 1.60 | - | 2.00 | - | 2.40 | - | 3.00 | - | ns | |
| $t_{KH\overline{K}H}$ | Clock to $\overline{clock}$ (K→$\overline{K}$,C→$\overline{C}$) | 1.80 | - | 2.20 | - | 2.70 | - | 3.38 | - | ns | |
| $t_{\overline{K}HKH}$ | Clock to $\overline{clock}$ ($\overline{K}$→K,$\overline{C}$→C) | 1.80 | - | 2.20 | - | 2.70 | - | 3.38 | - | ns | |
| $t_{KHCH}$ | Clock to data clock (K→C,$\overline{K}$→$\overline{C}$) | 0.00 | 1.80 | 0.00 | 2.30 | 0.00 | 2.80 | 0.00 | 3.55 | ns | |
| $t_{KC\ lock}$ | DLL lock time (K, C) | 1024 | - | 1024 | - | 1024 | - | 1024 | - | cycles | 6 |
| $t_{KC\ reset}$ | K static to DLL reset | 30 | - | 30 | - | 30 | - | 30 | - | ns | |
| **Output Parameters** | | | | | | | | | | | |
| $t_{CHQV}$ | C,$\overline{C}$ HIGH to output valid | - | 0.45 | - | 0.45 | - | 0.50 | - | 0.50 | ns | 3 |
| $t_{CHQX}$ | C,$\overline{C}$ HIGH to output hold | -0.45 | - | -0.45 | - | -0.50 | - | -0.50 | - | ns | 3 |
| $t_{CHCQV}$ | C,$\overline{C}$ HIGH to echo clock valid | - | 0.45 | - | 0.45 | - | 0.50 | - | 0.50 | ns | |
| $t_{CHCQX}$ | C,$\overline{C}$ HIGH to echo clock hold | -0.45 | - | -0.45 | - | -0.50 | - | -0.50 | - | ns | |
| $t_{CQHQV}$ | CQ,$\overline{CQ}$ HIGH to output valid | - | 0.30 | - | 0.35 | - | 0.40 | - | 0.40 | ns | 7 |
| $t_{CQHQX}$ | CQ,$\overline{CQ}$ HIGH to output hold | -0.30 | - | -0.35 | - | -0.40 | - | -0.40 | - | ns | 7 |
| $t_{CHQZ}$ | $\overline{C}$ HIGH to output High-Z | - | 0.45 | - | 0.45 | - | 0.50 | - | 0.50 | ns | 3 |
| $t_{CHQX1}$ | $\overline{C}$ HIGH to output Low-Z | -0.45 | - | -0.45 | - | -0.50 | - | -0.50 | - | ns | 3 |
| **Set-Up Times** | | | | | | | | | | | |
| $t_{AVKH}$ | Address valid to K,$\overline{K}$ rising edge | 0.40 | - | 0.40 | - | 0.50 | - | 0.50 | - | ns | |
| $t_{IVKH}$ | Control inputs valid to K,$\overline{K}$ rising edge | 0.40 | - | 0.40 | - | 0.50 | - | 0.50 | - | ns | 2 |
| $t_{DVKH}$ | Date-in valid to K, $\overline{K}$ rising edge | 0.40 | - | 0.40 | - | 0.50 | - | 0.50 | - | ns | |
| **Hold Times** | | | | | | | | | | | |
| $t_{KHAX}$ | K,$\overline{K}$ rising edge to address hold | 0.40 | - | 0.40 | - | 0.50 | - | 0.50 | - | ns | |
| $t_{KHIX}$ | K,$\overline{K}$ rising edge to control inputs hold | 0.40 | - | 0.40 | - | 0.50 | - | 0.50 | - | ns | |
| $t_{KHDX}$ | K, $\overline{K}$ rising edge to data-in hold | 0.40 | - | 0.40 | - | 0.50 | - | 0.50 | - | ns | |

6109 tbl 11

**NOTES:**

1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are $\overline{R}$, $\overline{W}$,$\overline{BW_0}$,$\overline{BW_1}$ and ($\overline{NW_0}$,$\overline{NW_1}$, for x8) and ($\overline{BW_2}$,$\overline{BW_3}$ also for x36)
3. If C,$\overline{C}$ are tied high, K,$\overline{K}$ become the references for C,$\overline{C}$ timing parameters.
4. To avoid bus contention, at a given voltage and temperature $t_{CHQX1}$ is bigger than tCHQZ.
   The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7V)
   It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. $V_{dd}$ slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
7. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ± 0.1 ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.

# Timing Waveform of Combined Read and Write Cycles

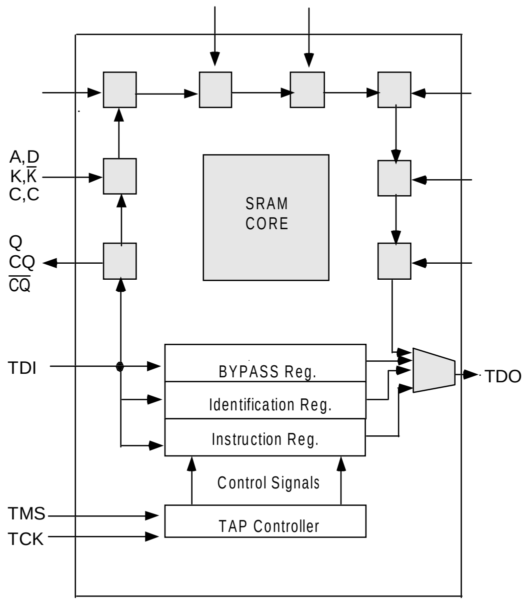



6109 drw 09a

## IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

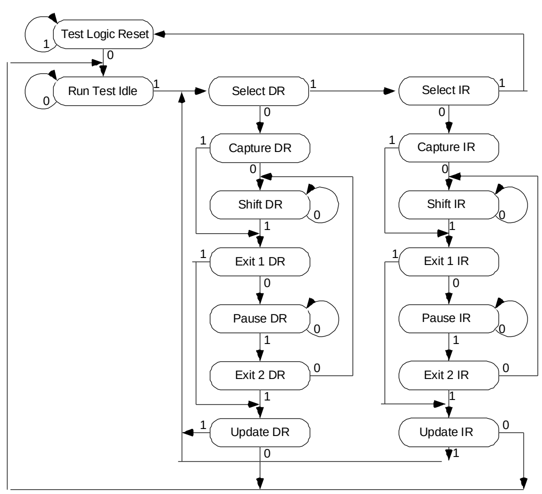
This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, the TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to VSS to preclude a mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected, but they may also be tied to VDD through a register. TDO should be left unconnected.

### JTAG Block Diagram




6109 drw 18

### TAP Controller State Diagram




6109 drw 17

### JTAG Instruction Coding

| IR2 | IR1 | IR0 | Instruction | TDO Output | Notes |
|---|---|---|---|---|---|
| 0 | 0 | 0 | EXTEST | Boundary Scan Register | |
| 0 | 0 | 1 | IDCODE | Identification register | 2 |
| 0 | 1 | 0 | SAMPLE-Z | Boundary Scan Register | 1 |
| 0 | 1 | 1 | RESERVED | Do Not Use | 5 |
| 1 | 0 | 0 | SAMPLE/PRELOAD | Boundary Scan register | 4 |
| 1 | 0 | 1 | RESERVED | Do Not Use | 5 |
| 1 | 1 | 0 | RESERVED | Do Not Use | 5 |
| 1 | 1 | 1 | BYPASS | Bypass Register | 3 |

6109tbl 13

**NOTE:**

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not place Qs in Hi-Z.
5. This instruction is reserved for future use.

## Scan Register Definition

| Part | Instruction Register | Bypass Register | ID Register | Boundary Scan |
|---|---|---|---|---|
| 512Kx36 | 3 bits | 1 bit | 32 bits | 109 bits |
| 1Mx18 | 3 bits | 1 bit | 32 bits | 109 bits |
| 2Mx8/x9 | 3 bits | 1 bit | 32 bits | 109 bits |

6109 tbl 14

## Identification Register Definitions

| INSTRUCTION FIELD | ALL DEVICES | DESCRIPTION | PART NUMBER |
|---|---|---|---|
| Revision Number (31:29) | 000 | Revision Number | |
| Device ID (28:12) | 0010 0100 0100<br>0010 0100 0101<br>0010 0100 0110<br>0010 0100 0111 | 512Kx36 QDRII Burst of 2<br>1Mx18<br>2Mx9<br>2Mx8 | 71P72604S<br>71P72804S<br>71P72104S<br>71P72204S |
| IDT JEDEC ID CODE (11:1) | 0x33 | Allows unique identification of SRAM vendor. | |
| ID Register Presence Indicator (0) | 1 | Indicates the presence of an ID register. | |

6109 tbl 15

## Boundary Scan Exit Order

| ORDER | PIN ID |
|---|---|
| 1 | 6R |
| 2 | 6P |
| 3 | 6N |
| 4 | 7P |
| 5 | 7N |
| 6 | 7R |
| 7 | 8R |
| 8 | 8P |
| 9 | 9R |
| 10 | 11P |
| 11 | 10P |
| 12 | 10N |
| 13 | 9P |
| 14 | 10M |
| 15 | 11N |
| 16 | 9M |
| 17 | 9N |
| 18 | 11L |
| 19 | 11M |
| 20 | 9L |
| 21 | 10L |
| 22 | 11K |
| 23 | 10K |
| 24 | 9J |
| 25 | 9K |
| 26 | 10J |
| 27 | 11J |
| 28 | 11H |
| 29 | 10G |
| 30 | 9G |
| 31 | 11F |
| 32 | 11G |
| 33 | 9F |
| 34 | 10F |
| 35 | 11E |
| 36 | 10E |

6109 tbl 16

| ORDER | PIN ID |
|---|---|
| 37 | 10D |
| 38 | 9E |
| 39 | 10C |
| 40 | 11D |
| 41 | 9C |
| 42 | 9D |
| 43 | 11B |
| 44 | 11C |
| 45 | 9B |
| 46 | 10B |
| 47 | 11A |
| 48 | 10A |
| 49 | 9A |
| 50 | 8B |
| 51 | 7C |
| 52 | 6C |
| 53 | 8A |
| 54 | 7A |
| 55 | 7B |
| 56 | 6B |
| 57 | 6A |
| 58 | 5B |
| 59 | 5A |
| 60 | 4A |
| 61 | 5C |
| 62 | 4B |
| 63 | 3A |
| 64 | $V_{SS}$ |
| 65 | 1A |
| 66 | 2B |
| 67 | 3B |
| 68 | 1C |
| 69 | 1B |
| 70 | 3D |
| 71 | 3C |
| 72 | 1D |

6109 tbl 17

| ORDER | PIN ID |
|---|---|
| 73 | 2C |
| 74 | 3E |
| 75 | 2D |
| 76 | 2E |
| 77 | 1E |
| 78 | 2F |
| 79 | 3F |
| 80 | 1G |
| 81 | 1F |
| 82 | 3G |
| 83 | 2G |
| 84 | 1H |
| 85 | 1J |
| 86 | 2J |
| 87 | 3K |
| 88 | 3J |
| 89 | 2K |
| 90 | 1K |
| 91 | 2L |
| 92 | 3L |
| 93 | 1M |
| 94 | 1L |
| 95 | 3N |
| 96 | 3M |
| 97 | 1N |
| 98 | 2M |
| 99 | 3P |
| 100 | 2N |
| 101 | 2P |
| 102 | 1P |
| 103 | 3R |
| 104 | 4R |
| 105 | 4P |
| 106 | 5P |
| 107 | 5N |
| 108 | 5R |

6109 tbl 18

## JTAG DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Output Power Supply | VDDQ | 1.4 | - | 1.9 | V | |
| Power Supply Voltage | VDD | 1.7 | 1.8 | 1.9 | V | |
| Input High Level | VIH | 1.3 | - | VDD+0.3 | V | |
| Input Low Level | VIL | -0.3 | - | 0.5 | V | |
| Output High Voltage (IOH = -1mA) | VOH | VDDQ - 0.2 | - | VDD | V | 1 |
| Output Low Voltage (IOL = 1mA) | VOL | VSS | - | 0.2 | V | 1 |

Note: 1. ZQ = VDDQ2

6109 tbl 19

## JTAG AC Test Conditions

| Parameter | Symbol | Min | Unit | Note |
|---|---|---|---|---|
| Input High/Low Level | VIH/VIL | 1.3/0.5 | V | |
| Input Rise/Fall Time | TR/TF | 1.0/1.0 | ns | |
| Input and Output Timing Reference Level | | VDDQ/2 | V | |

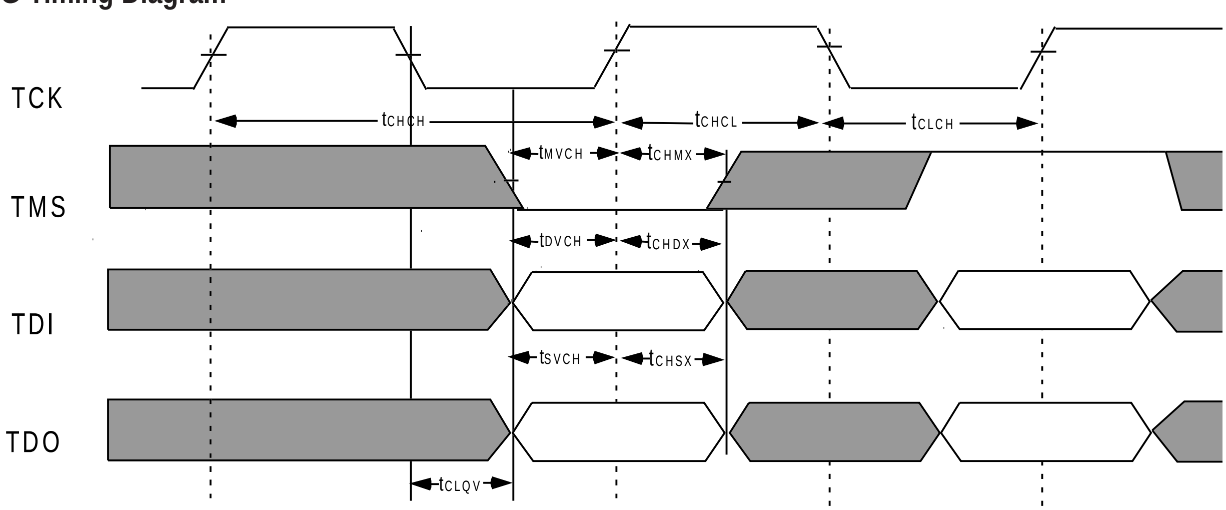
6109 tbl 20

## JTAG AC Characteristics

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| TCK Cycle Time | tCHCH | 50 | - | ns | |
| TCK High Pulse Width | tCHCL | 20 | - | ns | |
| TCK Low Pulse Width | tCLCH | 20 | - | ns | |
| TMS Input Setup Time | tMVCH | 5 | - | ns | |
| TMS Input Hold Time | tCHMX | 5 | - | ns | |
| TDI Input Setup Time | tDVCH | 5 | - | ns | |
| TDI Input Hold Time | tCHDX | 5 | - | ns | |
| SRAM Input Setup Time | tSVCH | 5 | - | ns | |
| SRAM Input Hold Time | tCHSX | 5 | - | ns | |
| Clock Low to Output Valid | tCLQV | 0 | 10 | ns | |

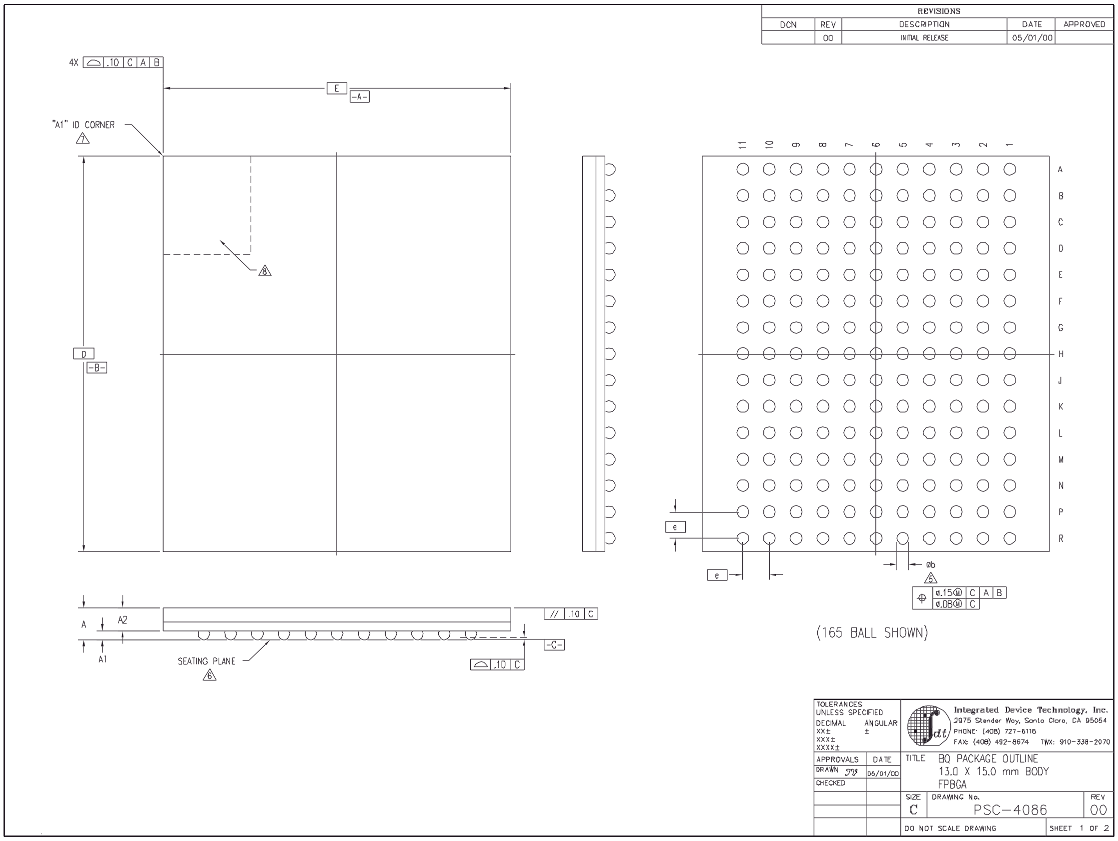
6109 tbl.21

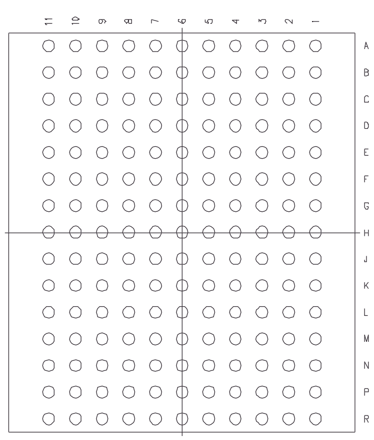
## JTAG Timing Diagram




6109 drw 19

# Package Diagram Outline for 165-Ball Fine Pitch Grid Array




REVISIONS

| DCN | REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|---|
| | 00 | INITIAL RELEASE | 05/01/00 | |

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2 "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH

3 "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE

4 "N" REPRESENTS THE BALLCOUNT NUMBER

5 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

6 SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

7 "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY

8 IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED

9 ALL DIMENSIONS ARE IN MILLIMETERS

| SYMBOL | JEDEC VARIATION NOT YET REGISTERED | | | NOTE |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| A | – | – | 1.20 | |
| A1 | .30 | .35 | .40 | |
| A2 | .78 | .85 | .92 | |
| D | 15.00 BSC | | | |
| E | 13.00 BSC | | | |
| M | 11 X 15 | | | 3 |
| N | 165 | | | 4 |
| e | 1.00 BSC | | | |
| b | .35 | .45 | .50 | 5 |
| CENTER BALL MATRIX | N/A | | | |

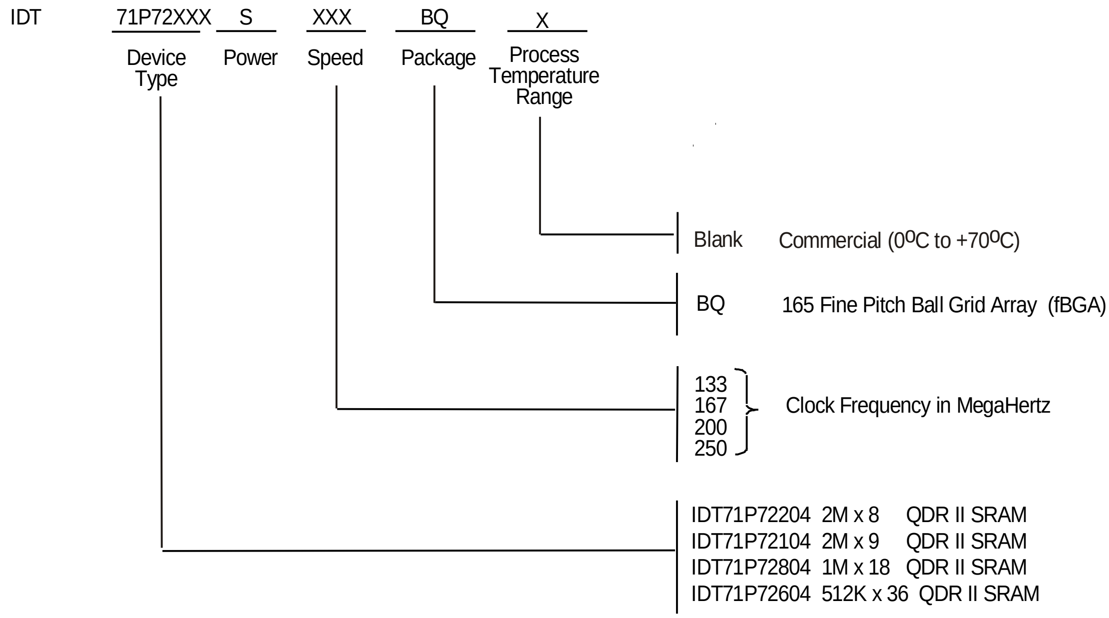
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054

TITLE BQ PACKAGE OUTLINE 13.0 X 15.0 mm BODY FPBGA

SIZE C DRAWING No. PSC-4086 REV 00

DO NOT SCALE DRAWING SHEET 2 OF 2

## Ordering Information

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# Revision History

| Revision | Date | Pages | Description |
|---|---|---|---|
| O | 8/1/03 | 1-20 | Initial Advance Information Data Sheet Release |