

1M x 8 HIGH-SPEED CMOS STATIC RAM

ADVANCED INFORMATION
MAY 2002

FEATURES

- High-speed access times:
8, 10, 12 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ options
- $\overline{\text{CE}}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
 - 48-ball miniBGA (9mm x 11mm)
 - 36-ball miniBGA (9mm x 11mm)
 - 44-pin TSOP (Type II)

DESCRIPTION

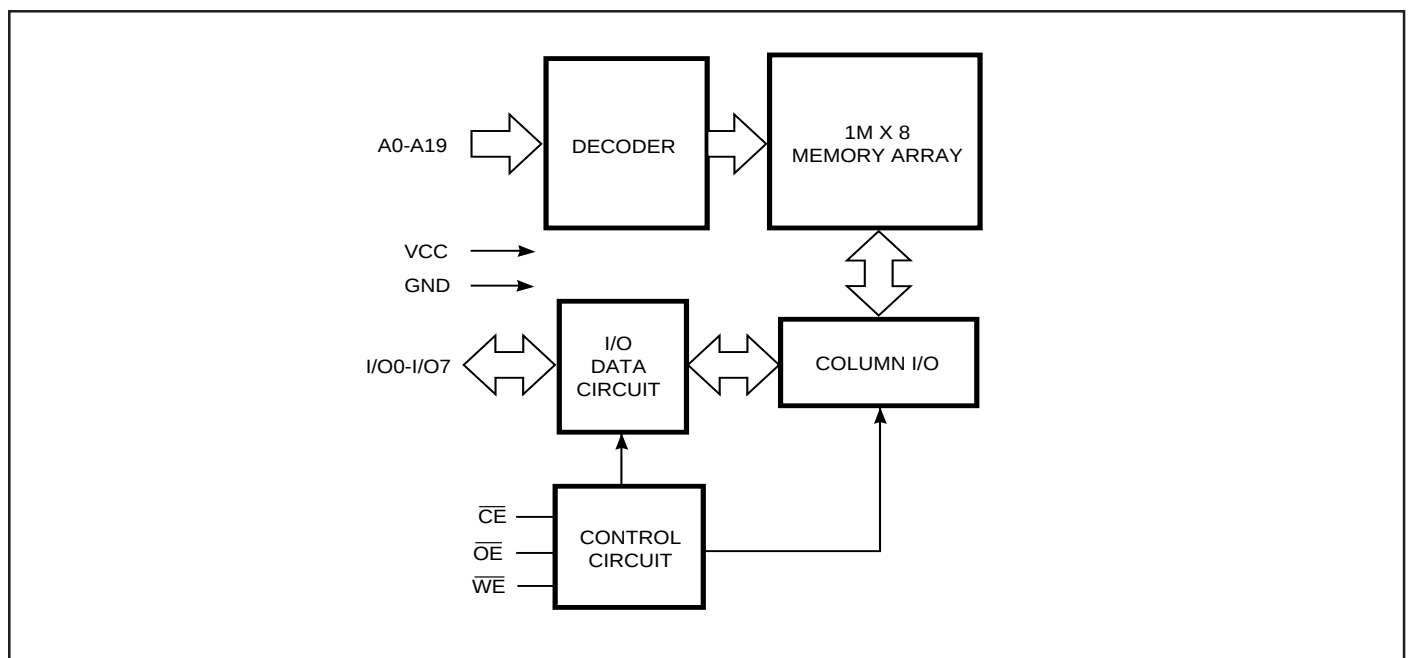
The *ISSI* IS61LV10008 is a very high-speed, low power, 1M-word by 8-bit CMOS static RAM. The IS61LV10008 is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 μW (typical) with CMOS input levels.

The IS61LV10008 operates from a single 3.3V power supply and all inputs are TTL-compatible.

The IS61LV10008 is available in 48 ball mini BGA, 36-ball mini BGA, and 44-pin TSOP (Type II) packages.

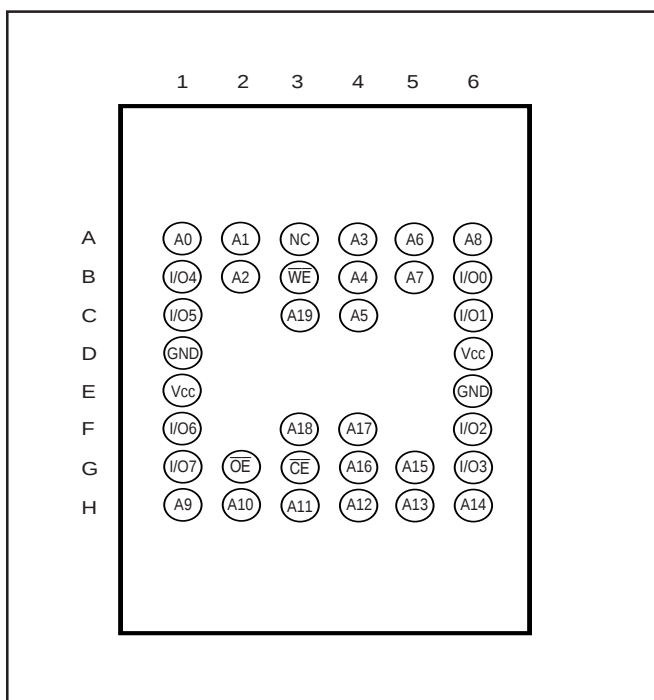
FUNCTIONAL BLOCK DIAGRAM



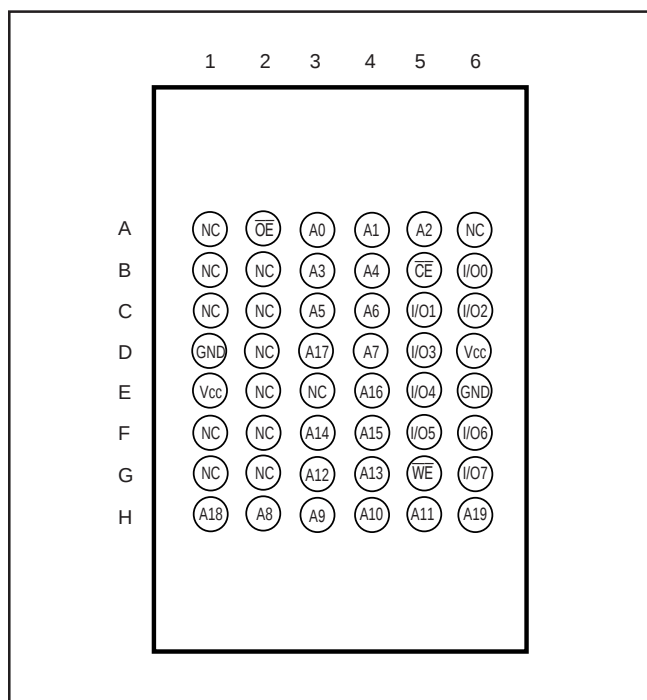
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PIN CONFIGURATION

36 mini BGA (B)



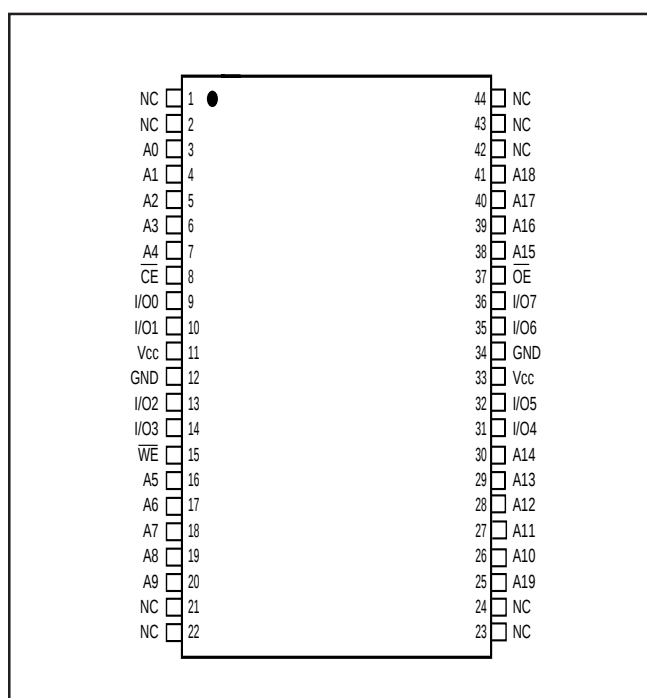
48-pin Mini BGA (M) (9mm x 11mm)



PIN DESCRIPTIONS

A0-A19	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Data Input / Output
Vcc	Power
GND	Ground
NC	No Connection

44-pin TSOP (Type II)



TRUTH TABLE

Mode	$\overline{WE}$	$\overline{OE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{CC}
Read	H	L	L	D _{OUT}	I _{CC}
Write	L	L	X	D _{IN}	I _{CC}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{CC} + 0.5	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V +10%, -5%
Industrial	-40°C to +85°C	3.3V +10%, -5%

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	Com. Ind.	-1 5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled	Com. Ind.	-1 5	μA

Note:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-8		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX}	Com. Ind.	— 230 — 240	— 220 — 230	— 210 — 220	— 210 — 220	— 210 — 220	mA
I _{SB}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = f _{MAX} .	Com. Ind.	— 70 — 80	— 60 — 70	— 50 — 60	— 50 — 60	— 50 — 60	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com. Ind.	— 50 — 55	— 50 — 55	— 50 — 55	— 50 — 55	— 50 — 55	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com. Ind.	— 40 — 45	— 40 — 45	— 40 — 45	— 40 — 45	— 40 — 45	mA

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

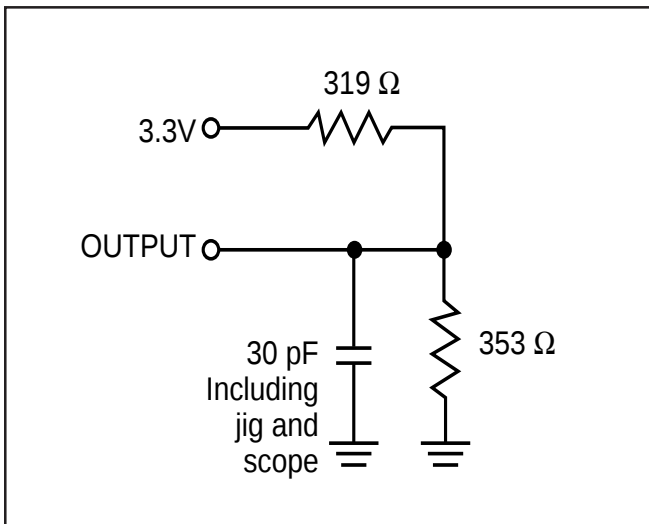
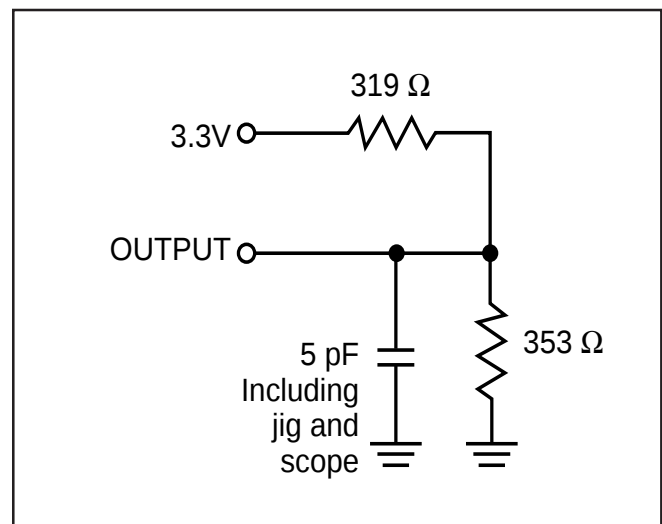
Symbol	Parameter	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t _{AA}	Address Access Time	—	8	—	10	—	12	ns
t _{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t _{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	ns
t _{DOE}	$\overline{OE}$ Access Time	—	3.5	—	4	—	5	ns
t _{HZE⁽²⁾}	$\overline{OE}$ to High-Z Output	—	3	—	4	—	5	ns
t _{LZE⁽²⁾}	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t _{HZCE⁽²⁾}	$\overline{CE}$ to High-Z Output	—	3	0	4	0	6	ns
t _{LZCE⁽²⁾}	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t _{BA}	$\overline{LB}, \overline{UB}$ Access Time	—	3.5	—	4	—	5	ns
t _{HZB⁽²⁾}	$\overline{LB}, \overline{UB}$ to High-Z Output	0	3	0	3	0	4	ns
t _{LZB⁽²⁾}	$\overline{LB}, \overline{UB}$ to Low-Z Output	0	—	0	—	0	—	ns
t _{PU}	Power Up Time	0	—	0	—	0	—	ns
t _{PD}	Power Down Time	—	8	—	10	—	12	ns

Notes:

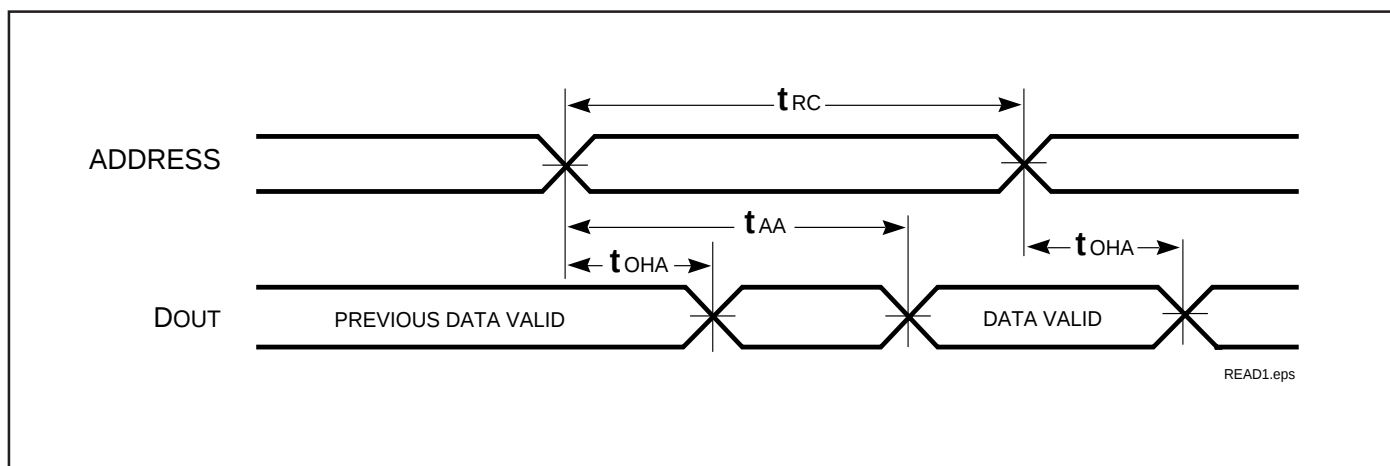
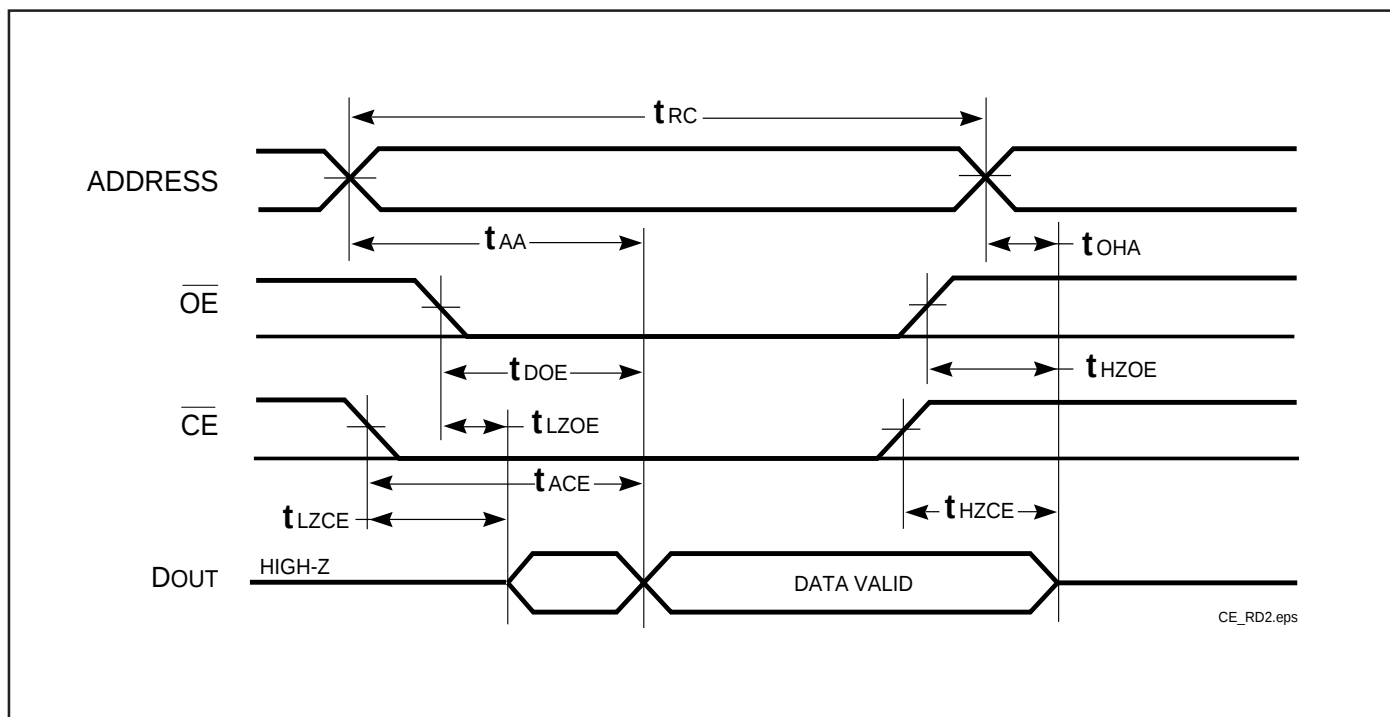
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-stat voltage.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS**Figure 1****Figure 2**

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)READ CYCLE NO. 2^(1,3) ($\overline{CE}$ and $\overline{OE}$ Controlled)

Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

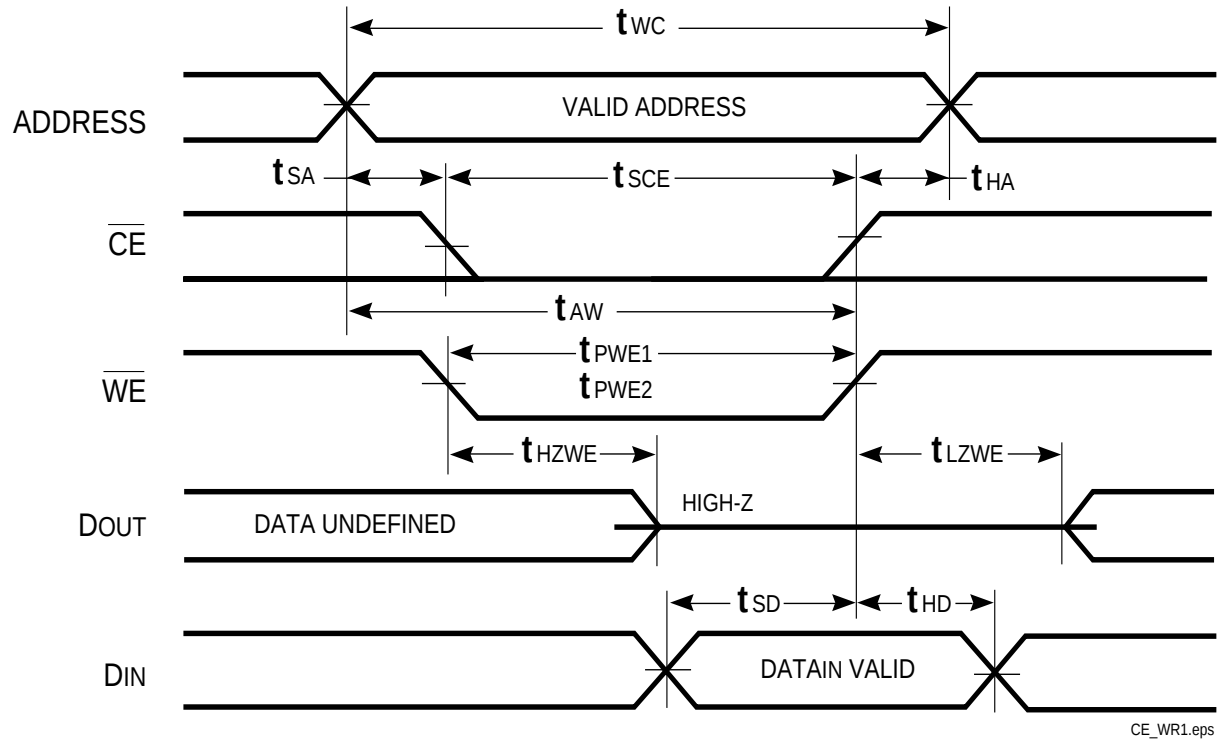
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t _{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	9	—	ns
t _{AW}	Address Setup Time to Write End	6.5	—	8	—	9	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	6.5	—	8	—	8	—	ns
t _{PWE1}	$\overline{WE}$ Pulse Width	6.5	—	8	—	8	—	ns
t _{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	6.5	—	10	—	12	—	ns
t _{SD}	Data Setup to Write End	4	—	6	—	6	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	—	6	ns
t _{LZWE} ⁽²⁾	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	2	—	ns

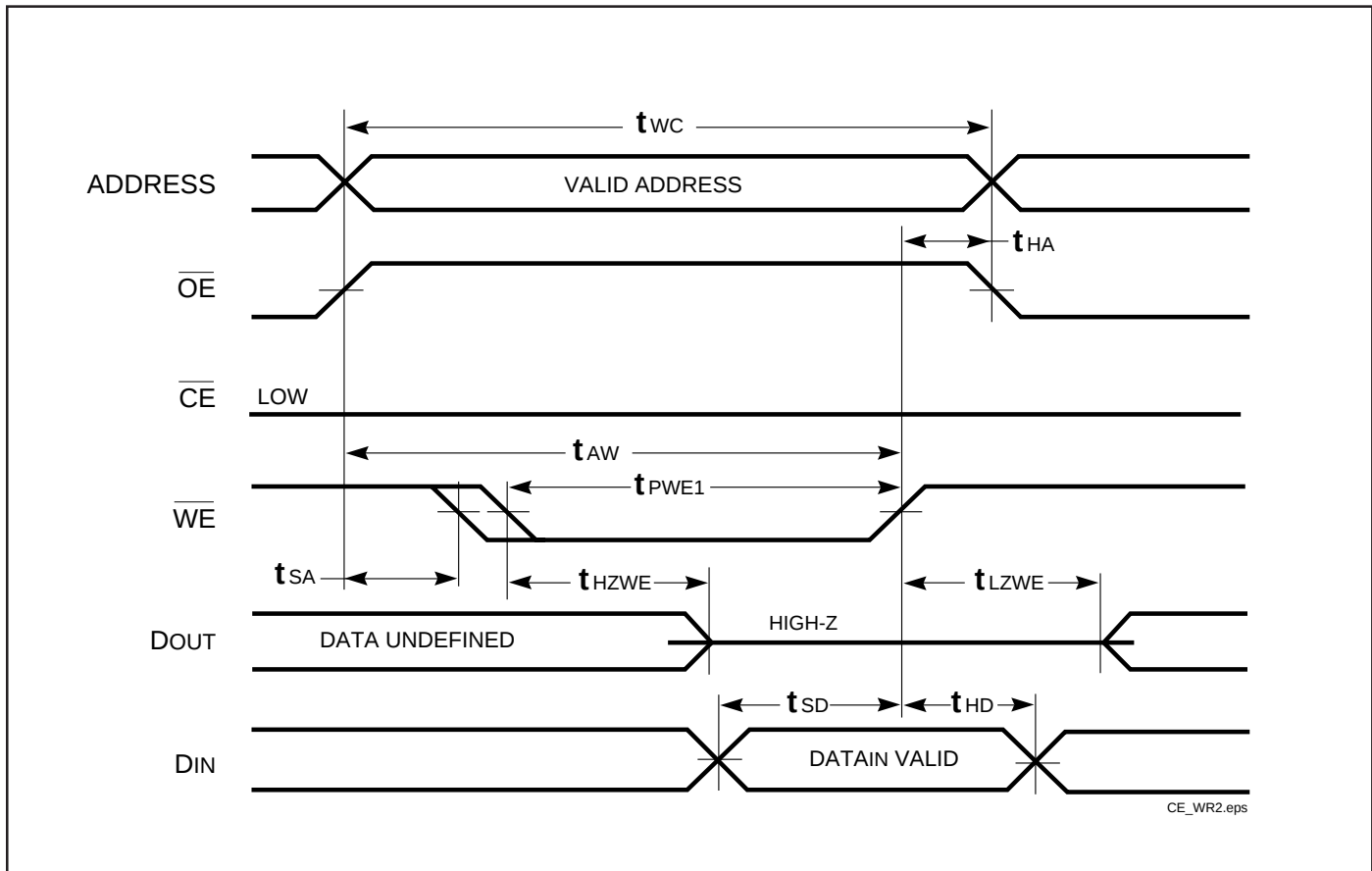
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

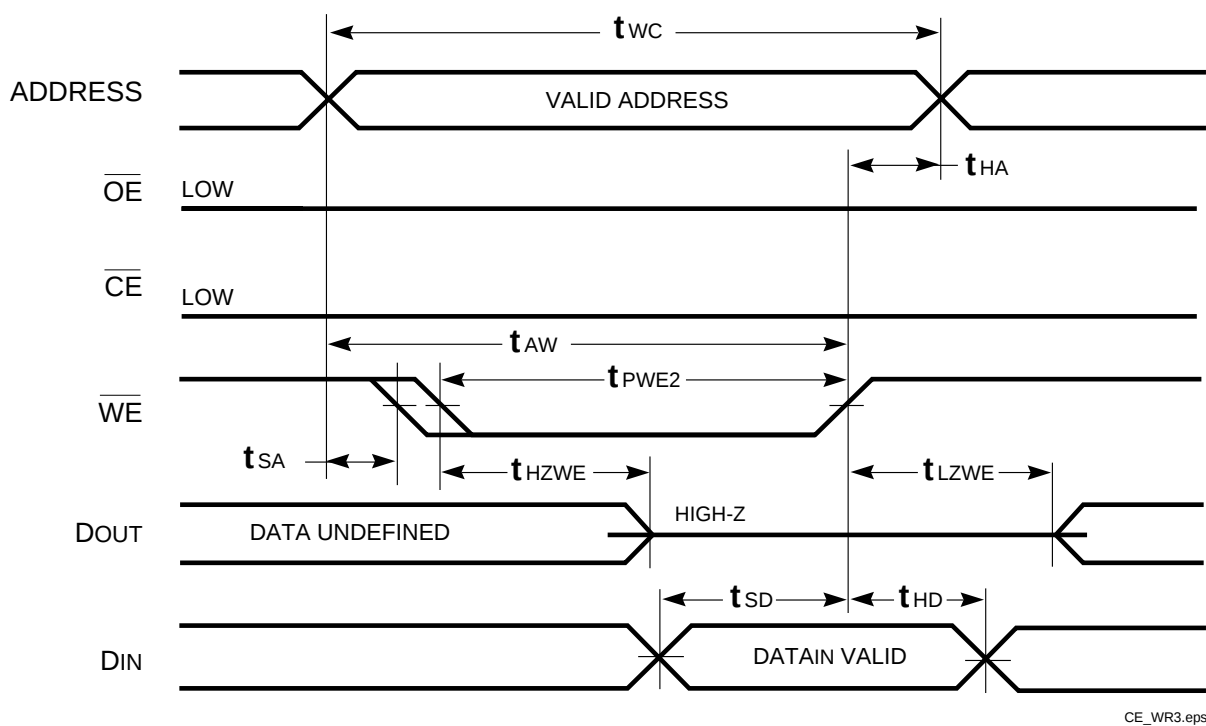
AC WAVEFORMS

WRITE CYCLE NO. 2^(1,2) ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)

Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \cdot V_{IH}$.

AC WAVEFORMS

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
8	IS61LV10008-8M	48 mini BGA (9mm x 11mm)
	IS61LV10008-8T	TSOP (Type II)
	IS61LV10008-8B	36 mini BGA (9mm x 11mm)
10	IS61LV10008-10M	48 mini BGA (9mm x 11mm)
	IS61LV10008-10T	TSOP (Type II)
	IS61LV10008-10B	36 mini BGA (9mm x 11mm)
12	IS61LV10008-12M	48 mini BGA (9mm x 11mm)
	IS61LV10008-12T	TSOP (Type II)
	IS61LV10008-12B	36 mini BGA (9mm x 11mm)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
8	IS61LV10008-8MI	48 mini BGA (9mm x 11mm)
	IS61LV10008-8TI	TSOP (Type II)
	IS61LV10008-8BI	36 mini BGA (9mm x 11mm)
10	IS61LV10008-10MI	48 mini BGA (9mm x 11mm)
	IS61LV10008-10TI	TSOP (Type II)
	IS61LV10008-10BI	36 mini BGA (9mm x 11mm)
12	IS61LV10008-12MI	48 mini BGA (9mm x 11mm)
	IS61LV10008-12TI	TSOP (Type II)
	IS61LV10008-12BI	36 mini BGA (9mm x 11mm)