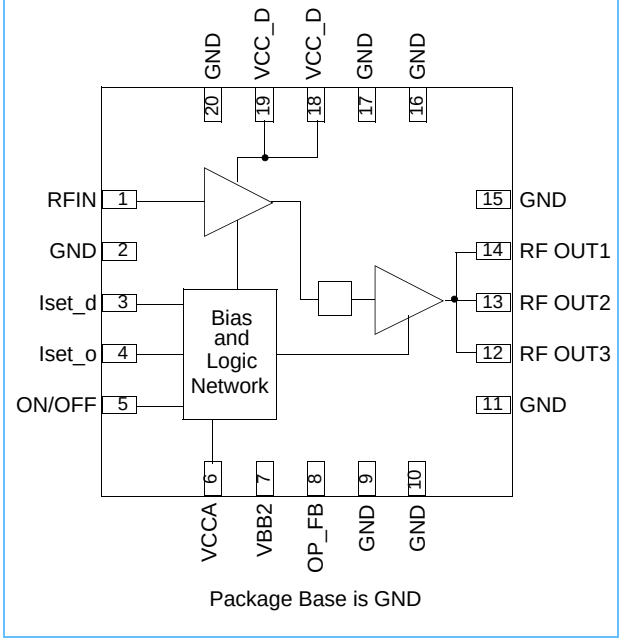
IBM3602022Q020
Datasheet
900 MHz AMPS/TDMA Power Amplifier

Features

- Highly integrated SiGe BiCMOS technology
- +29.5dBm output power for TDMA operation
- +31.5dBm output power for AMPS operation
- +16 dBm Low Power TDMA operation
- High power added efficiency
- Two-stage design with partial on-chip impedance matching
- On-chip VSWR protection
- Single power supply operation
- Low standby current: <2µA
- Built-in on/off function
- Small-outline, low profile package: QFN
- Low quiescent current

AMPS/TDMA Power Amplifier Block Diagram



Description

The IBM3602022Q020 900MHz AMPS/TDMA Power Amplifier (PA) is a single band, two-stage power amplifier using IBM's silicon germanium (SiGe) BiCMOS technology to yield maximum efficiency in wireless handset applications. The PA is optimized for both AMPS (U.S. Analog Mobile Phone System) and TDMA/IS-54 operations.

Advanced on-chip biasing technology ensures reliable performance in both operating modes. The power amplifier also has a power down function to extend battery life. On-chip VSWR protection allows the power amplifier to pass industry-standard ruggedness tests at full RF drive (+4dBm input) with a 10:1 load VSWR at Vcc = 5Vdc.

The 900MHz AMPS/TDMA PA is available in a 20-lead, 4mm low profile QFN package. The QFN package incorporates partial impedance matching for both the input and intermediate stages, with each requiring only one off-chip matching element. The output stage requires off-chip matching.

Ordering Information

To order samples of this product or a demonstration board, visit the IBM Microelectronics Division Web site at www.chips.ibm.com/support/howtobuy.html

Part Number	Product
IBM3602022Q020	900 MHZ AMPS/TDMA PA
IBM3602022EVBA	Evaluation Board

Note: The 900MHz AMPS/TDMA Power Amplifier is susceptible to damage from electrostatic discharge (ESD). Observe normal ESD precautions at all times when handling or using the device.

Electrical and Thermal Characteristics

Table 1. Absolute Maximum and Minimum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units	Mode
Supply voltage	Vsupply	--	3.5	5.0	Vdc	All
Standby current	--	--	--	2	µA	All
Mode control	Iset_d, Iset_o	--	--	5.0	Vdc	All
Input RF power	--	--	--	7	dBm	AMPS
Operating temperature	--	-30	--	+85	°C	All
Storage temperature	--	-65	--	+150	°C	All

Table 2. Logic Input Voltage Levels

Level	Minimum	Maximum	Units
Logic 0	0	0.6	Vdc
Logic 1	2	V_{CC}	Vdc

Table 3. AMPS Operating Characteristics (T_A = 25°C, V_{CC} = 3.5Vdc, CW, ON/OFF input = logic '0')

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Mode control	Iset_d, Iset_o	2.4	2.5	2.6	Vdc	AMPS mode
Frequency range	--	824	836.5	849	MHz	--
Gain	--	--	28.5	--	dB	--
Output power	--	--	31.5	--	dBm	--
PAE	--	50	--	--	%	--
Gain vs. Temperature	--	--	±1.0	--	dB	1
Stability	--	--	--	-60	dBc	2
Harmonics	--	--	-36	--	dBc	--
Input VSWR	--	--	2.1:1	--	--	--
Ruggedness VSWR	--	10:1	--	--	--	3

1. -30 to +85°C
2. Maximum spurs out-of-band load VSWR <5:1, in-band load VSWR <3:1
3. No damage with P_{in} = +4dBm, V_{CC} = 5Vdc

Table 4. High Power TDMA Operating Characteristics
(T_A = 25°C, V_{CC} = 3.5Vdc, NADC modulation, ON/OFF input = logic '0')

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Mode control	Iset_d, Iset_o	1.2	1.3	1.4	Vdc	IS-54 mode
Frequency range	--	824	836.5	849	MHz	--
Gain	--	28	30.5	31	dB	--
Gain vs. Temperature	--	--	±0.8	--	dB	1
Output power	--	--	29.5	--	dBm	--
Quiescent current	--	--	135	160	mA	--
PAE	--	40	--	--	%	--
ACPR	--	--	-29	-28	dBc	2
ALT1	--	--	-49	-48	dBc	3

1. -30 to +85°C
2. ±30 KHz
3. ±60KHz

Table 5. Low Power TDMA Operating Characteristics
(T_A = 25°C, V_{CC} = 3.5Vdc, F = 836.5 MHz, NADC modulation, ON/OFF input = logic '0')

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Mode control	Iset_d,Iset_o	2.4	2.5	2.6	Vdc	IS-54 mode
Frequency range	--	824	836.5	849	MHz	--
Gain	--	26	28.5	31	dB	--
Output power	--	--	16.0	--	dBm	--
Quiescent current	--	--	45	60	mA	--
PAE	--	8	--	--	%	--
Gain vs. Temperature	--	--	±1.0	--	dB	1
ACPR	--	--	-29	-28	dBc	2
ALT1	--	--	-49	-48	dBc	3

1. -30 to +85°C
2. ±30 kHz
3. ±60 kHz

Figure 1. Functional Block Diagram

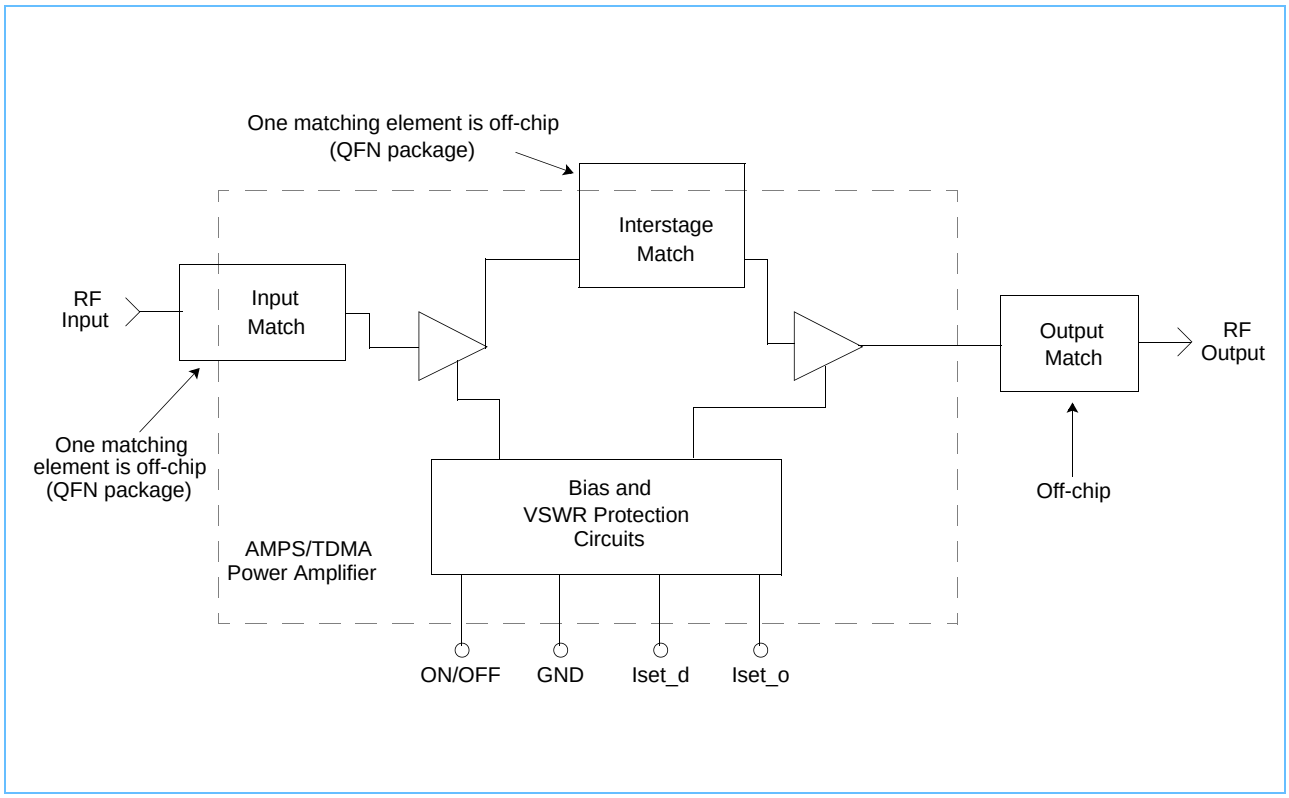
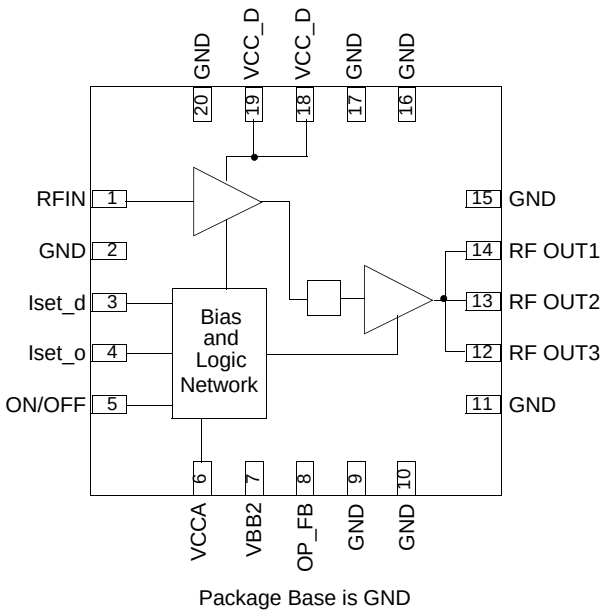


Table 6. Lead Description (QFN, 20-lead, 4mm x 4mm package)

Lead	Name	Type	Description
1	RF IN	RF	PA input
2	GND	--	No connection, may be connected to ground
3	Iset_d	Power	Resistor connected to ground or to MD_SEL to control driver (first) stage Icc
4	Iset_o	Power	Resistor connected to ground or to MD_SEL to control output (second) stage Icc
5	ON/OFF	Input	PA on/off; logic low turns PA on
6	VCCA	Power	DC supply for bias circuitry
7	VBB2	Power	Capacitor to ground for additional bypassing of output (second) stage
8	OP_FB	Power	Optional output feedback
9	GND	--	No connection required, grounding recommended
10	GND	--	No connection required, grounding recommended
11	GND	--	No connection required grounding recommended
12	RFOUT1/VCCO	Output	PA output; 1 of 3 / DC supply for final stage (VCCO)
13	RFOUT2/VCCO	Output	PA output; 2 of 3 / DC supply for final stage (VCCO)
14	RFOUT3/VCCO	Output	PA output; 3 of 3 / DC supply for final stage (VCCO)
15	GND	--	No connection required, grounding recommended
16	GND	--	No connection required, grounding recommended
17	GND	--	No connection required, grounding recommended
18	VCC_D	Power	DC supply for driver (first) stage; 1 of 2
19	VCC_D	Power	DC supply for driver (first) stage; 2 of 2
20	GND	--	No connection required, grounding recommended
paddle	GND	Power	Exposed paddle; DC and RF ground

Table 7. Pin Out



Function Description

DC supply voltages are fed to the power amplifier through VCCD, VCCA, and VCCO. The output amplifier stage is supplied through an RF choke via the RF OUT leads. VCCD supplies power to the driver stage, while VCCA supplies power to the biasing circuits. The Iset_o and Iset_d leads are used to control collector current (I_{CC}) in the output and driver amplifiers. The power amplifier can be configured to run in the AMPS or low-power TDMA modes when Iset_d and Iset_o are connected as shown in Figure 2 to create a single mode control input pin P5 or P6. To select an operating mode, connect an analog voltage supply to the control input pins P5 or P6. Set the mode voltage to the values listed in Tables 3,4 or 5 for the proper mode of operation. The ON/OFF lead controls power amplifier on/off switching. A high logic level turns the power amplifier off, which results in low standby current.

Figure 2. Demonstration Board Schematic

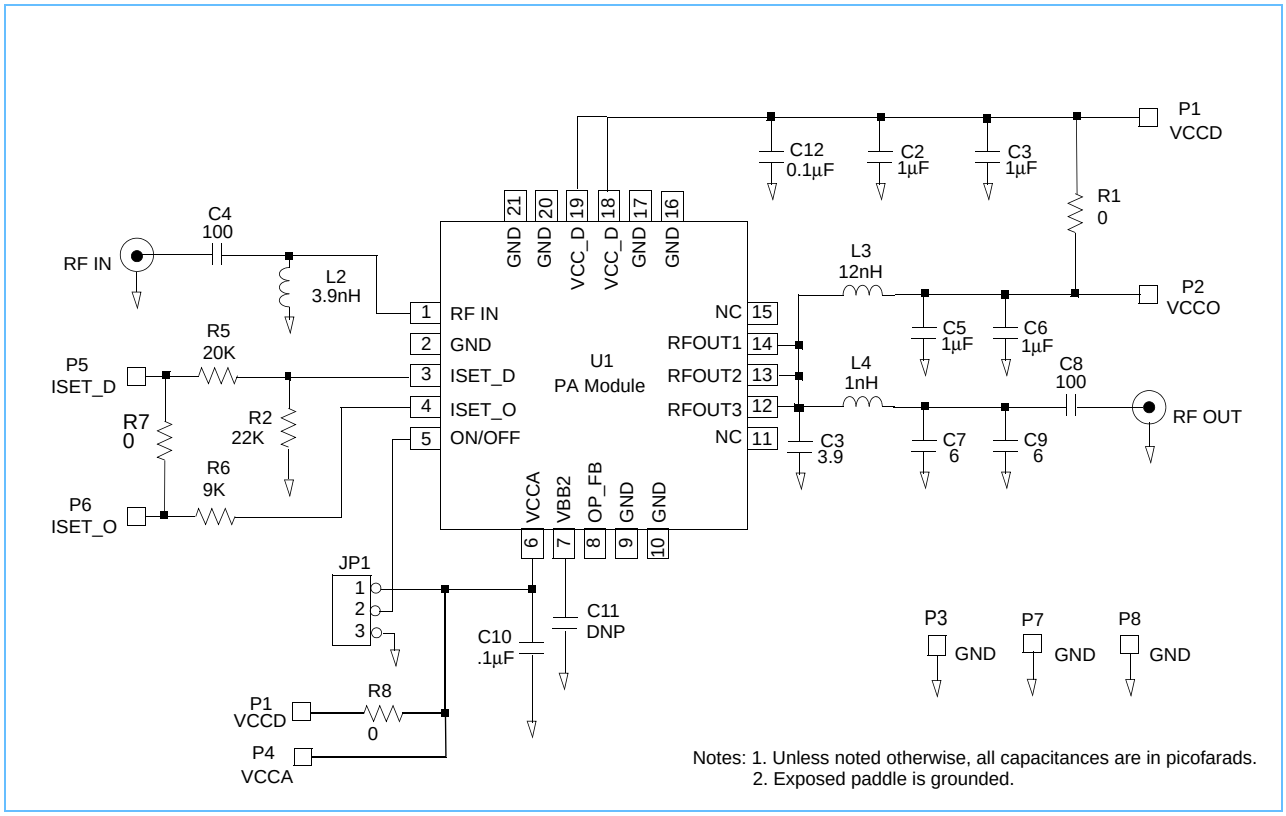
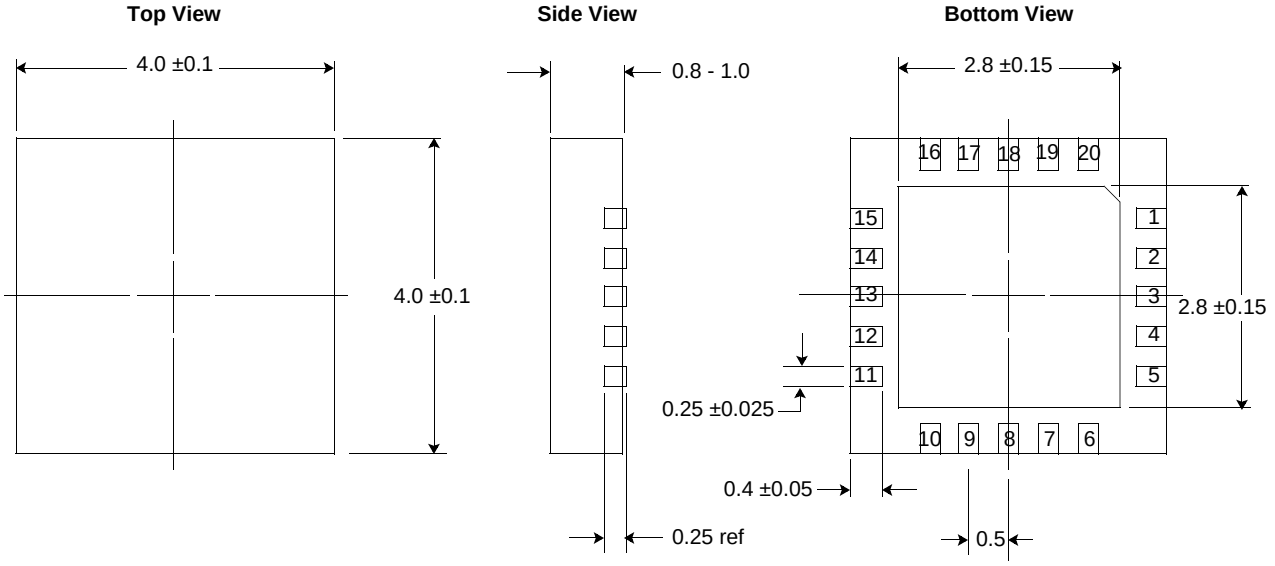
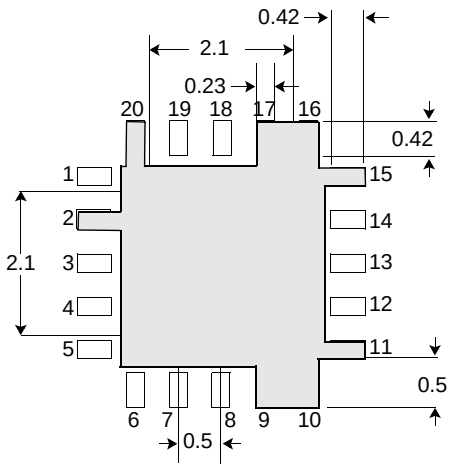


Figure 3. QFN Package Dimensions



Notes: Dimensions are in millimeters. Not to scale. Pin numbers are shown for reference.

Figure 4. PCB Pad Placement, QFN Package



Notes: Dimensions are in millimeters. Not to scale. Shaded area shows PCB pad. Pin numbers are shown for reference.

Document Revision Log

Revision Date	Contents of Modification
November 2, 2001	Advance release (00).
December 19, 2001	General release (01)

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