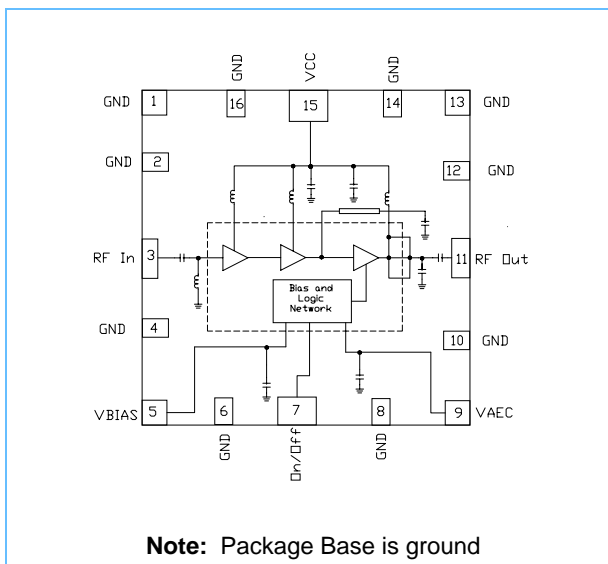


Features

- IS-95/PCS operation in 1850-1910 MHz band
- 50Ω Matched Module
- +28.5dBm output power
- Passes industry standard VSWR ruggedness test.
- 32% Power Added Efficiency (PAE)
- Single power supply (no reference voltage required)
- On-chip logic-controlled power shutdown
- Small-outline, low profile, 6mm x 6mm, 16-lead LGA module

1900MHz CDMA Power Amplifier Block Diagram



Description

The IBM3602017M016 CDMA Power Amplifier (PA) is a highly integrated module with a single band, three-stage device fabricated using IBM's Silicon Germanium (SiGe) BiCMOS technology for high efficiency in wireless handset applications. The power amplifier is optimized for Code Division Multiple Access (CDMA) operation in compliance with IS-95 standards

Advanced on-chip biasing technology enables optimum CDMA performance and eliminates the need for external reference voltages. An integrated power down function extends battery life. On-chip VSWR protection allows the 1900MHz CDMA PA to pass industry-standard ruggedness tests at full RF drive (+30dBm output) with load VSWR's exceeding 10:1 at $V_{CC} = 5V$.

The 1900MHz CDMA PA is available in a 16-lead, 6mm x 6mm, low profile module. The use of internal impedance matching within the module results in optimal operating characteristics with a small footprint.

Ordering Information

To order samples of the 1900MHz CDMA PA or a demonstration board, contact an IBM sales representative or distributor. Regional contact information is located on the IBM Microelectronics Division website at:

www.chips.ibm.com/support/howtobuy.html

Part Number	Description	Packaging
IBM3602017M016	1900MHz CDMA PA	6x6mm LGA
IBM2017EVBA	1900MHz CDMA PA Demonstration Board	PCB assembly

Note: The Power Amplifier is susceptible to damage from electrostatic discharge (ESD). Observe normal ESD precautions at all times when handling or using the device.

Electrical and Thermal Characteristics

Table 1. Absolute Minimum and Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Supply voltage	V _{CC}	2.9	5.0	Vdc	--
Standby current	--	--	2.0	μA	1
RF input power	--	--	+5	dBm	--
Collector-emitter breakdown (open)	BV _{ceo}	5.0	--	Vdc	--
PA on/off control	ON/OFF	-0.6	3.6	Vdc	--
Analog Efficiency Control	V _{aec}	--	4.0	Vdc	--
Operating temperature	--	-20	+85	°C	--
Storage temperature	--	-65	+150	°C	--

Notes:

1) VAEC set to 0V.

Table 2. RF Specifications, Standby Mode

Note: All measurements taken using the IBM2017EVBA Demonstration Board under IS-95 reverse link modulation with V_{CC} = 3.4Vdc; T_A = 25°C; ON/OFF input = logic '0', VAEC=0V

Parameter	Minimum	Typical	Maximum	Units
Frequency range	1850	1880	1910	MHz
Gain	--	--	-30	dB
Leakage current	--	--	2.0	μA

Table 3. RF Specifications, CDMA High Power Mode

Note: All measurements taken using the IBM2017EVBA Demonstration Board under IS-95 reverse link modulation with V_{CC} = 3.4Vdc; T_A = 25°C; ON/OFF input = logic '0'

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Analog efficiency control	V _{aec}	--	0.9	--	Vdc	1
Frequency range	--	1850	1880	1910	MHz	--
Gain	--	--	29	--	dB	--
Gain vs. temperature	--	-2	--	+2	dB	2
Noise figure	--	4.0	4.5	5.5	dB	--
Output power	--	--	+28.5	--	dBm	--
Quiescent current	I _{cq}	--	85	95	mA	--
PAE	--	--	32	--	%	--
ACPR	--	-45	--	--	dBc	3
ACPR, temperature/voltage	--	--	-43	--	dBc	3
ALT1	--	--	-51	--	dBc	4
Stability	--	--	-60	--	dBc	5
Harmonics	--	--	-30	--	dBc	--
Input VSWR	--	--	--	2:1	--	--
Ruggedness VSWR	--	10:1	--	--	--	6

1. I_{cq} = 85mA. Typical combined quiescent of stages 1, 2, and 3.
2. -20 to +85°C
3. ±1.25 MHz
4. ±1.98 MHz
5. Maximum spurs with out-of-band load VSWR < 5:1, in-band load VSWR < 3:1
6. No damage with P_{out} = +30dBm, V_{CC} = 5Vdc

Table 4. RF Specifications, CDMA Low Power Mode

Note: All measurements taken using the IBM2017EVBA Demonstration Board under IS-95 reverse link modulation with $V_{CC} = 3.4Vdc$; $T_A = 25^{\circ}C$; ON/OFF input = logic '0')

(@

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Analog efficiency control	Vaec	--	1.6	--	Vdc	1
Frequency range	--	1850	1880	1910	MHz	
Gain	--	--	25	--	dB	
Gain vs. temperature	--	-2	--	+2	dB	2
Output power	--	--	+12	--	dBm	
Quiescent current	Icq	--	70	80	mA	
PAE	--	--	4	--	%	
ACPR	--	-46	--	--	dBc	3
ALT1	--	--	-58	--	dBc	4
Stability	--	--	-60	--	dBc	5
Harmonics	--	--	-30	--	dBc	
Input VSWR	--	--	--	2:1	--	
Ruggedness VSWR	--	10:1	--	--	--	6

1. Icq =70mA. Typical combined quiescent of stages 1, 2, and 3.
2. -20 to +85°C
3. ±1.25 MHz
4. ±1.98 MHz
5. Maximum spurs with out-of-band load VSWR < 5:1, in-band load VSWR < 3:1
6. No damage with $P_{out} = +30dBm$, $V_{CC} = 5Vdc$

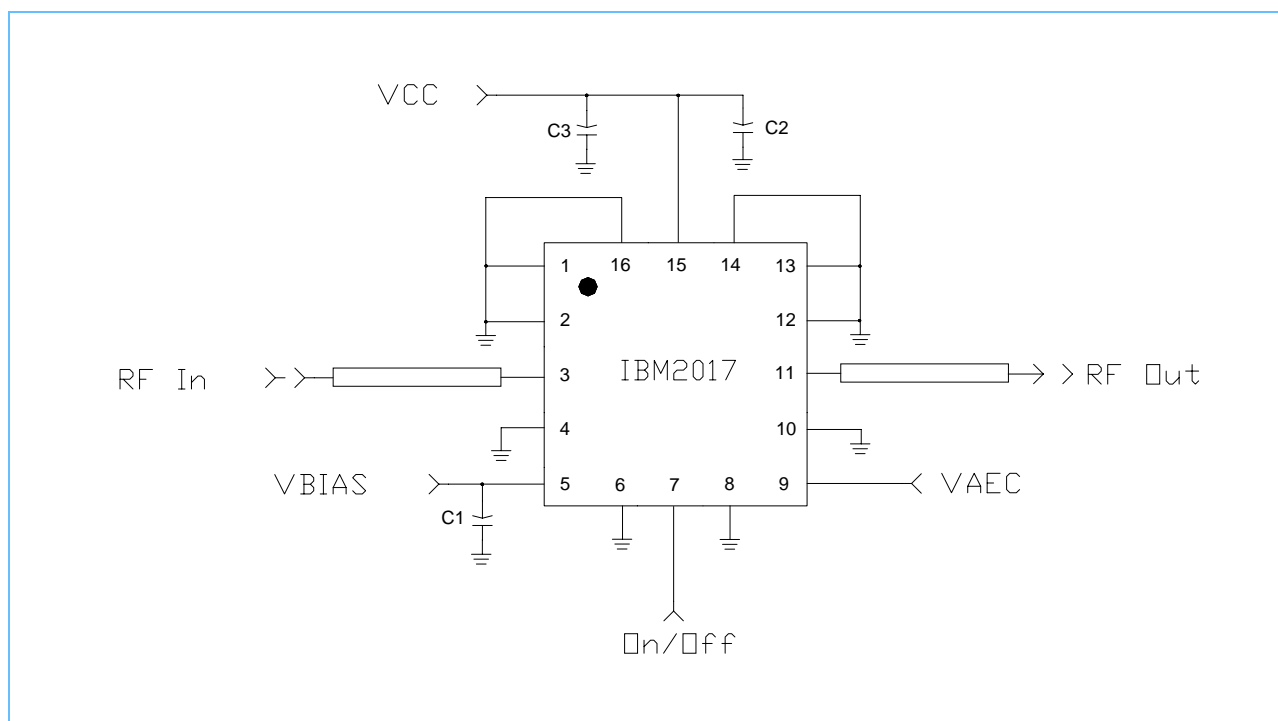
Table 5. Lead Description

Lead	Name	Type	Description
1	GND	--	Ground
2	GND	--	Ground
3	RF_IN	Input	RF Input
4	GND	--	Ground
5	VBIAS	Input	Bias and Logic Network Bias
6	GND	--	Ground
7	ON / OFF	Input	Power Amplifier ON / OFF Control
8	GND	--	Ground
9	VAEC	Input	Gain control
10	GND	--	Ground
11	RF_OUT	Output	RF Output
12	GND	--	Ground
13	GND	--	Ground
14	GND	--	Ground
15	VCC	Input	Collector Bias, Stages 1,2,3
16	GND	--	Ground

Table 6. Logic Input Voltage Levels

Level	Minimum	Maximum	Units
Logic 0	0	0.6	Vdc
Logic 1	2	V_{CC}	Vdc

Figure 1. Demonstration Board Schematic



Functional Description

Figure 1 shows the 1900MHz CDMA PA module as configured with the IBM2017EVBA Power Amplifier Demonstration Board. Pins VCC and VBIAS supply DC power to the PA. A nominal voltage of 3.4Vdc biases the PA and the Bias and Logic Network. The only other components required are de-coupling capacitors C1, C2 and C3.

The Demonstration Board contains the fully integrated IBM3602017M016 1900MHz CDMA PA module which provides all required power amplifier matching. No other components are required.

A positive voltage applied to the analog efficiency control pin, "VAEC", sets the PA's quiescent current and determines ACPR vs. output power. Applying a logic '1' level (2-3.6V) to the ON/OFF pin places the PA into a power down state that draws less than 2 μ A of current. VAEC should be set to 0V during "OFF" mode.

Figure 2. Module Package Dimensions

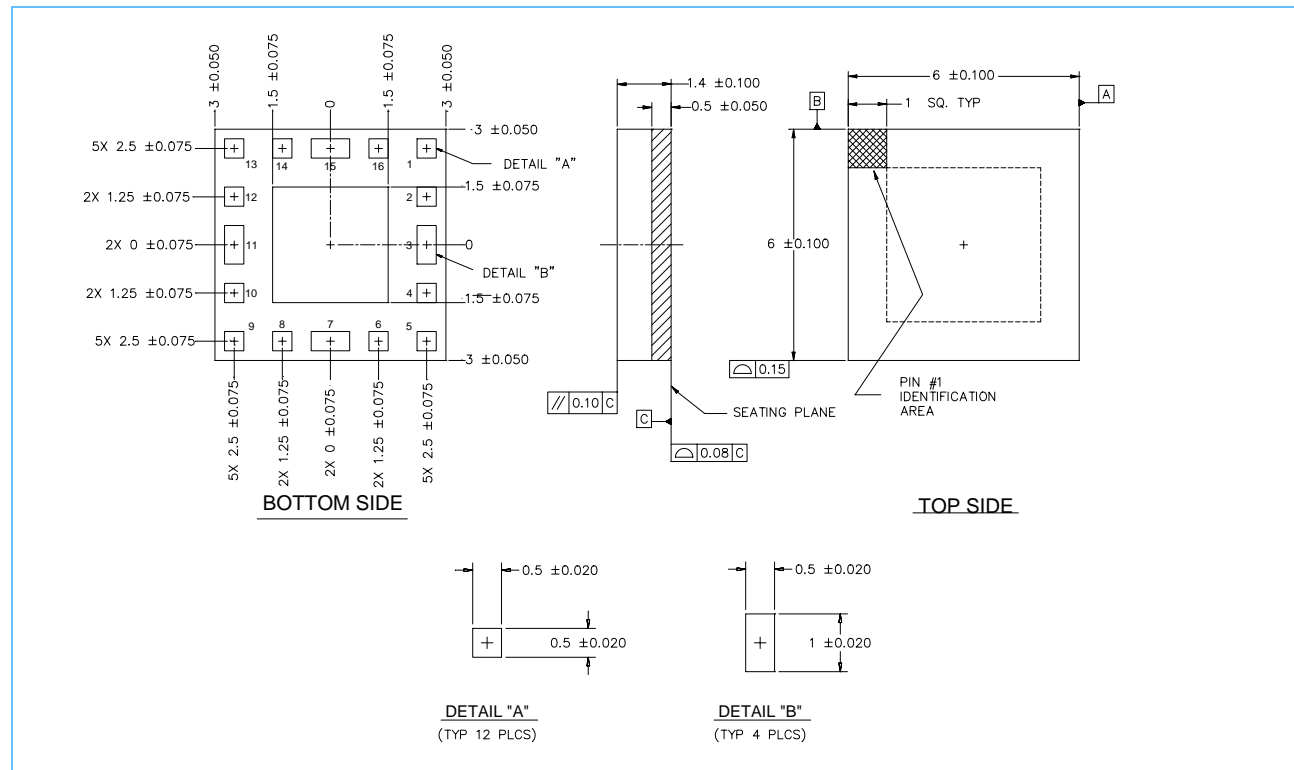
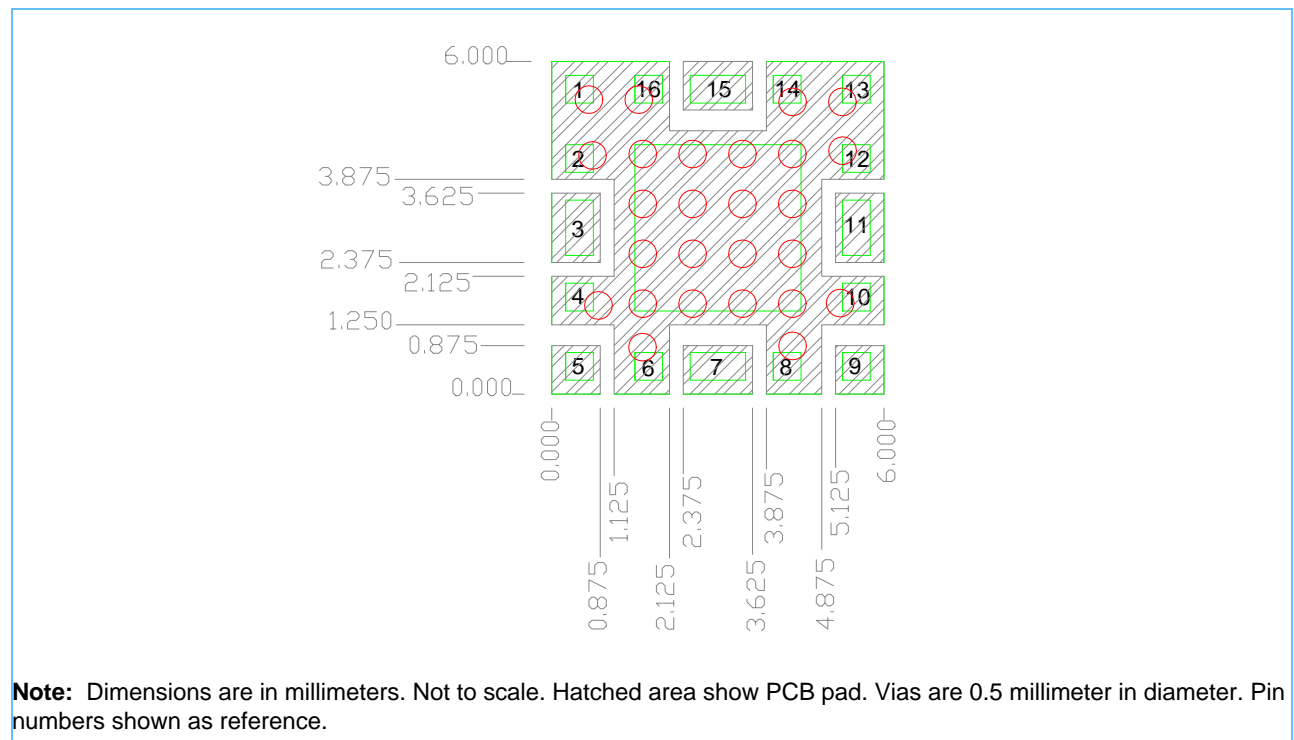
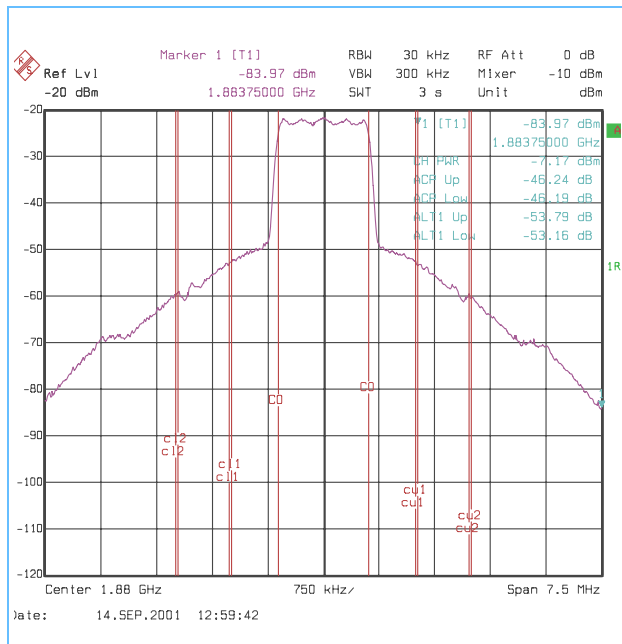


Figure 3. PCB Pad Placement

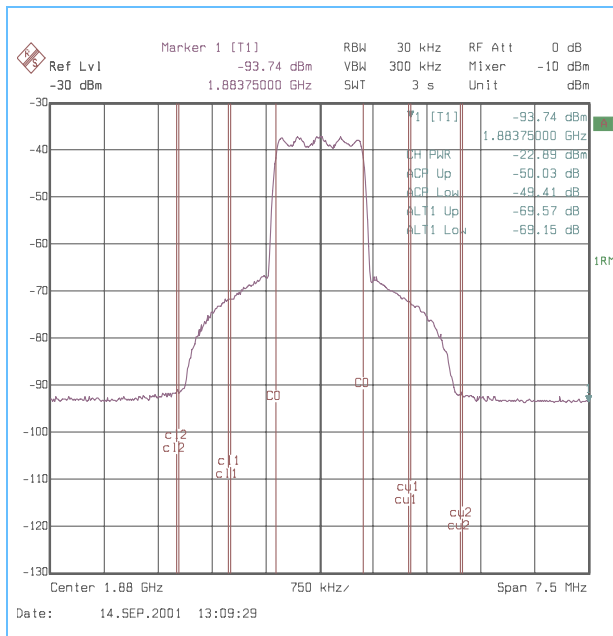


Appendix: Gain and Power Plots

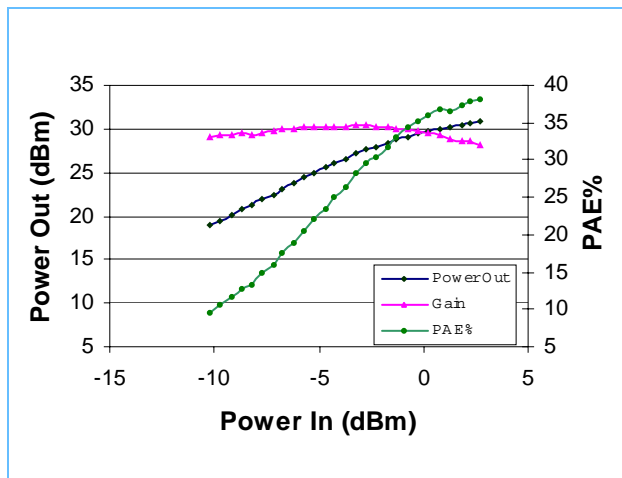
ACPR, High Power Mode



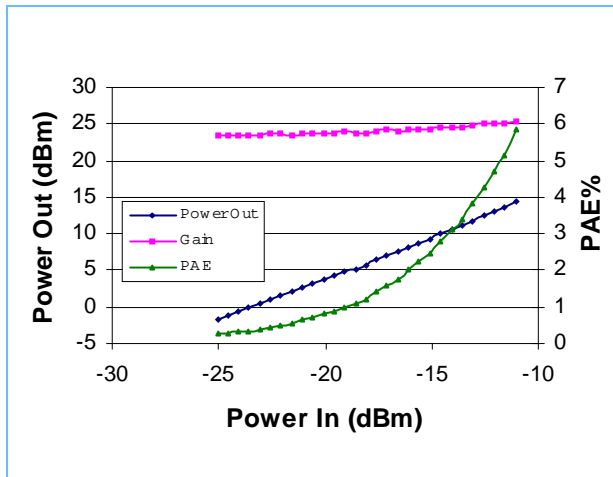
ACPR, Low Power Mode



P_{out} , PAE, Gain vs. P_{in} , High Power Mode



P_{out} , PAE, Gain vs. P_{in} , Low Power Mode





Document Revision Log

Revision Date	Contents of Modification
August 7, 2001	Initial release (00).
November 1, 2001	Revised (01), Kermit_V3
February 21, 2002	Revised (02), Pepe_2PO

Note: This document contains information on products in the design, sampling and/or initial production phases of development. This is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

© Copyright International Business Machines Corp. 2002
All Rights Reserved
Printed in the United States of America. February 2002

The following are trademarks of International Business Machines Corporation in the United States, or other countries, or both.

IBM IBM Logo

Other company, product and service names may be trademarks or service marks of others.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in implantation or other life support applications where malfunction may result in injury or death to persons. The information contained in this document does not affect or change IBM product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All information contained in this document was obtained in specific environments, and is presented as an illustration. The results obtained in other operating environments may vary.

While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will IBM be liable for damages arising directly or indirectly from any use of the information contained in this document.

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction NY 12533-6351

The IBM home page can be found at <http://www.ibm.com>

The IBM Microelectronics Division home page can be found at <http://www.chips.ibm.com>

pa2017_ds_022102.fm.02
February 21, 2002