IC80LV52
IC80LV32

CMOS SINGLE CHIP LOW VOLTAGE 8-BIT MICROCONTROLLER

FEATURES

- 80C51 based architecture
- 8K x 8 ROM (IC80LV52 only)
- 256 x 8 RAM
- Three 16-bit Timer/Counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- Memory addressing capability
  – 64K ROM and 64K RAM
- Program memory lock
  – Encrypted verify (32 bytes)
  – Lock bits (2)
- Power save modes:
  – Idle and power-down
- Eight interrupt sources
- Most instructions execute in 0.5 μs
- CMOS and TTL compatible
- Maximum speed: 24 MHz @ Vcc = 3.3V
- Packages available:
  – 40-pin DIP
  – 44-pin PLCC
  – 44-pin PQFP

GENERAL DESCRIPTION

The *ICSI* IC80LV52 and IC80LV32 are high-performance microcontrollers fabricated using high-density CMOS technology. The CMOS IC80LV52/32 is functionally compatible with the industry standard 8052/32 microcontrollers.

The IC80LV52/32 is designed with 8K x 8 ROM (IC80LV52 only); 256 x 8 RAM; 32 programmable I/O lines; a serial I/O port for either multiprocessor communications, I/O expansion or full duplex UART; three 16-bit timer/counters; an eight-source, two-priority-level, nested interrupt structure; and an on-chip oscillator and clock circuit. The IC80LV52/32 can be expanded using standard TTL compatible memory.

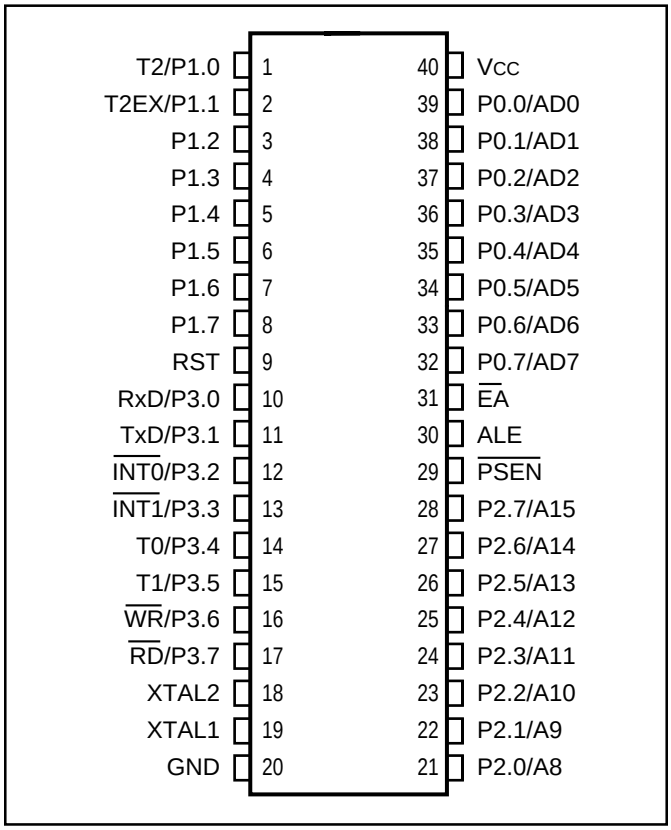

Figure 1. IC80LV52/32 Pin Configuration: 40-pin DIP

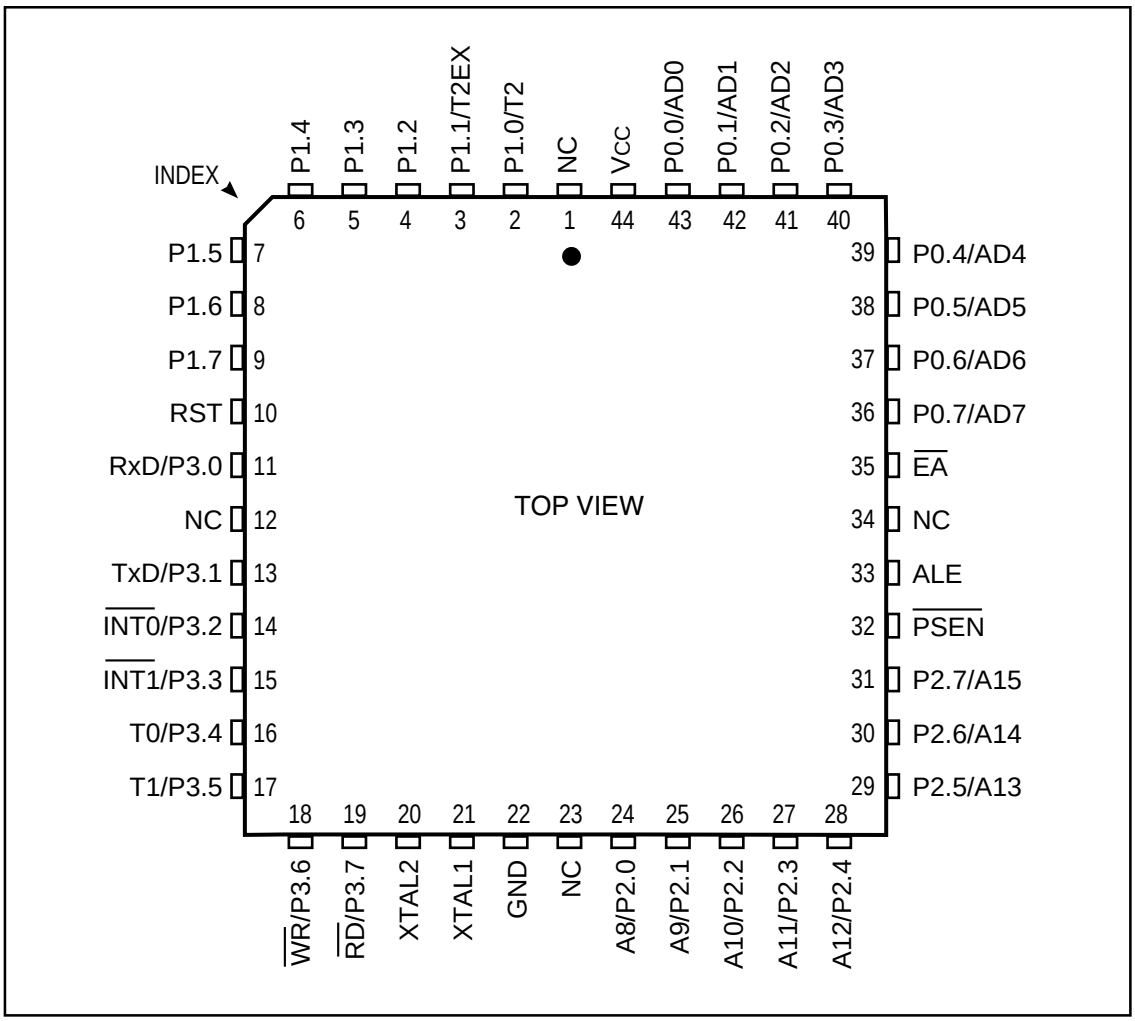

Figure 2. IC80LV52/32 Pin Configuration: 44-pin PLCC

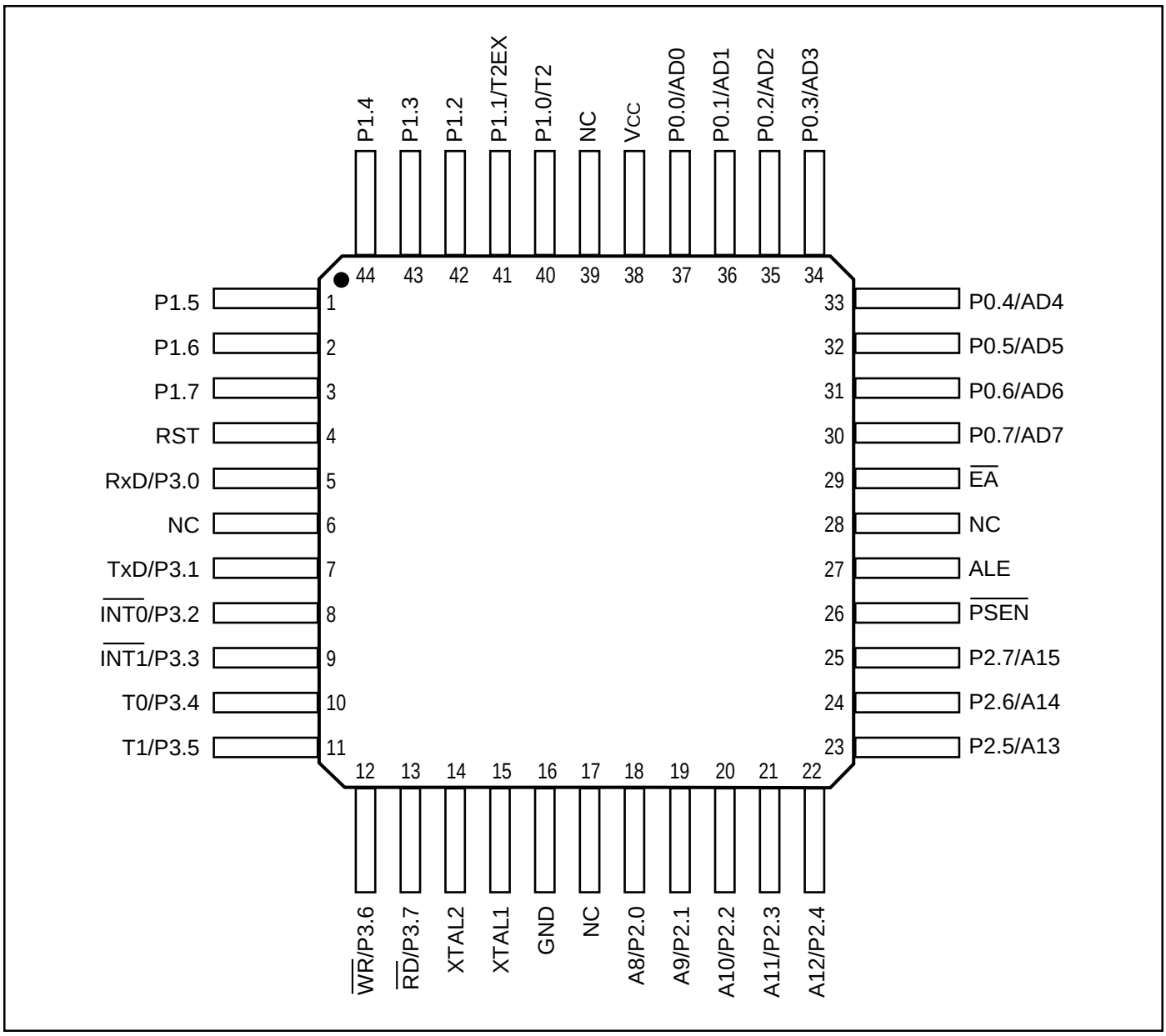

Figure 3. IC80LV52/32 Pin Configuration: 44-pin PQFP

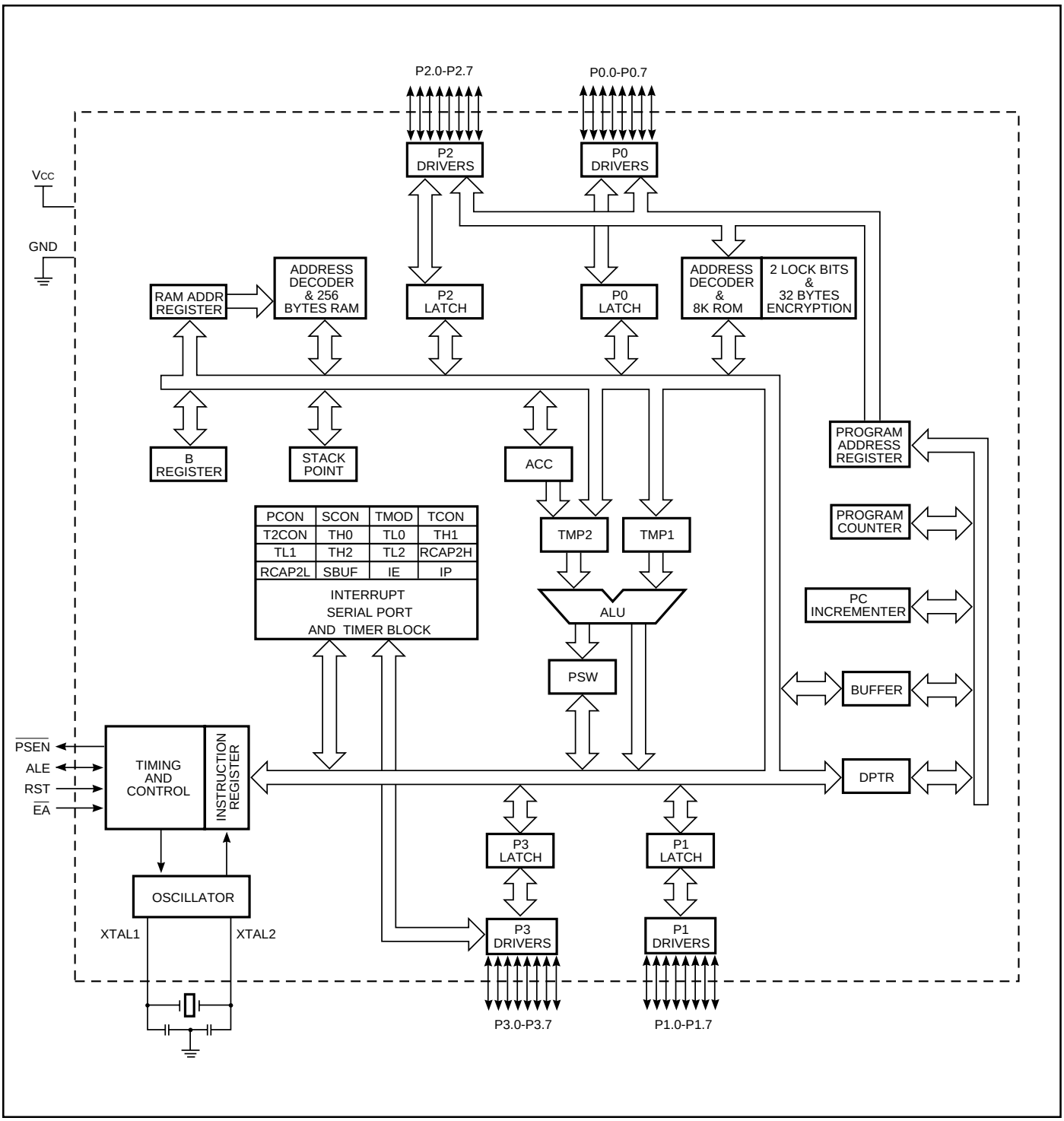

Figure 4. IC80LV52/32 Block Diagram

Table 1. Detailed Pin Description

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
ALE	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an address to the external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{EA}$	31	35	29	I	**External Access enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to FFFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH.
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0:** Port 0 is an 8-bit open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pullups when emitting 1s.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). The Port 1 output buffers can sink/source four TTL inputs. Port 1 also receives the low-order address byte during ROM verification.
	1 2	2 3	40 41	I I	**T2(P1.0):** Timer/Counter 2 external count input. **T2EX(P1.1):** Timer/Counter 2 trigger input.
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that used 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ Ri [i = 0, 1]), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order bits and some control signals during ROM verification.

Table 1. Detailed Pin Description *(continued)*

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). Port 3 also serves the special features of the IC80LV52/32, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port.
	11	13	7	O	**TxD (P3.1):** Serial output port.
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0.
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1.
	14	16	10	I	**T0 (P3.4):** Timer 0 external input.
	15	17	11	I	**T1 (P3.5):** Timer 1 external input.
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe.
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe.
$\overline{\text{PSEN}}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal MOS resistor to GND permits a power-on reset using only an external capacitor connected to Vcc.
XTAL 1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL 2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.
GND	20	22	16	I	**Ground:** 0V reference.
Vcc	40	44	38	I	**Power Supply:** This is the power supply voltage for operation.

OPERATING DESCRIPTION

The detail description of the IC80LV52/32 included in this description are:

- **Memory Map and Registers**
- **Timer/Counters**
- **Serial Interface**
- **Interrupt System**
- **Other Information**

The detail information desription of the IC80LV52/32 refer to IC80C52/32 data sheet

OTHER INFORMATION

Reset

The reset input is the RST pin, which is the input to a Schmitt Trigger.

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), *while the oscillator is running*. The CPU responds by generating an internal reset, with the timing shown in Figure 6.

The external reset signal is asynchronous to the internal clock. The RST pin is sampled during State 5 Phase 2 of every machine cycle. The port pins will maintain their current activities for 19 oscillator periods after a logic 1 has been sampled at the RST pin; that is, for 19 to 31 oscillator periods after the external reset signal has been applied to the RST pin.

The internal reset algorithm writes 0s to all the SFRs except the port latches, the Stack Pointer, and SBUF. The port latches are initialized to FFH, the Stack Pointer to 07H, and SBUF is indeterminate. Table 2 lists the SFRs and their reset values.

Then internal RAM is not affected by reset. On power-up the RAM content is indeterminate.

Table 2. Reset Values of the SFR's

SFR Name	Reset Value
PC	0000H
ACC	00H
B	00H
PSW	00H
SP	07H
DPTR	0000H
P0-P3	FFH
IP	XX000000B
IE	0X000000B
TMOD	00H
TCON	00H
T2CON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
TH2	00H
TL2	00H
RCAP2H	00H
RCAP2L	00H
SCON	00H
SBUF	Indeterminate
PCON	0XXX0000B

Power-on Reset

An automatic reset can be obtained when Vcc goes through a 10μF capacitor and GND through an 8.2K resistor, providing the Vcc rise time does not exceed 1 msec and the oscillator start-up time does not exceed 10 msec. This power-on reset circuit is shown in Figure 5. The CMOS devices do not require the 8.2K pulldown resistor, although its presence does no harm.

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the value of the capacitor and the rate at which it charges. To ensure a good reset, the RST pin must be high long enough to allow the oscillator time to start-up (normally a few msec) plus two machine cycles.

Note that the port pins will be in a random state until the oscillator has start and the internal reset algorithm has written 1s to them.

With this circuit, reducing Vcc quickly to 0 causes the RST pin voltage to momentarily fall below 0V. However, this voltage is internally limited, and will not harm the device.

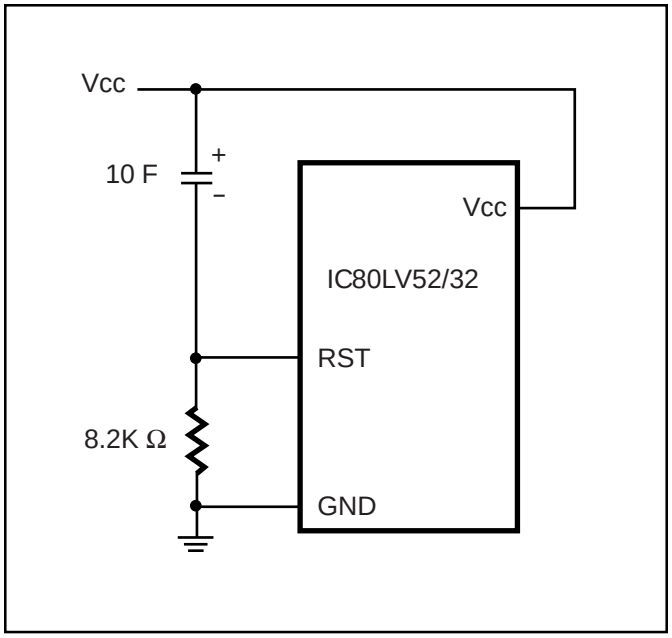

Figure 5. Power-On Reset Circuit

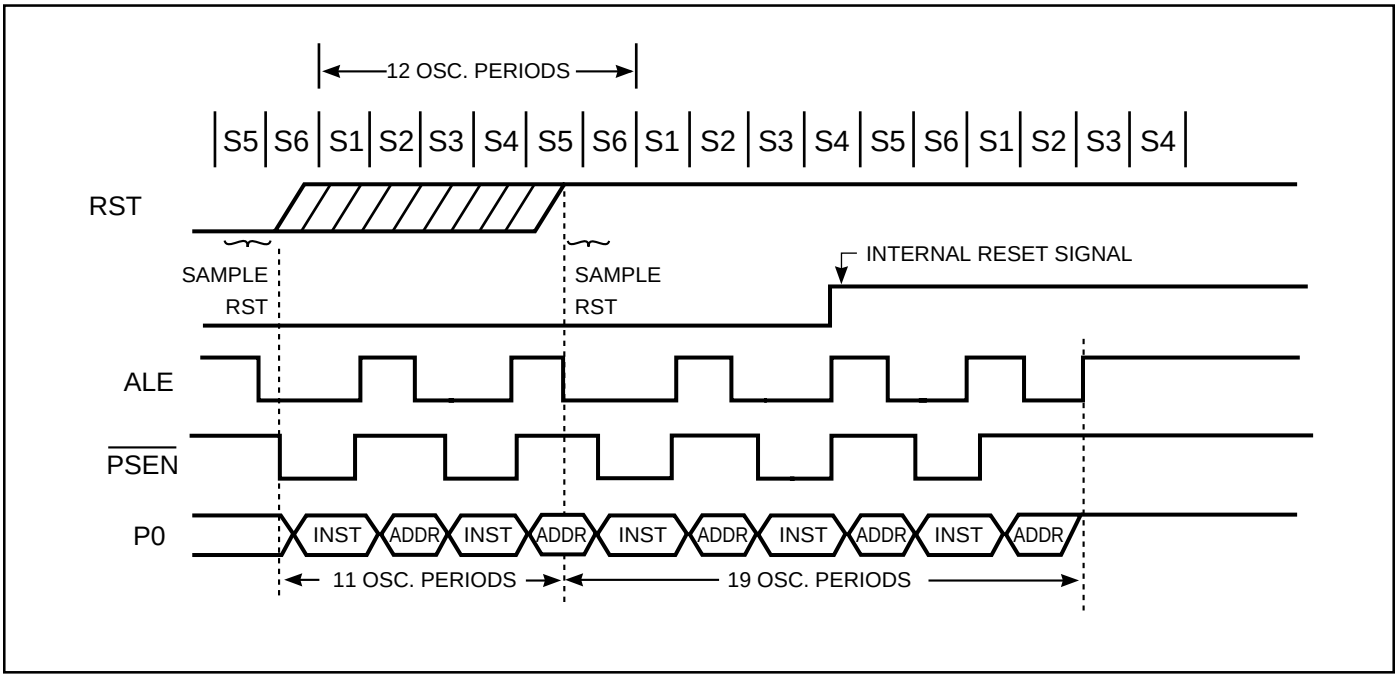

Figure 6. Reset Timing

Power-Saving Modes of Operation

The IC80LV52/32 has two power-reducing modes. Idle and Power-down. The input through which backup power is supplied during these operations is Vcc. Figure 7 shows the internal circuitry which implements these features. In the Idle mode (IDL = 1), the oscillator continues to run and the Interrupt, Serial Port, and Timer blocks continue to be clocked, but the clock signal is gated off to the CPU. In Power-down (PD = 1), the oscillator is frozen. The Idle and Power-down modes are activated by setting bits in Special Function Register PCON.

Idle Mode

An instruction that sets PCON.0 is the last instruction executed before the Idle mode begins. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the Interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

The flag bits GF0 and GF1 can be used to indicate whether an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset must be held active for only two machine cycles (24 oscillator periods) to complete the reset.

The signal at the RST pin clears the IDL bit directly and asynchronously. At this time, the CPU resumes program execution from where it left off; that is, at the instruction following the one that invoked the Idle Mode. As shown in Figure 22, two or three machine cycles of program execution may take place before the internal reset algorithm takes control. On-chip hardware inhibits access to the internal RAM during his time, but access to the port pins is not inhibited. To eliminate the possibility of unexpected outputs at the port pins, the instruction following the one that invokes Idle should not write to a port pin or to external data RAM.

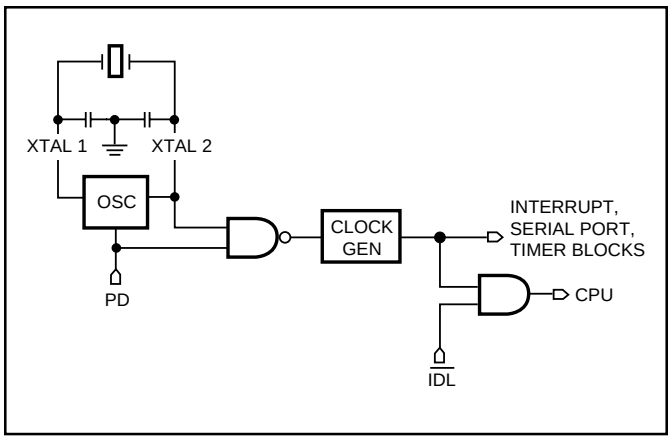

Figure 7. Idle and Power-Down Hardware

Power-down Mode

An instruction that sets PCON.1 is the last instruction executed before Power-down mode begins. In the Power-down mode, the on-chip oscillator stops. With the clock frozen, all functions are stopped, but the on-chip RAM and Special function Registers are held. The port pins output the values held by their respective SFRs. ALE and $\overline{\text{PSEN}}$ output lows.

In the Power-down mode of operation, Vcc can be reduced to as low as 2V. However, Vcc must not be reduced before the Power-down mode is invoked, and Vcc must be restored to its normal operating level before the Power-down mode is terminated. The reset that terminates Power-down also frees the oscillator. The reset should not be activated before Vcc is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (normally less than 10 msec).

The only exit from power-down is a hardware reset. Reset redefines all the SFRs but does not change the on-chip RAM.

Table 3. Status of the External Pins During Idle and Power-down Modes.

Mode	Memory	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

On-Chip Oscillators

The on-chip oscillator circuitry of the IC80LV52/32 is a single stage linear inverter, intended for use as a crystal-controlled, positive reactance oscillator (Figure 8). In this application the crystal is operated in its fundamental response mode as an inductive reactance in parallel resonance with capacitance external to the crystal (Figure 8). Examples of how to drive the clock with external oscillator are shown in Figure 9.

The crystal specifications and capacitance values (C1 and C2 in Figure 8) are not critical. 20 pF to 30 pF can be used in these positions at a12 MHz to 24 MHz frequency with good quality crystals. A ceramic resonator can be used in place of the crystal in cost-sensitive applications. When a ceramic resonator is used, C1 and C2 are normally selected to be of somewhat higher values. The manufacturer of the ceramic resonator should be consulted for recommendation on the values of these capacitors.

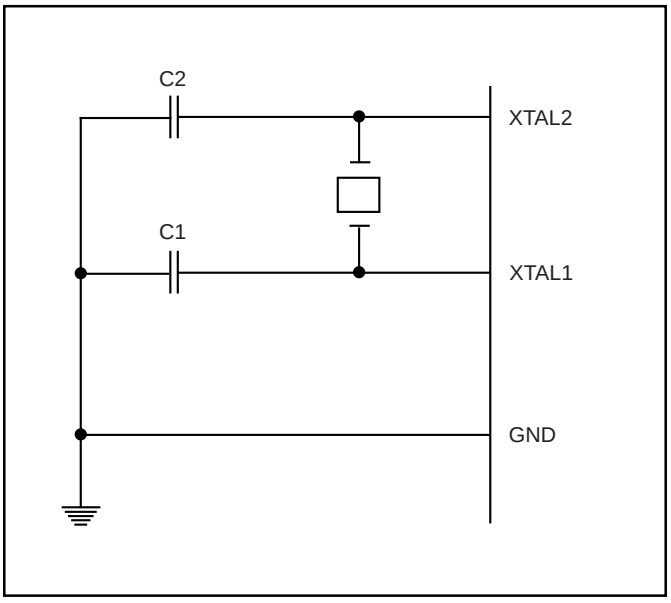

Figure 8. Oscillator Connections

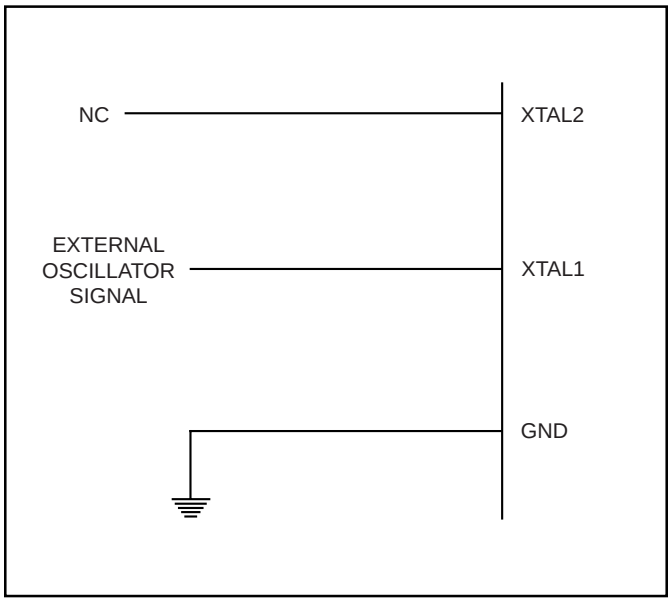

Figure 9. External Clock Drive Configuration

Table 4. Recommended Value for C1, C2, R

	Frequency Range	
	4 MHz-24 MHz	30 MHz-40 MHz
C1	20 pF-30 pF	–
C2	20 pF-30 pF	–
R	Not Apply	–

ROM Verification

The address of the program memory location to be read is applied to Port 1 and pins P2.4-P2.0. The other pins should be held at the “Verify” level are indicated in Figure 10. The contents of the addressed locations exits on Port 0. External pullups are required on Port 0 for this operation. Figure 10 shows the setup to verify the program memory.

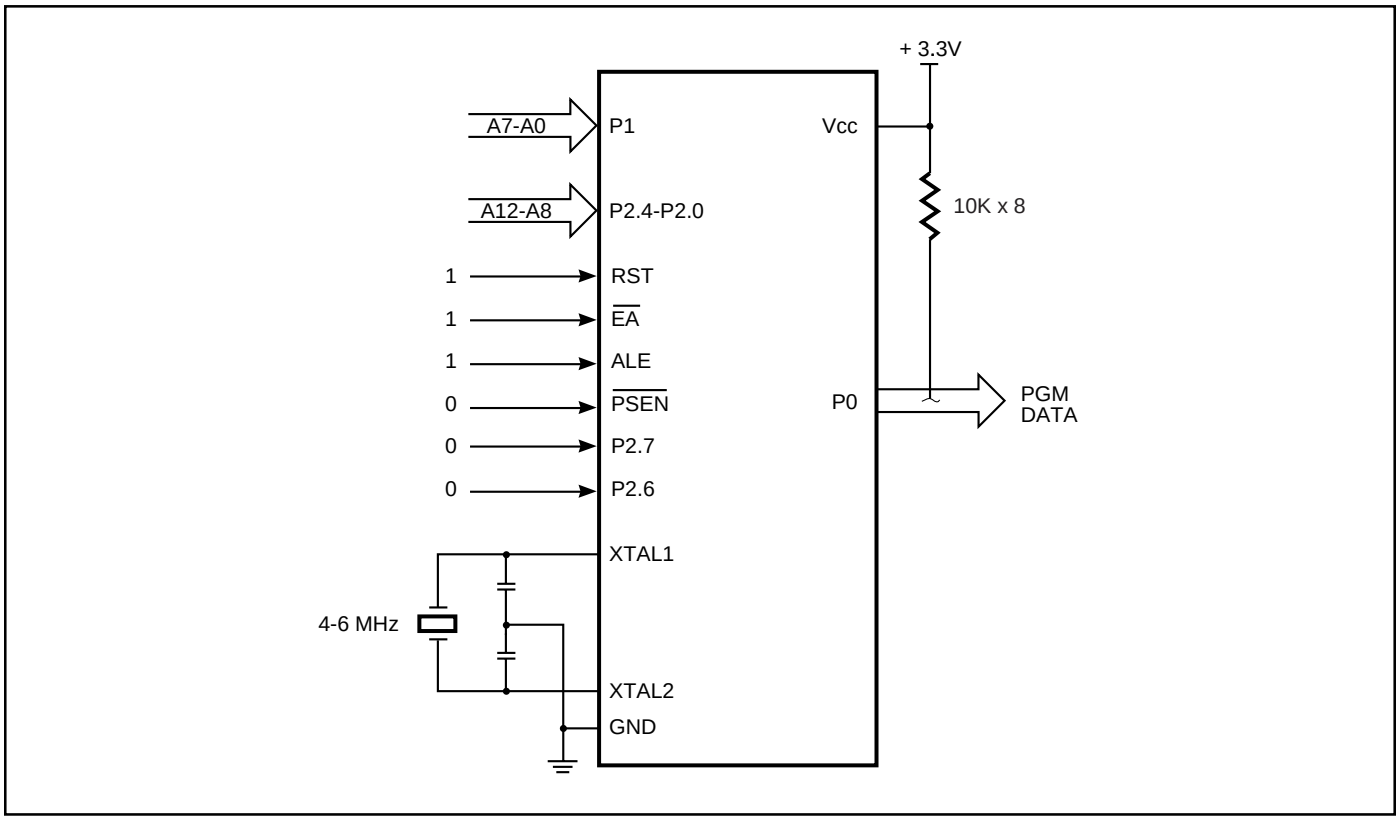

Figure 10. ROM Verification

ROM Lock System

The program lock system, when programmed, protects the ROM code against software piracy. The IC80LV52/32 has a two-level program lock system (see Table 5) and a 32-byte encryption table. No matter what lock bit is, the user submits the encryption table with his or her code in verify ROM mode. Both the lock-bit and encryption array programmed by the factory.

Encryption Array

Within the ROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during verify, five address lines are used to select a byte of the Encryption Array.This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (> 32 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason, all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value.

Table 5. Program Lock Bits

	LB1	LB2	Protection Type
1	U	U	No Program Lock Features enabled. (Code verify will still be encrypted by the Encryption Array if Programmed)
2	P	U	MOVC instructions executed from external program memory are diabled form fetching code bytes from internal memory, EA is sampled and latched on Reset.
3	P	P	Same as 2, also ROM verify is disabled.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND(2)	–2.0 to +7.0	V
T_{BIAS}	Temperature Under Bias(3)	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +125	°C
P_T	Power Dissipation	1.5	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods less than 20 ns. Maximum DC voltage on output pins is Vcc + 0.5V which may overshoot to Vcc + 2.0V for periods less than 20 ns.
3. Operating temperature is for commercial products only defined by this specification.

OPERATING RANGE(1)

Range	Ambient Temperature	Vcc	Oscillator Frequency
Commercial	0°C to +70°C	3.3V ± 10%	3.5 to 24 MHz

Note:
1. Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(T_A = 0°C to 70°C; Vcc = 3.3V ± 10%; GND = 0V)

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{IL}	Input low voltage (All except $\overline{EA}$)		–0.5	0.2Vcc + 0.1	V
$V_{IL}1$	Input low voltage ($\overline{EA}$)		–0.5	0.2Vcc + 0.1	V
V_{IH}	Input high voltage (All except XTAL 1, RST)		0.2Vcc + 0.9	Vcc + 0.5	V
$V_{IH}1$	Input high voltage (XTAL 1)		0.7Vcc	Vcc + 0.5	V
$V_{SCH}+$	RST positive schmitt-trigger threshold voltage		0.7Vcc	Vcc + 0.5	V
$V_{SCH}–$	RST negative schmitt-trigger threshold voltage		0	0.3Vcc	V
Vol(1)	Output low voltage (Ports 1, 2, 3)	I_{OL} = 1.6 mA	—	0.45	V
$V_{OL}1$(1)	Output low voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA	—	0.45	V
V_{OH}	Output high voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = –20 µA	Vcc–0.9	—	V
$V_{OH}1$	Output high voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OH} = –800 µA	Vcc–0.9	—	V
I_{IL}	Logical 0 input current (Ports 1, 2, 3)	V_{IN} = 0.45V	—	–50	µA
I_{LI}	Input leakage current (Port 0)	0.45V < V_{IN} < Vcc	–5	5	µA
I_{TL}	Logical 1-to-0 transition current (Ports 1, 2, 3)	V_{IN} = 2.0V	—	–450	µA
R_{RST}	RST pulldown resister		150	450	KΩ

Note:

1. Under steady state (non-transient) conditions, Iol must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
Pins are not guaranteed to sink greater than the listed test conditions.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Max	Unit
Icc	Power supply current[1]	Vcc = 3.3V			
	Active mode	12 MHz	—	15	mA
		24 MHz	—	24	mA
	Idle mode	12 MHz	—	4	mA
		24 MHz	—	8	mA
	Power-down mode	Vcc = 3.3V	—	50	µA

Note:
1. See Figures 11, 12, 13, and 14 for Icc test conditiions.

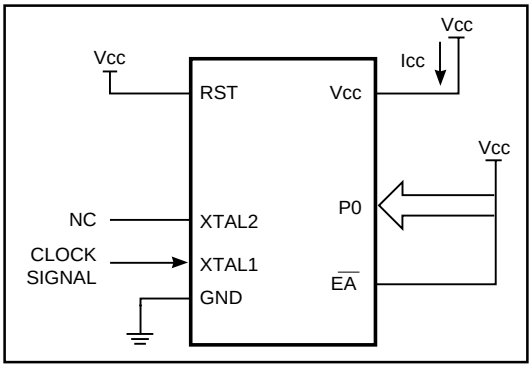

Figure 11. Active Mode

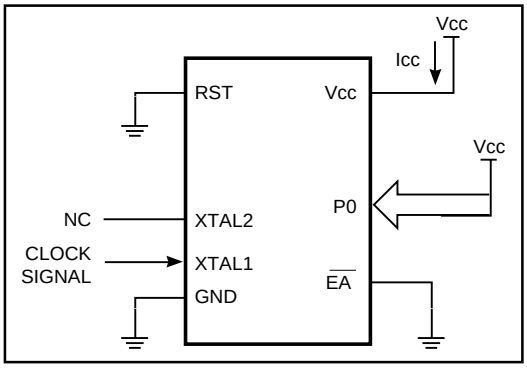

Figure 12. Idle Mode

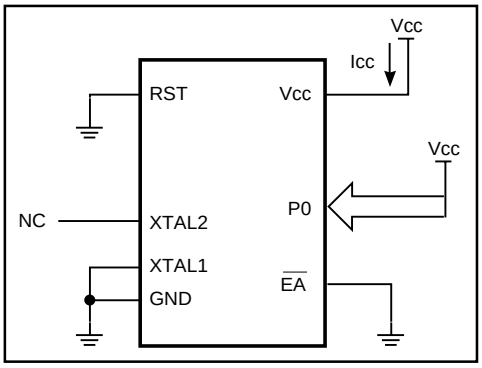

Figure 13. Power-down Mode

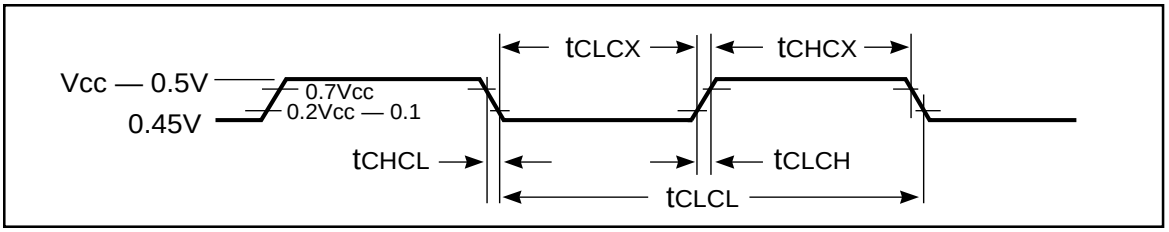

Figure 14. Clock Signal Waveform for Icc Tests in Active and Idle Modes. (t_{CLCH}=t_{CHCL}=5 ns)

AC CHARACTERISTICS

(T_A = 0°C to 70°C; Vcc = 3.3V ± 10%; GND = 0V; Cl for Port 0, ALE and PSEN Outputs = 100 pF; Cl for other outputs = 80 pF)

EXTERNAL MEMORY CHARACTERISTICS

		12 MHz Clock		24 MHz Clock		Variable Oscillator (3.5-24 MHz)		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1/t_{CLCL}	Oscillator frequency	—	—	—	—	3.5	24	MHz
t_{LHLL}	ALE pulse width	152	—	68	—	2t_{CLCL}–15	—	ns
t_{AVLL}	Address valid to ALE low	68	—	26	—	t_{CLCL}–15	—	ns
t_{LLAX}	Address hold after ALE low	73	—	31	—	t_{CLCL}–10	—	ns
t_{LLIV}	ALE low to valid instr in	—	313	—	147	—	4t_{CLCL}–20	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	73	—	31	—	t_{CLCL}–10	—	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	235	—	110	—	3t_{CLCL}–15	—	ns
t_{PLIV}	$\overline{PSEN}$ low to valid instr in	—	230	—	105	—	3t_{CLCL}–20	ns
t_{PXIX}	Input instr hold after $\overline{PSEN}$	0	—	0	—	0	—	ns
t_{PXIZ}	Input instr float after $\overline{PSEN}$	—	78	—	37	—	t_{CLCL}–5	ns
t_{AVIV}	Address to valid instr in	—	397	—	188	—	5t_{CLCL}–20	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float	—	10	—	10	—	10	ns
t_{RLRH}	$\overline{RD}$ pulse width	480	—	230	—	6t_{CLCL}–20	—	ns
t_{WLWH}	WR pulse width	480	—	230	—	6t_{CLCL}–20	—	ns
t_{RLDV}	$\overline{RD}$ low to valid data in	—	323	—	157	—	4t_{CLCL}–10	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	—	0	—	0	—	ns
t_{RHDZ}	Data float after $\overline{RD}$	—	162	—	78	—	2t_{CLCL}–5	ns
t_{LLDV}	ALE low to valid data in	—	573	—	282	—	7t_{CLCL}–10	ns
t_{AVDV}	Address to valid data in	—	656	—	323	—	8t_{CLCL}–10	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	230	270	105	145	3t_{CLCL}–20	3t_{CLCL}+20	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ low	313	—	146	—	4t_{CLCL}–20	—	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	68	—	26	—	t_{CLCL}–15	—	ns
t_{WHQX}	Data hold after $\overline{WR}$	73	—	31	—	t_{CLCL}–10	—	ns
t_{RLAZ}	$\overline{RD}$ low to address float	—	0	—	0	—	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ high to ALE high	68	98	26	57	t_{CLCL}–15	t_{CLCL}+15	ns

EXTERNAL MEMORY CHARACTERISTICS

(CONTINUED)

Symbol	Parameter	12 MHz Clock Min	12 MHz Clock Max	24 MHz Clock Min	24 MHz Clock Max	Variable Oscillator (3.5-24 MHz) Min	Variable Oscillator (3.5-24 MHz) Max	Unit
t_{XLXL}	Serial port clock cycle time	990	1010	290	310	$12t_{CLCL}-10$	$12t_{CLCL}+10$	ns
t_{QVXH}	Output data setup to clock rising edge	823	—	240	—	$10t_{CLCL}-10$	—	ns
t_{XHQX}	Output data hold after clock rising edge	157	—	40	—	$2t_{CLCL}-10$	—	ns
t_{XHDX}	Input data hold after clock rising edge	0	—	0	—	0	—	ns
t_{XHDV}	Clock rising edge to input data valid	—	833	—	250	—	$10t_{CLCL}$	ns

EXTERNAL CLOCK DRIVE

Symbol	wParameter	Min	Max	Unit
$1/t_{CLCL}$	Oscillator Frequency	3.5	40	MHz
t_{CHCX}	High time	10	—	ns
t_{CLCX}	Low time	10	—	ns
t_{CLCH}	Rise time	—	10	ns
t_{CHCL}	Fall time	—	10	ns

ROM VERIFICATION CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
$1/t_{CLCL}$	Oscillator Frequency	4	6	MHz
t_{AVQV}	Address to data valid	—	$48t_{CLCL}$	
t_{ELQV}	ENABLE low to data valid	—	$48t_{CLCL}$	
t_{EHQZ}	Data float after ENABLE	0	$48t_{CLCL}$	

TIMING WAVEFORMS

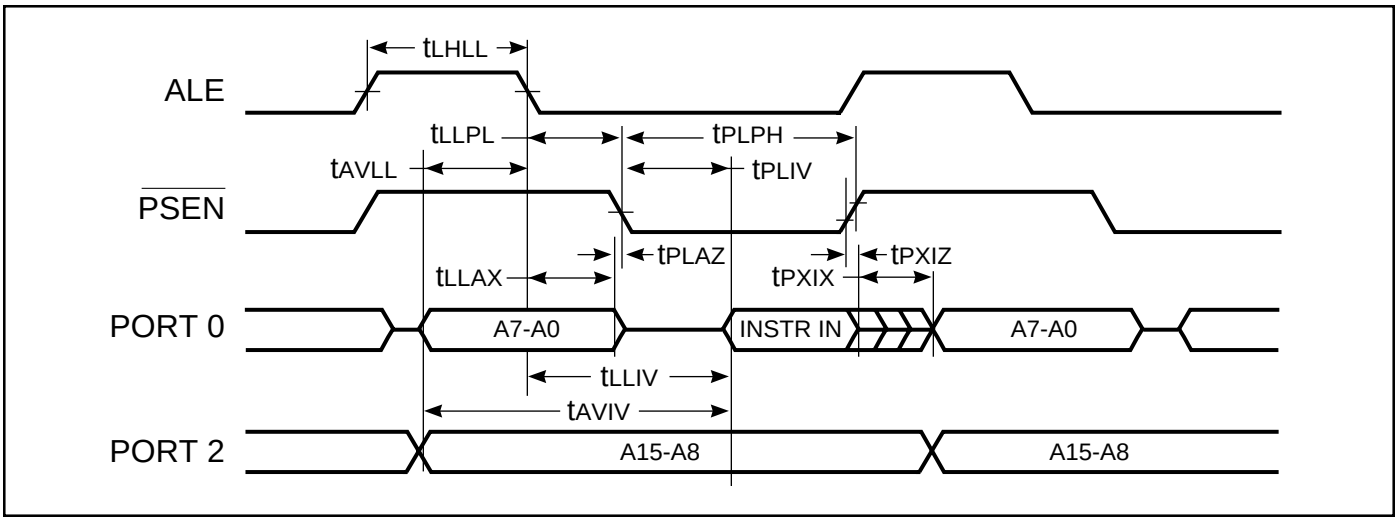

Figure 15. External Program Memory Read Cycle

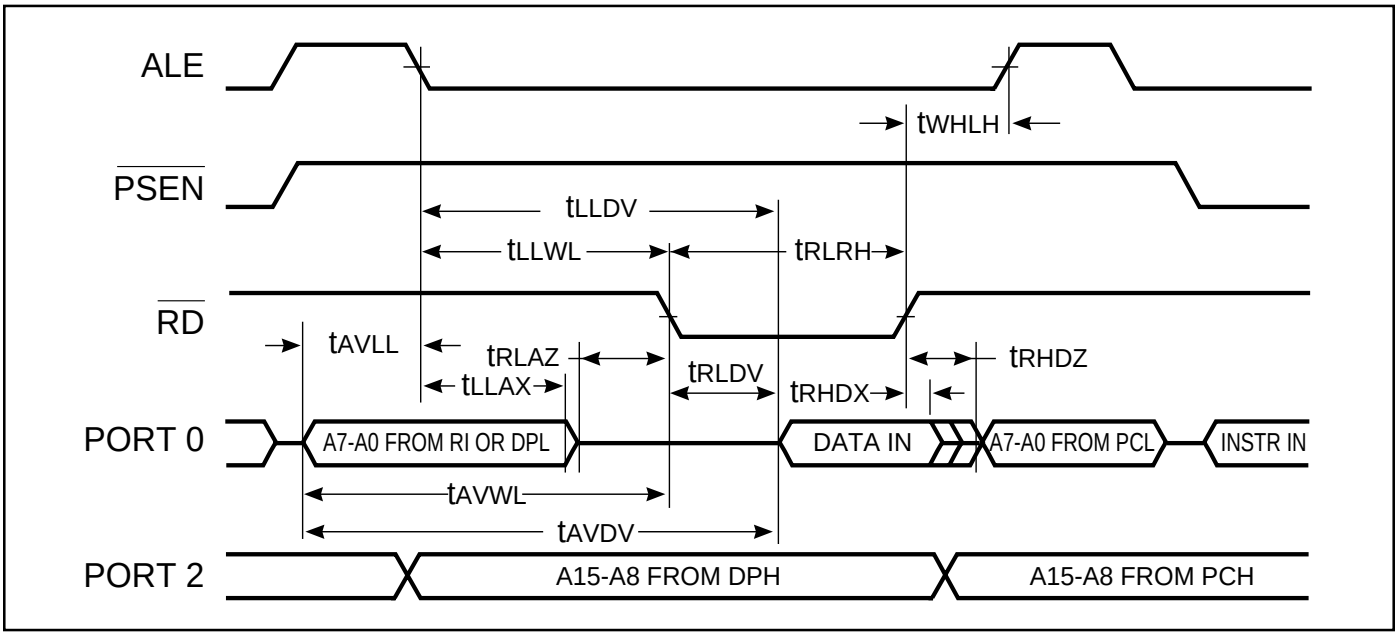

Figure 16. External Data Memory Read Cycle

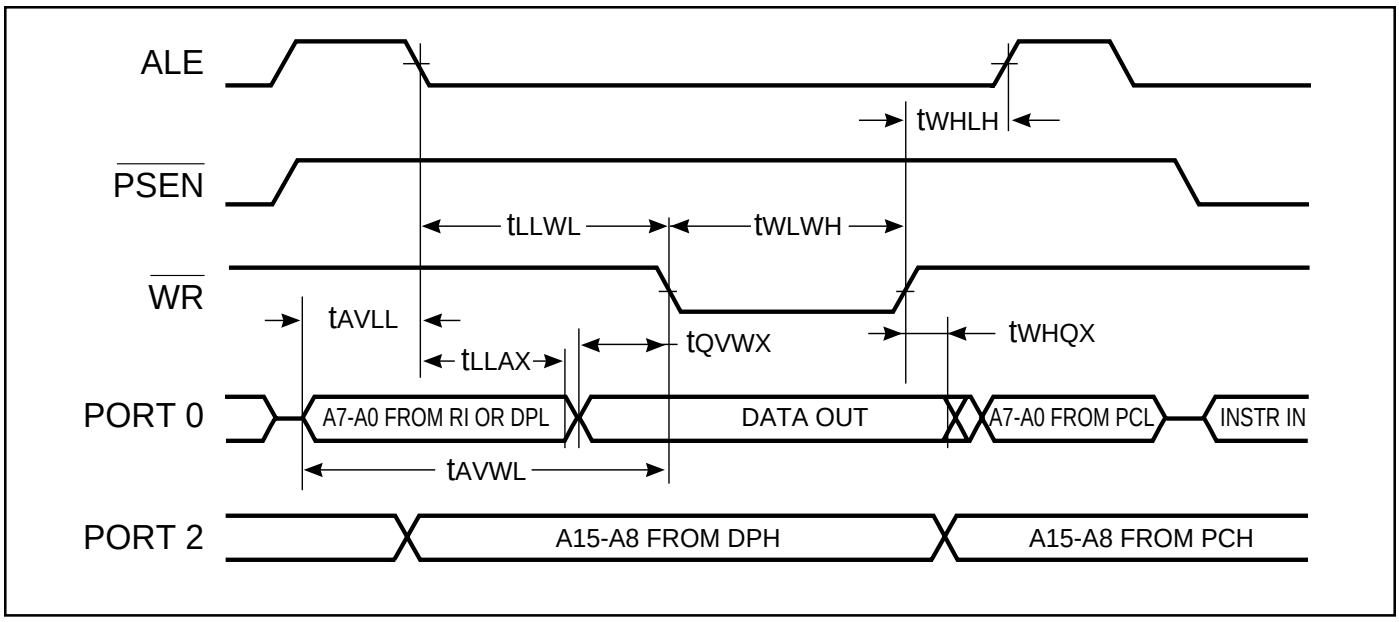

Figure 17. External Data Memory Write Cycle

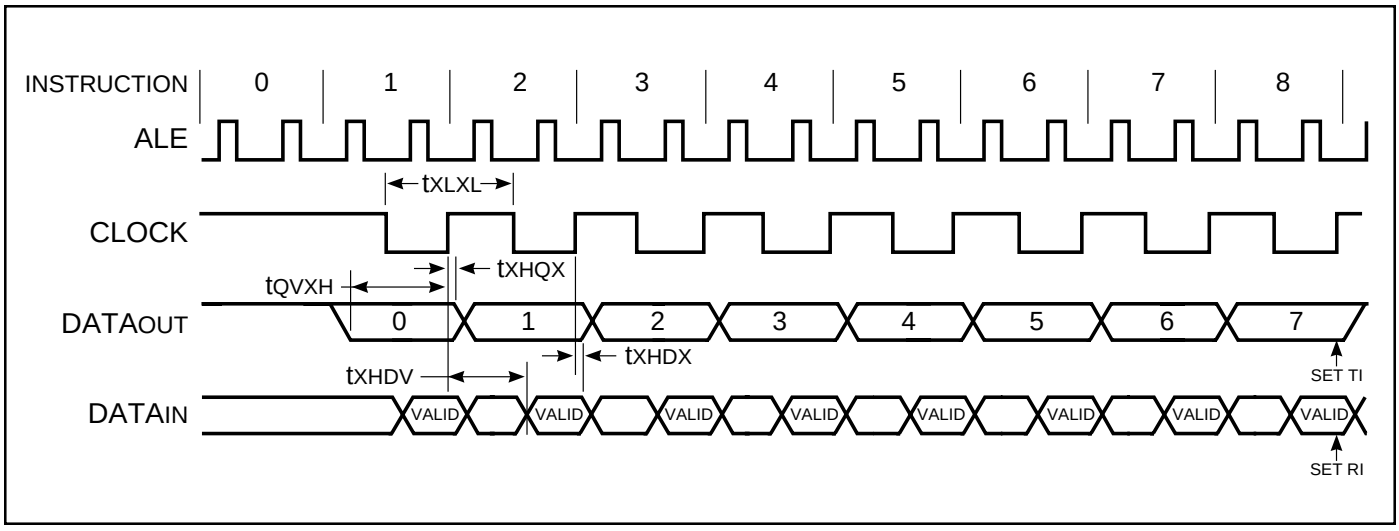

Figure 18. Shift Register Mode Timing Waveform

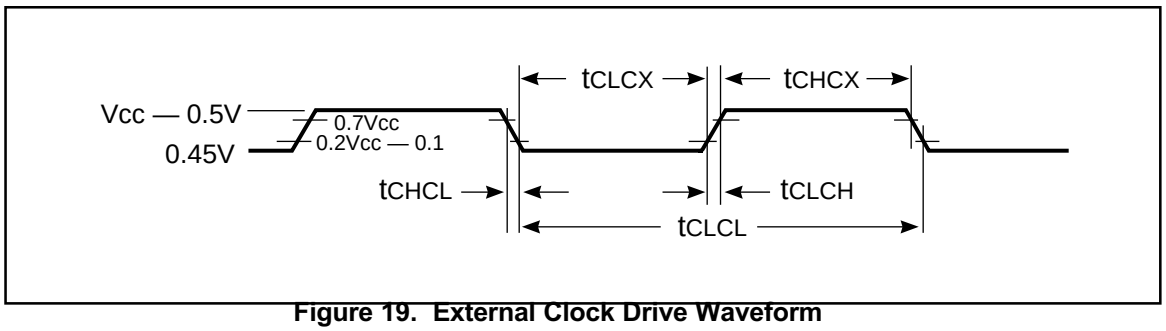

Figure 19. External Clock Drive Waveform

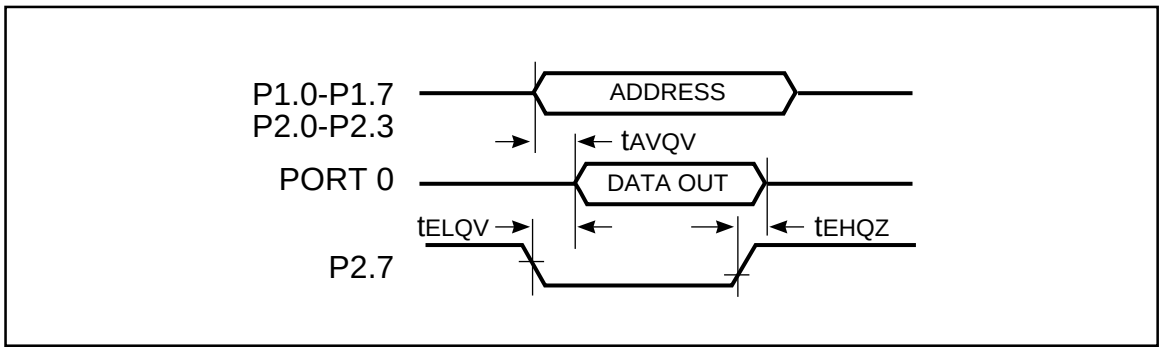

Figure 20. ROM Verification Waveforms

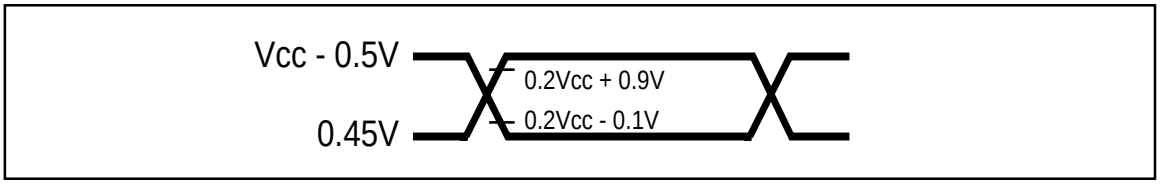

Figure 21. AC Test Point

Note:
1. AC inputs during testing are driven at VCC – 0.5V for logic “1” and 0.45V for logic “0”. Timing measurements are made at V_{IH} min for logic “1” and max for logic “0”.

ORDERING INFORMATION

COMMERCIAL TEMPERATURE: 0°C to +70°C

Speed	Order Part Number	Package
24 MHz	IC80LV52-24PL	PLCC
	IC80LV52-24PQ	PQFP
	IC80LV52-24W	600mil DIP
24 MHz	IC80LV32-24PL	PLCC
	IC80LV32-24PQ	PQFP
	IC80LV32-24W	600mil DIP

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FAX: 886-2-26962252
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