CMOS SINGLE CHIP 8-BIT MICROCONTROLLER with 8(4)-Kbytes of FLASH

FEATURES

- 80C52(51) based architecture
- 8(4)-Kbytes Flash memory with fast-pulse programming algorithm and software protection
- 256 x 8 RAM (128 x 8 RAM)
- Three (Two)16-bit Timer/Counters
- Full duplex serial channel
- Boolean processor
- Four 8-bit I/O ports, 32 I/O lines
- Memory addressing capability
  – 64K ROM and 64K RAM
- Program memory lock
  – Lock bits (3)
- Power save modes:
  – Idle and power-down
- Eight interrupt sources
- Most instructions execute in 0.5 µs
- CMOS and TTL compatible
- Maximum speed: 24 MHz @ Vcc = 3.3V
- Packages available:
  – 40-pin DIP
  – 44-pin PLCC
  – 44-pin PQFP

GENERAL DESCRIPTION

The ICSI IC89LV52(51)A is a high-performance microcontroller fabricated with high-density CMOS technology. The CMOS IC89LV52A is functionally compatible with the NMOS Intel 8052(51) and Philips' 80C52(51) micro controller, but its VCC is 3.05V~3.6V .

The IC89LV52(51)A contains a 8K (4K) x 8 Flash; a 256 x 8 RAM (128 x 8 RAM); 32 I/O lines for either multiprocessor communications; I/O expansion or full duplex UART; three (two) 16-bit timers/counters; a six-source (five-source), two-priority-level, nested interrupt structure; and on chip oscillator and clock circuit.

The IC89LV52(51)A can be expanded using standard TTL compatible memory.

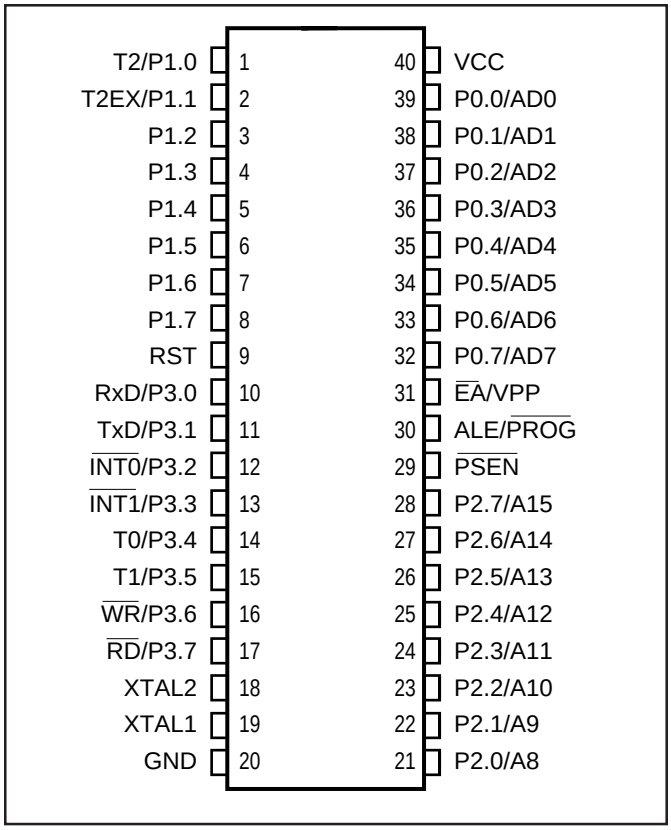


Figure 1. IC89LV52(51)A Pin Configuration: 40-pin DIP

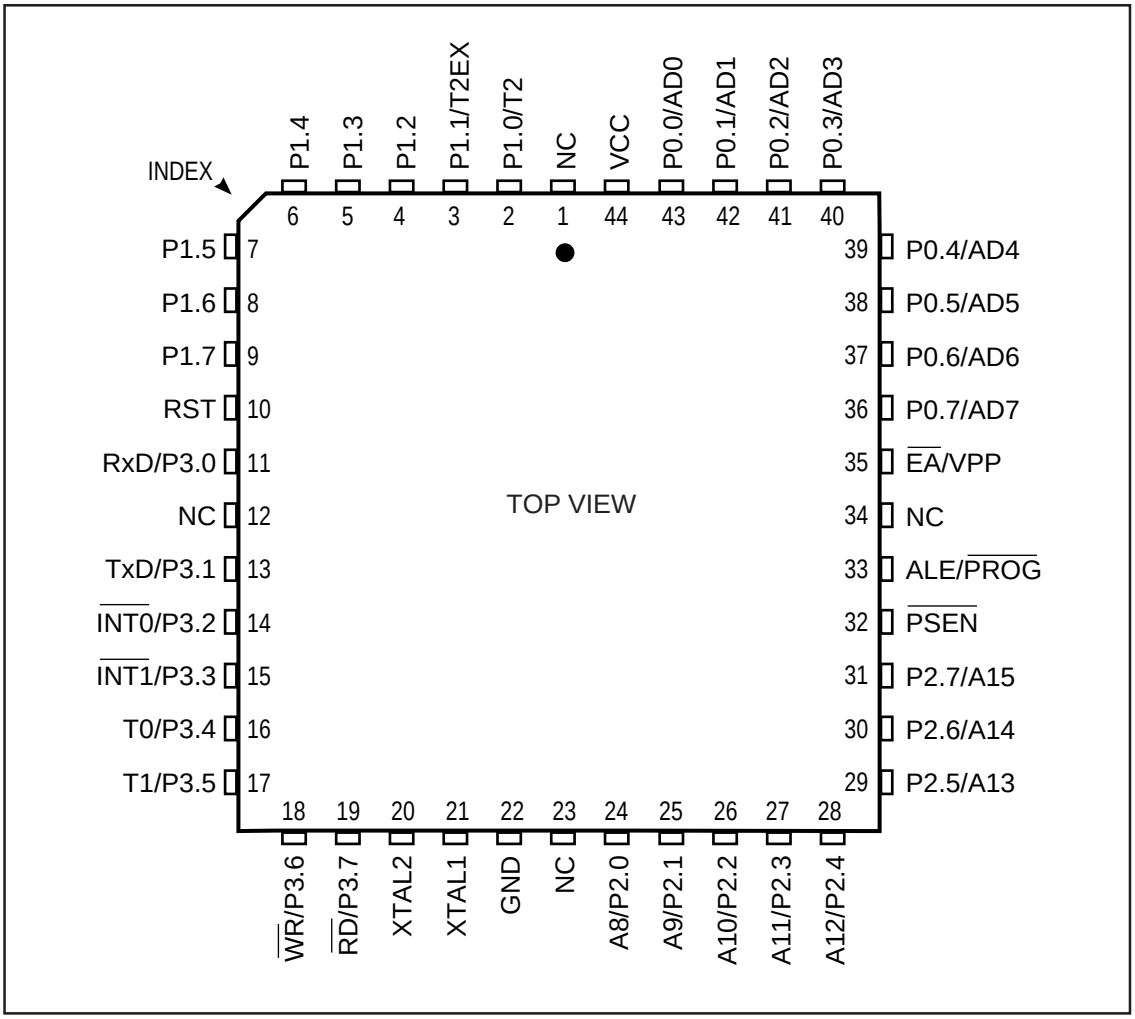


Figure 2. IC89LV52(51)A Pin Configuration: 44-pin PLCC

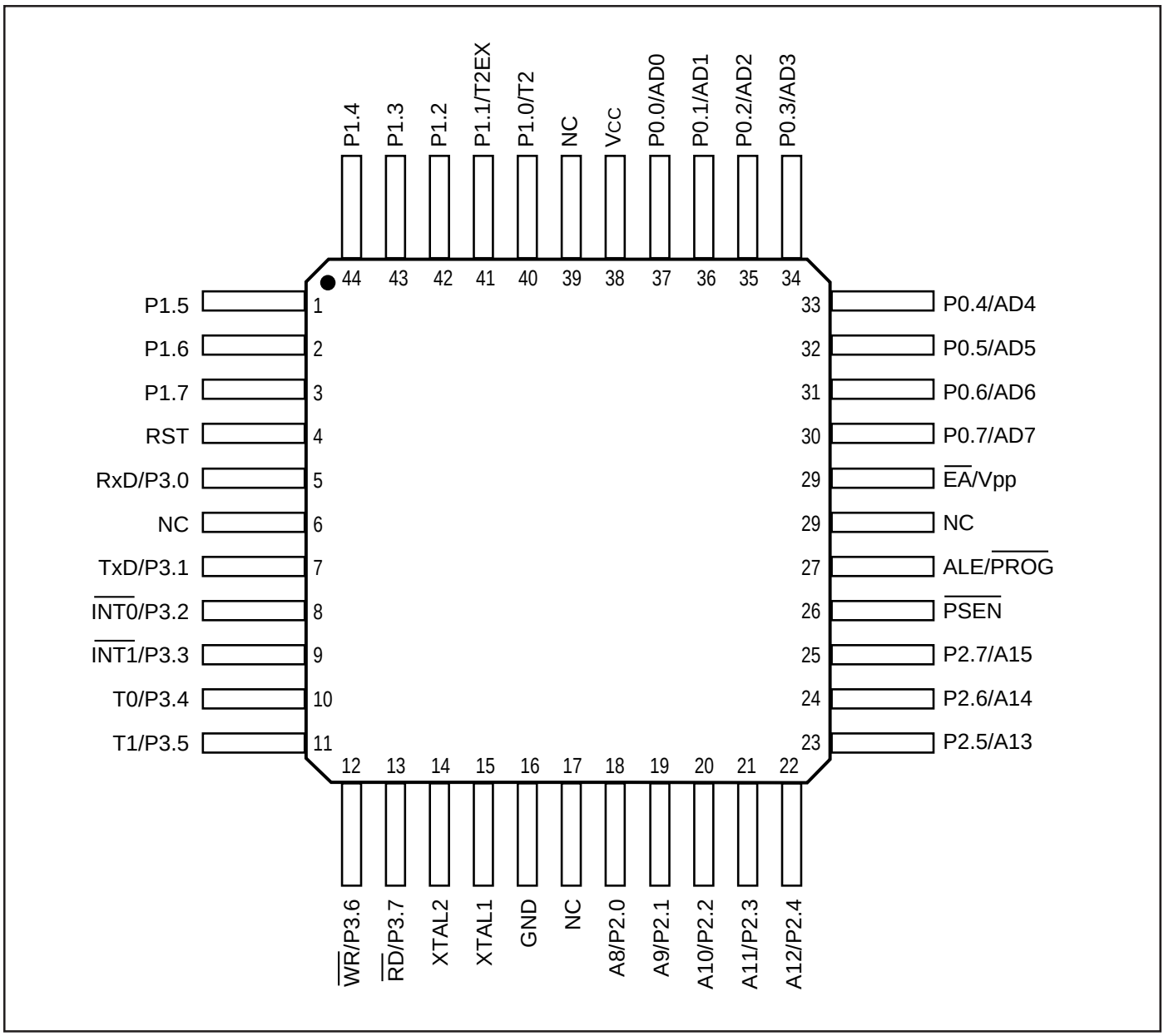


Figure 3. IC89LV52(51)A Pin Configuration: 44-pin PQFP

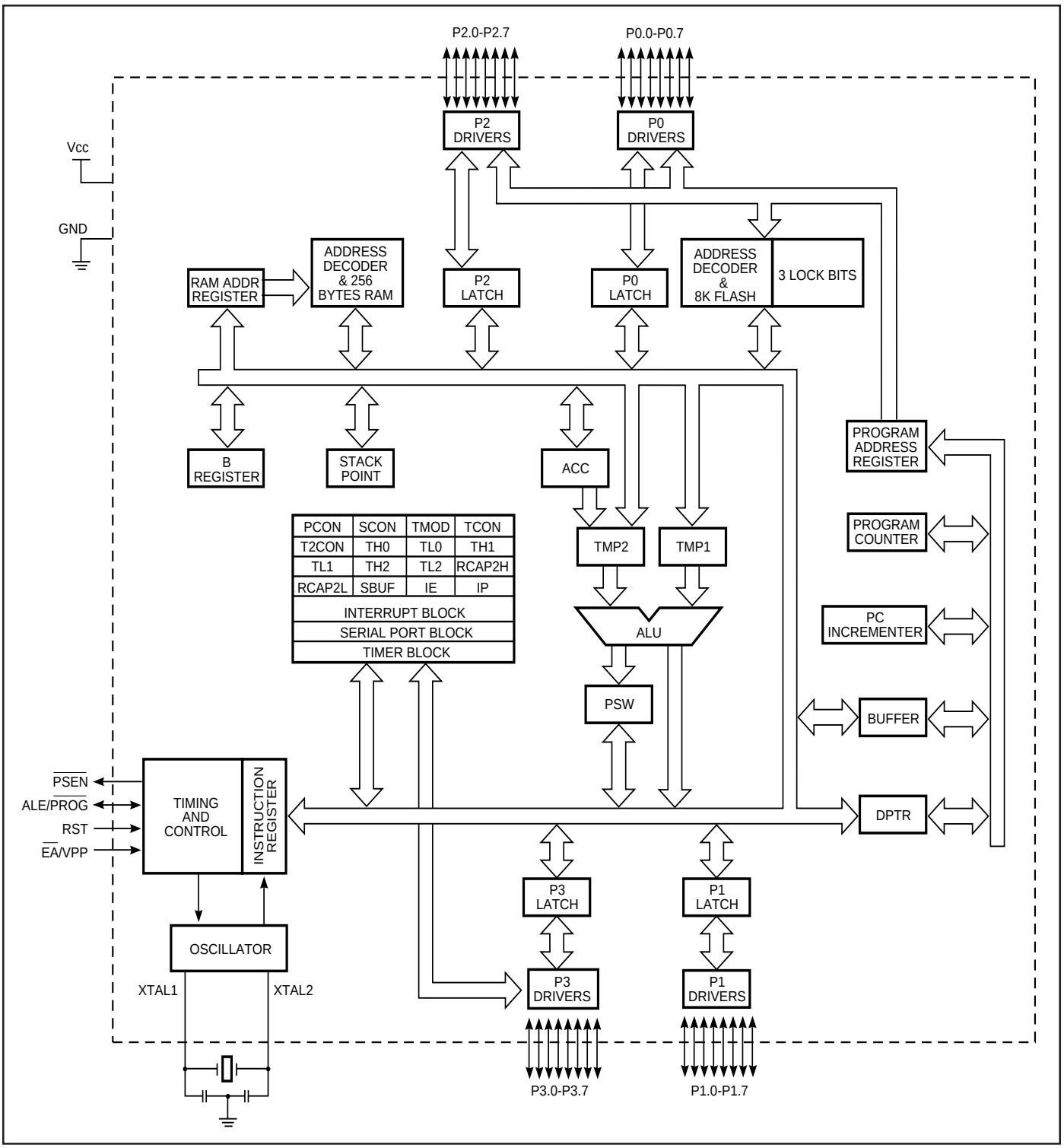


Figure 4. IC89LV52(51)A Block Diagram

Table 1. Detailed Pin Description

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an address to the external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the Program Pulse input ($\overline{PROG}$) during Flash programming.
$\overline{EA}$/V_{PP}	31	35	29	I	**External access enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address grater than 1FFFH. **IC89C51A internal Programming memory range is from 0000-0FFFH.** This is also receives the 12 V programming enable voltage (Vpp) during Flash programming, when 12 V programming is selected.
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0:** Port 0 is an 8-bit open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pullups when emitting 1s. Port 0 also receives the command and code bytes during programmable memory programming and outputs the code bytes during program verification. External pullups are required during program verification.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). The Port 1 output buffers can sink/source four TTL inputs. Port 1 also receives the low-order address byte during Flash programming and verification.
	1 2	2 3	40 41	I I	**T2(P1.0):** Timer/Counter 2 external count input.(IC89LV52A only) **T2EX(P1.1):** Timer/Counter 2 trigger input.(IC89LV52A only)
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). Port 2 emits the high order address byte during fetches from external program memory and during accesses to external data memory that used 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ Ri [i = 0, 1]), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order bits and some control signals during Flash programming and verification. P2.6 is a program command strobe signal. P2.7 is a data output enable signal.

Table 1. Detailed Pin Description *(continued)*

Symbol	PDIP	PLCC	PQFP	I/O	Name and Function
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pullups. (See DC Characteristics: I_{IL}). Port 3 also serves the special features of the IC89LV52(51)A, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port.
	11	13	7	O	**TxD (P3.1):** Serial output port.
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt 0.
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt 1.
	14	16	10	I	**T0 (P3.4):** Timer 0 external input.
	15	17	11	I	**T1 (P3.5):** Timer 1 external input.
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe. Program control signal while the chip programs and erases.
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe. Program control signal while the chip programs and erases.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. $\overline{PSEN}$ is an input control signal while memory program and verification.
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycleswhile the oscillator is running resets the device. An internal resistor to GND permits a power-on reset using only an external capacitor. A small internal resistor permits power-on reset using only a capacitor connected to VCC. RST is an input control signal during memory program and verification.
XTAL 1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL 2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.
GND	20	22	16	I	**Ground:** 0V reference.
Vcc	40	44	38	I	**Power Supply:** This is the power supply voltage for operation.

OPERATING DESCRIPTION

The detail description of the IC89LV52(51)A included in this description are:

- **Memory Map and Registers**
- **Timer/Counters**
- **Serial Interface**
- **Interrupt System**
- **Other Information**

The detail information desription of the IC89LV52(51)A refer to IS80C52/32 data sheet

Programming the IC89LV52(51)A:

The IC89LV52(51)A is normally shipped the on-chip Flash memory array in the erased state (i.e. contents=FFH) and ready to be programmed. The IC89LV52(51)A is programmed byte-by-byte in programming mode. Before the on-chip flash code memory can be re-programmed, the entire memory array must be erased electrically.

Programming Interface:

Some conditions must be satisfied before entering the programming mode. The conditions are listed following.

1. RST is high level
2. $\overline{\text{PSEN}}$ is low level
3. P3.6 and P3.7 is high level

The interface-controlled signals are matched these conditions, then the IC89C52(51)A will enter received command mode. The flash command is accepted by the flash command decoder in command received mode. The programming interface is listed in figure 5.

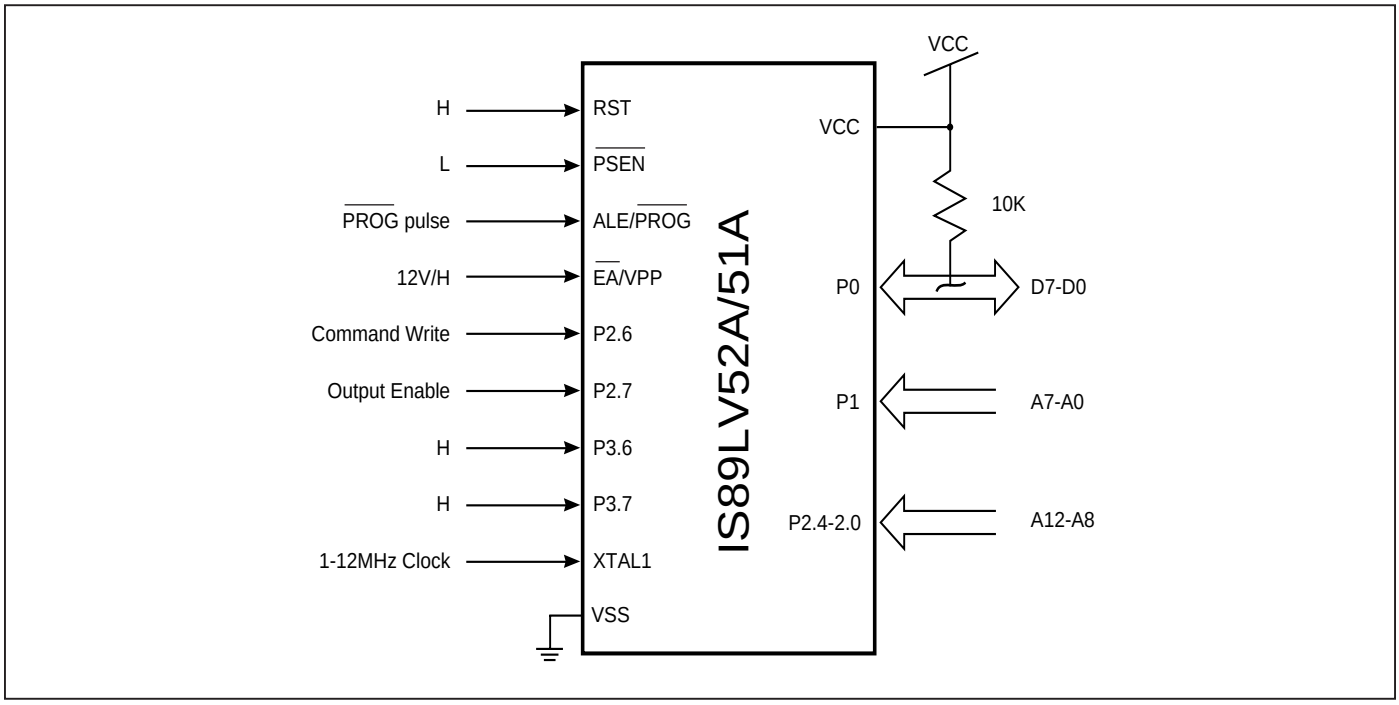


Figure 5. Programming Interface

Flash Command Definitions

	Bus	First Bus Cycle				Second Bus Cycle			
	Cycle	Operation	Address	Data	VPP	Operation	Address	Data	VPP
Normal Verify(1)	(n+1) (2)	P2.6 ⎍	X	00H	H	P2.7 Low	$SA_{(3)}$	$SD_{(3)}$	H
Read Signature Byte	4	P2.6 ⎍	X	90H	H	P2.7 Low	30H	D5H	
							31H	52H	
							32H	55H/AAH	
Program Code Memory	2	P2.6 ⎍	X	40H	H	$\overline{PROG}$ ⎍	$PA_{(3)}$	$PD_{(3)}$	12V/H
Program Verify(1)	(n+1) (2)	P2.6 ⎍	X	C0H	H	P2.7 Low	SA	$PVD_{(3)}$	H
Program Lock Bit 1	2	P2.6 ⎍	X	60H	H	$\overline{PROG}$ ⎍	X	D0H	12V/H
Program Lock Bit 2	2	P2.6 ⎍	X	70H	H	$\overline{PROG}$ ⎍	X	D0H	12V/H
Program Lock Bit 3	2	P2.6 ⎍	X	80H	H	$\overline{PROG}$ ⎍	X	D0H	12V/H
Chip Erase	2	P2.6 ⎍	X	20H	H	$\overline{PROG}$ ⎍	X	D0H	12V/H
Erase Verify(1)	(n+1) (2)	P2.6 ⎍	X	A0H	H	P2.7 Low	$EA_{(3)}$	$EVD_{(3)}$	H

Note:

1. Normal Verify: Internal flash sense amplifier uses the same threshold as instruction executing threshold.
   Program Verify: The flash sense amplifier applies an internally generated higher margin voltage to the addressed byte. If a comparison between the programmed byte and the true data is successful, there is a margin exists in the programmed data.
   Erase Verify: The flash sense amplifier applies an internally generated lower margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the bytes are erased.
2. To verify n bytes data.
3. SA = Selected Address of memory location to be read except program or erase verify.
   SD = Data read from location SA with Normal Verification threshold.
   PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   PVD = Data read from location PA during program verify.
   EA = Address of memory location to be read during erase verify.
   EVD - Data read from location EA during erase verify.

Programming Core Memory

Every code byte in the Flash array can be written and the entire array can be erased using the appropriate command from Port 0 by programmer or application system. The program/erase are two-cycle operations. The first cycle is command write cycle; the command 40H is written by P2.6 falling and rising edges. The command would be held a stable value within P2.6 low state. The command decoder enables programming flag after the first cycle is completion, then the internal programming flag is set. Rising edge of $\overline{PROG}$ will clear internal programming flag, so the programming command must be presented every programming cycle. The second cycle is real flash programming cycle. The programming address and data are latched at $\overline{PROG}$ falling edge, the programming time is controlled by low time of $\overline{PROG}$. The programming flag is cleared at $\overline{PROG}$ rising edge in the second cycle. Programming address range is from 0 to 1FFFH. IC89LV52(51)A programming range is from 0 to 1FFFH, but the program counter will jump to external menory while MCU executing the address is excess 0FFFH.

The IC89LV52(51)A code memory programming now is described in Figure 6.

Program Verify

If lock bits LB2 and LB3 have not been programmed, the programmed code data can be read back via the address and data lines for verification. 'C0H' command is needed for switching to program verify mode. During program verify, the code memory use the internally-generated higher margin voltage to the addressed byte.

Normal Verify

If lock bits LB2 and LB3 have not been programmed, the programmed code data can be read back via the address and data lines for verification. If flash command decoder receives the '00H' command or IC89C52(51)A power is initialized, the command decoder switches to normal verify mode. During normal verify, the code memory use the same threshold as instruction executing threshold.

Erase Verify

If lock bits LB2 and LB3 have not been programmed, the programmed code data can be read back via the address and data lines for verification. 'A0H' command is needed for switching to erase verify mode. During erase verify, the code memory use the internally-generated lower margin voltage to the addressed byte.

Program Lock Bit 1, 2, 3

The lock bit 1, 2, 3 is programmed by using the erase command '60H', '70H' and '80H' in the first cycle. In the second cycle, the 'D0H' command is presented on whole $\overline{PROG}$ strobe time. The $\overline{PROG}$ strobe time is real lock bits programming time. The $\overline{PROG}$ rising edge will clear the erasing state to normal verify state. The programming lock bits operations don't use the smart algorithm but it is programmed 10 times directly. If programming lock bits are needed, it must be programmed after the encryption array and code memory programming.

The IC89C52(51)A lock bits programming flow is described in Figure 7.

Chip Erase

All flash cell must be programmed to '00' before the chip is erased. The programming sequence is encryption array, code memory and lock bit 1, 2, 3. The entire flash array is erased electrically by using the erase command '20H' in the first cycle. In the second cycle, the 'D0H' command is presented on whole $\overline{PROG}$ strobe time. The $\overline{PROG}$ strobe time is real flash erasing time. The $\overline{PROG}$ rising edge will clear the erasing state to normal verify state. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed. If the any flash cell is not '1' (include encryption array and lock bits) repeat erase condition less than 50 times.

The IC89C52(51)A detail erase flow is described in Figure 8.

Reading the Signature Bytes:

The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H and 032H, except that command is '90H'. The values returned are:

(030H) = D5H indicates manufactured by ICSI

(031H) = 52H indicates IC89C52A/IC89C51A

(032H) = AAH indicates programming voltage is 12V

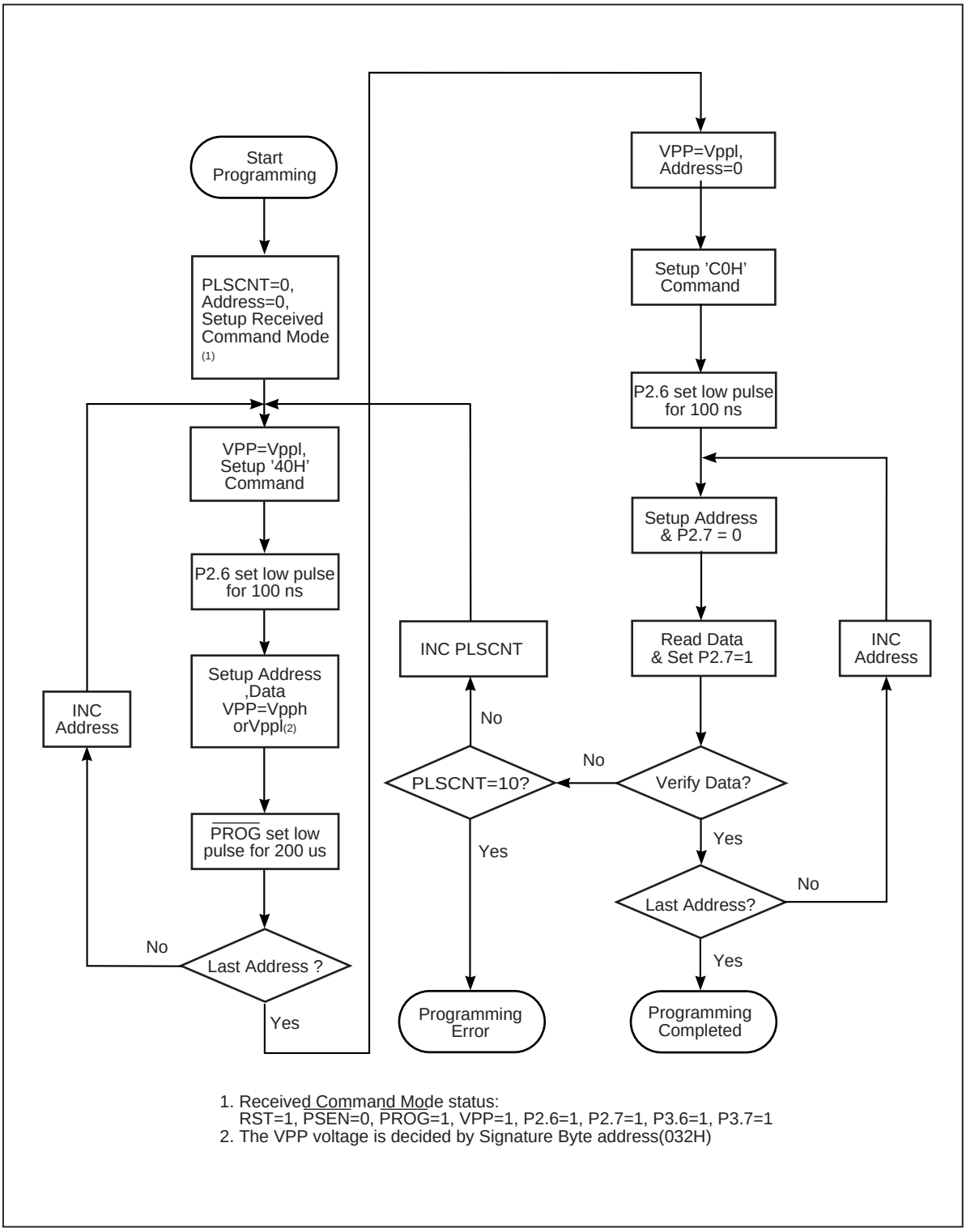
55H indicates programming voltage is 5V

The signatures can be read by following conditions. It's easier to recognize by programmer.

1. RST = high level. $\overline{PSEN}$ = Low level. $\overline{PROG}$ = High level. VPP = High Level. P2.6 = Low level. P2.7 = Low level. P3.6 = Low level. P3.7 = Low level.
2. Address is switched to (030H), (031H) and (032H). Then the Data bus outputs the D5H, 52H, AAH (55H).

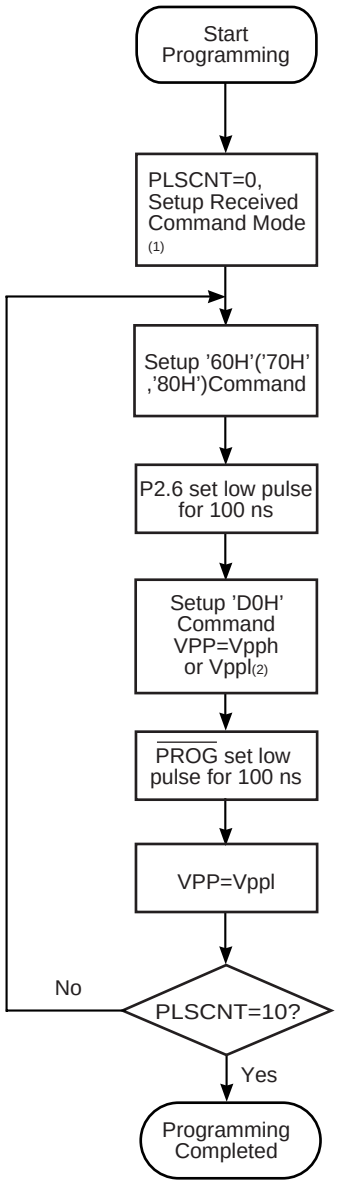
Lock bits Features

Program Lock bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock feature enabled.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as 2, also verify is disabled
4	P	P	P	Same as 3, also external execution is disabled



1. Received Command Mode status:
   RST=1, PSEN=0, PROG=1, VPP=1, P2.6=1, P2.7=1, P3.6=1, P3.7=1
2. The VPP voltage is decided by Signature Byte address(032H)

Figure. 6 IC89LV52(51)A Main Memory Programming Flow



1. Received Command Mode status:
   RST=1, PSEN=0, PROG=1, VPP=1, P2.6=1, P2.7=1, P3.6=1, P3.7=1
2. The VPP voltage is decided by Signature Byte address(032H)

Figure. 7 IC89LV52(51)A Lock Bits Programming Flow

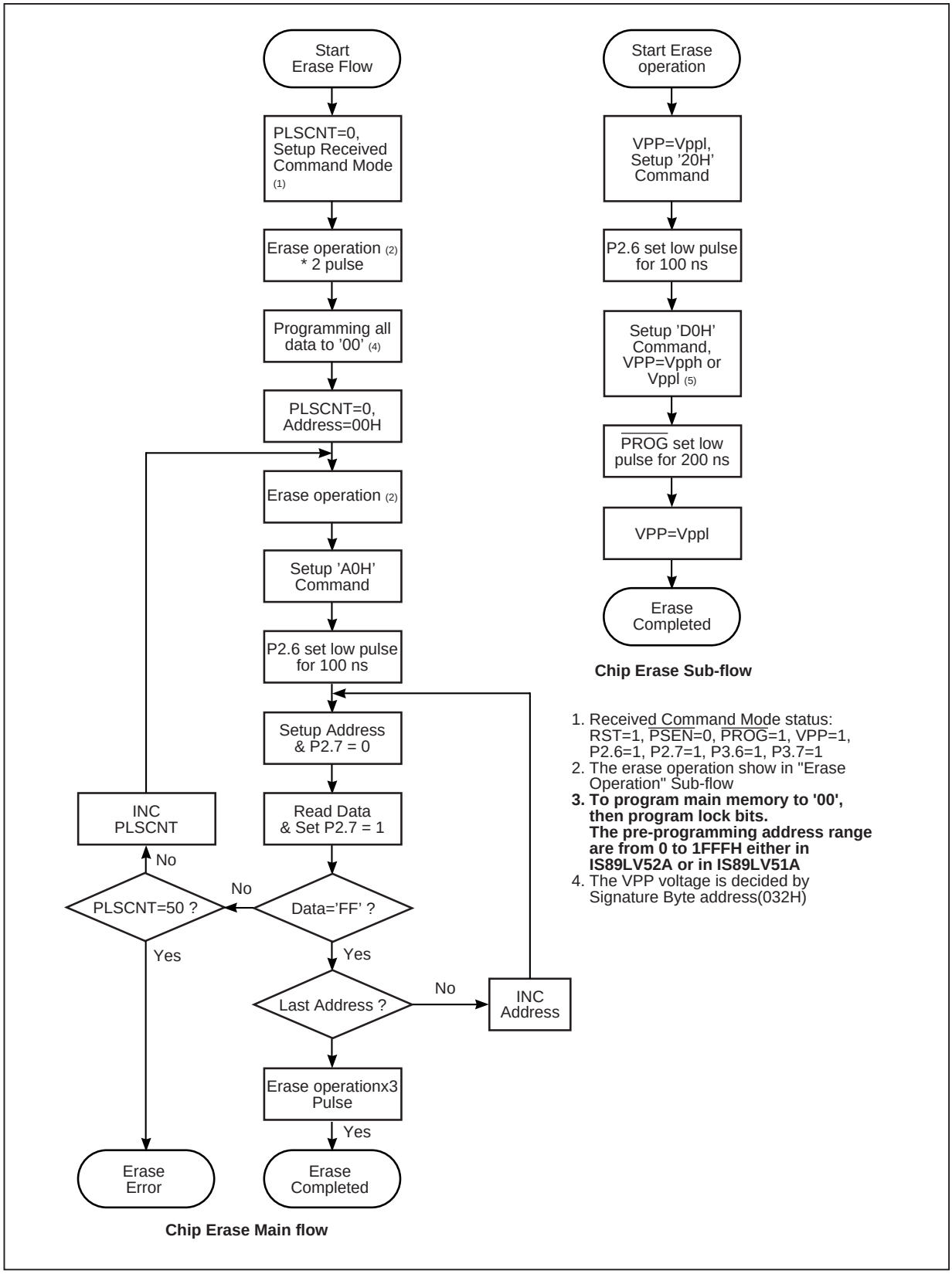


Figure. 8 IC89LV52(51)A Erase Flow

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND[2]	–2.0 to +7.0	V
T_{BIAS}	Temperature Under Bias[3]	0 to +70	°C
T_{STG}	Storage Temperature	–65 to +125	°C
P_T	Power Dissipation	1.5	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2. 0V for periods less than 20 ns. Maximum DC voltage on output pins is Vcc + 0.5V which may overshoot to Vcc + 2.0V for periods less than 20 ns.
3. Operating temperature is for commercial products only defined by this specification.

OPERATING RANGE[1]

Range	Ambient Temperature	Vcc	Oscillator Frequency
Commercial	0°C to +70°C	3.05V to 3.6V ; 5V ± 10%	3.5 to 24 MHz

Note:
1. Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(Ta=0°C to 70°C; VCC=3.05V-3.6V ; VSS=0V)

Symbol	Parameter	Test conditions	Min	Max	Unit
V_{IL}	Input low voltage (All except $\overline{EA}$)		–0.5	0.2Vcc + 0.1	V
$V_{IL}1$	Input low voltage (XTAL 1,$\overline{EA}$)		–0.5	0.2Vcc + 0.1	V
V_{IH}	Input high voltage (All except XTAL 1, RST, $\overline{EA}$)		0.2Vcc + 0.9	Vcc + 0.5	V
$V_{IH}1$	Input high voltage (XTAL 1)		0.7Vcc	Vcc + 0.5	V
$V_{SCH}+$	RST positive schmitt-trigger threshold voltage		0.7Vcc	Vcc + 0.5	V
$V_{SCH}–$	RST negative schmitt-trigger threshold voltage		0	0.3Vcc	V
V_{OL}(1)	Output low voltage (Ports 1, 2, 3)	I_{OL} = 1.6 mA	—	0.45	V
$V_{OL}1$(1)	Output low voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA	—	0.45	V
V_{OH}	Output high voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = –20 µA	Vcc-0.9	—	V
$V_{OH}1$	Output high voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OH} = –800 µA	V_{CC}-0.9	—	V
I_{IL}	Logical 0 input current (Ports 1, 2, 3)	V_{IN} = 0.45V	—	–50	µA
I_{LI}	Input leakage current (Port 0)	0.45V < V_{IN} < Vcc	–5	+5	µA
I_{TL}	Logical 1-to-0 transition current (Ports 1, 2, 3)	V_{IN} = 1.5V	—	–450	µA
R_{RST}	RST pulldown resister	V_{IN}=V_{CC}	150	450	KΩ

Note:

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port
   Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
   Pins are not guaranteed to sink greater than the listed test conditions.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test conditions	Min	Max	Unit
Icc	Power supply current[1]	Vcc = 3.3V			
	Active mode	12 MHz	—	15	mA
		24 MHz	—	24	mA
	Idle mode	12 MHz	—	4	mA
		24 MHz	—	8	mA
	Power-down mode	Vcc = 3.3V	—	50	µA

Note:
1. See Figures9,10,11 and 12 for Icc test conditiions.

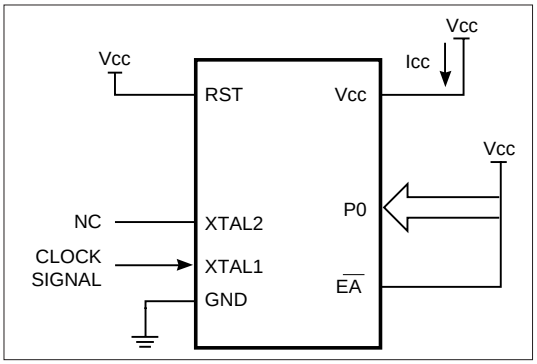


Figure 9. Active Mode

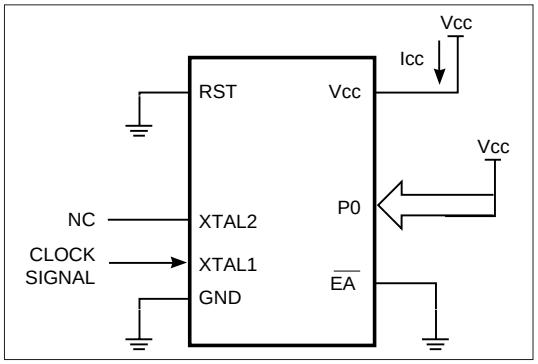


Figure 10. Idle Mode

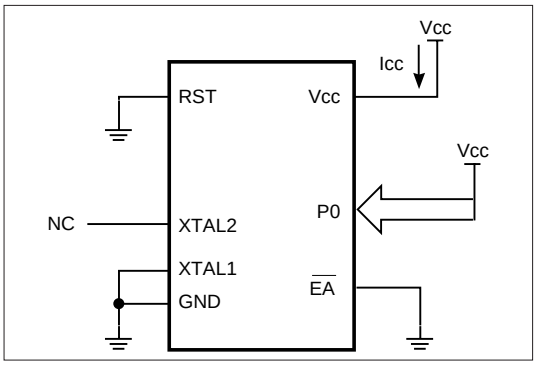


Figure 11. Power-down Mode
(Vcc = 2.0V ~ 3.0V)

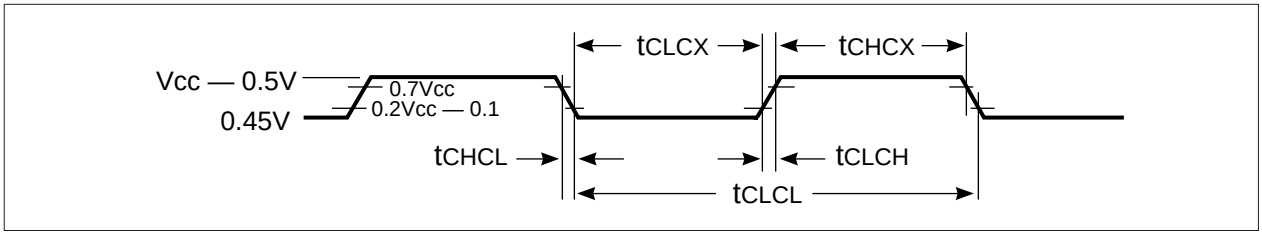


Figure 12. Clock Signal Waveform for I_{CC} Tests in Active and Idle Mode (t_{CLCH}=t_{CHCL}=5 ns)

AC CHARACTERISTICS

(Ta=0°C to 70 °C; V_{CC}=3.05V~3.6V ; V_{SS}=0V; C1 for port 0, ALE and $\overline{PSEN}$ Outputs=100pF; C1 for other outputs=80pF)

EXTERNAL MEMORY CHARACTERISTICS

		24 MHz Clock		12 MHz Clock		Variable Oscillator (3.5 - 24 MHz)		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1/t_{CLCL}	Oscillator frequency	—	—	—	—	3.5	24	MHz
t_{LHLL}	ALE pulse width	68	—	152	—	2t_{CLCL}–15	—	ns
t_{AVLL}	Address valid to ALE low	26	—	68	—	t_{CLCL}–15	—	ns
t_{LLAX}	Address hold after ALE low	31	—	73	—	t_{CLCL}–10	—	ns
t_{LLIV}	ALE low to valid instr in	—	147	—	312	—	4t_{CLCL}–20	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	31	—	68	—	t_{CLCL}–10	—	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	110	—	235	—	3t_{CLCL}–15	—	ns
t_{PLIV}	$\overline{PSEN}$ low to valid instr in	—	105	—	230	—	3t_{CLCL}–20	ns
t_{PXIX}	Input instr hold after $\overline{PSEN}$	0	—	0	—	0	—	ns
t_{PXIZ}	Input instr float after $\overline{PSEN}$	—	37	—	78	—	t_{CLCL}–5	ns
t_{AVIV}	Address to valid instr in	—	188	—	397	—	5t_{CLCL}–20	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float	—	10	—	10	—	10	ns
t_{RLRH}	$\overline{RD}$ pulse width	230	—	480	—	6t_{CLCL}–20	—	ns
t_{WLWH}	$\overline{WR}$ pulse width	230	—	480	—	6t_{CLCL}–20	—	ns
t_{RLDV}	$\overline{RD}$ low to valid data in	—	157	—	323	—	4t_{CLCL}–10	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	—	0	—	0	—	ns
t_{RHDZ}	Data float after $\overline{RD}$	—	78	—	162	—	2t_{CLCL}–5	ns
t_{LLDV}	ALE low to valid data in	—	282	—	573	—	7t_{CLCL}–10	ns
t_{AVDV}	Address to valid data in	—	323	—	656	—	8t_{CLCL}–10	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	105	145	230	270	3t_{CLCL}–20	3t_{CLCL}+20	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ low	146	—	313	—	4t_{CLCL}–20	—	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	26	—	68	—	t_{CLCL}–15	—	ns
t_{WHQX}	Data hold after $\overline{WR}$	31	—	73	—	t_{CLCL}–10	—	ns
t_{RLAZ}	$\overline{RD}$ low to address float	—	0	—	0	—	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ high to ALE high	26	57	68	98	t_{CLCL}–15	t_{CLCL}+15	ns

SERIAL PORT TIMING: SHIFT REGISTER MODE

Symbol	Parameter	24 MHz Clock Min	24 MHz Clock Max	12 MHz Clock Min	12 MHz Clock Max	Variable Oscillator (3.5-24 MHz) Min	Variable Oscillator (3.5-24 MHz) Max	Unit
t_{XLXL}	Serial port clock cycle time	490	—	990	—	$12t_{CLCL}$–10	—	ns
t_{QVXH}	Output data setup to clock rising edge	327	—	743	—	$10t_{CLCL}$–90	—	ns
t_{XHQX}	Output data hold after clock rising edge	58	—	142	—	$2t_{CLCL}$–25	—	ns
t_{XHDX}	Input data hold after clock rising edge	0	—	0	—	0	—	ns
t_{XHDV}	Clock rising edge to input data valid	—	284	—	700	—	$10t_{CLCL}$—133	ns

EXTERNAL CLOCK DRIVE CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
$1/t_{CLCL}$	Oscillator Frequency	3.5	24	MHz
t_{CHCX}	High time	10	—	ns
t_{CLCX}	Low time	10	—	ns
t_{CLCH}	Rise time	—	10	ns
t_{CHCL}	Fall time	—	10	ns

Flash Program/Erase and Verification & Test Mode Characteristics

Symbol	Parameter	Min	Max	Unit
Vcc	Programming and Erase Power Voleage	5.25	5.75	V
Vpp	Programming and Erase Enable Voltage	11.5	12.5	V
Ipp	Programming and Erase Enable Current	-	2.0	mA
tDVCL	Data Valid to Command Setup Low	10	-	ns
tCLCH	Command Setup Width	100	-	ns
tCHDX	Data Hold after Command Setup	10	-	ns
tAVGL	Address Setup to $\overline{\text{PROG}}$ Low	20	-	ns
tGHAX	Address Hold after $\overline{\text{PROG}}$	20	-	ns
tDVGL	Data Setup to $\overline{\text{PROG}}$ Low	20	-	ns
tGHDX	Data Hold after $\overline{\text{PROG}}$	20	-	ns
tSHGL	Vpp Setup to $\overline{\text{PROG}}$ Low	10	-	us
tGHSL	Vpp Hold after $\overline{\text{PROG}}$	10	-	us
tGLGH	$\overline{\text{PROG}}$ Pulse Width in Programming Cycle	200	-	us
tGLGHE	$\overline{\text{PROG}}$ Pulse Width in Erase Cycle	200	-	ms
tAVQV	Address Valid to Data Valid	-	50	ns
tELQV	$\overline{\text{ENABLE}}$ Low to Data Valid	-	50	ns
tAXQX	Data Float after Address Float	0	-	ns
tEHQX	Data Float after $\overline{\text{ENABLE}}$	0	-	ns

TIMING WAVEFORMS

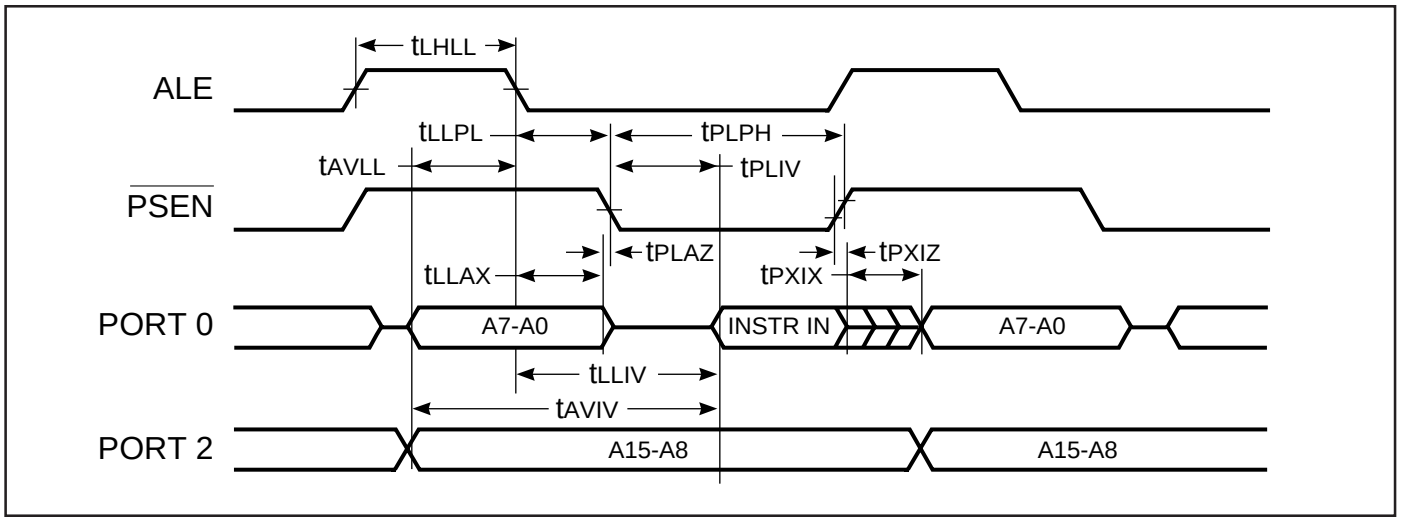


Figure 13. External Program Memory Read Cycle

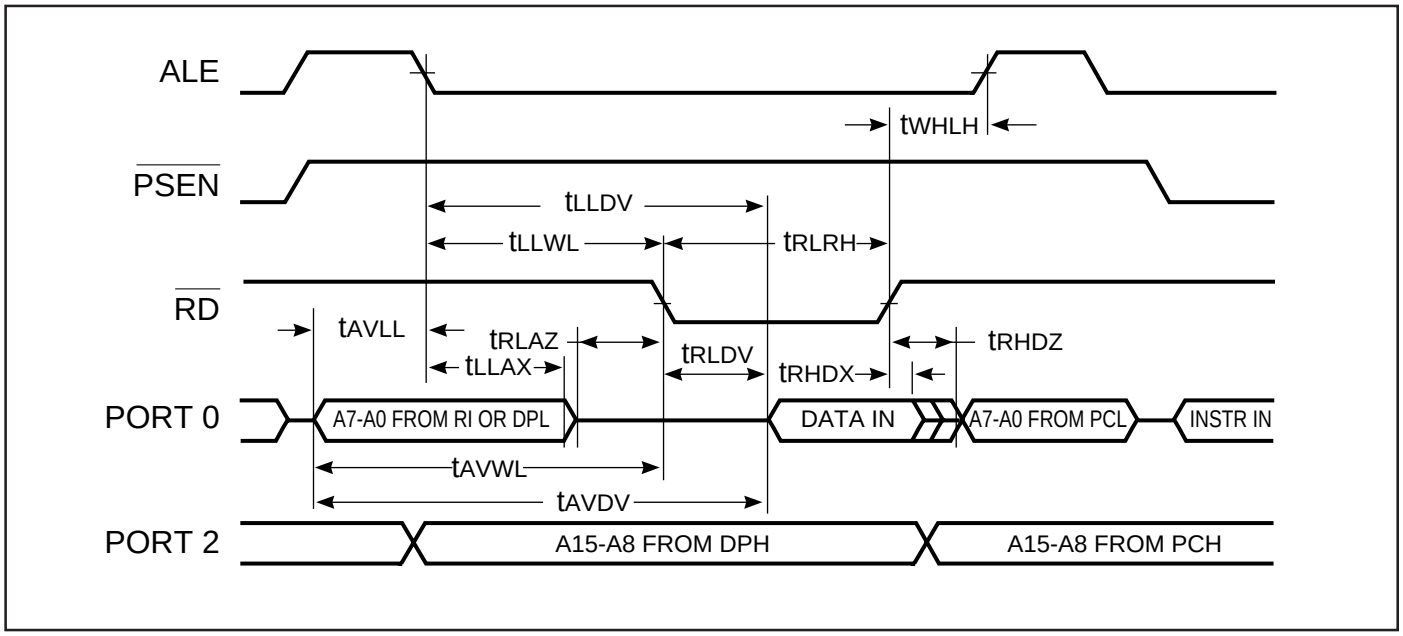


Figure 14. External Data Memory Read Cycle

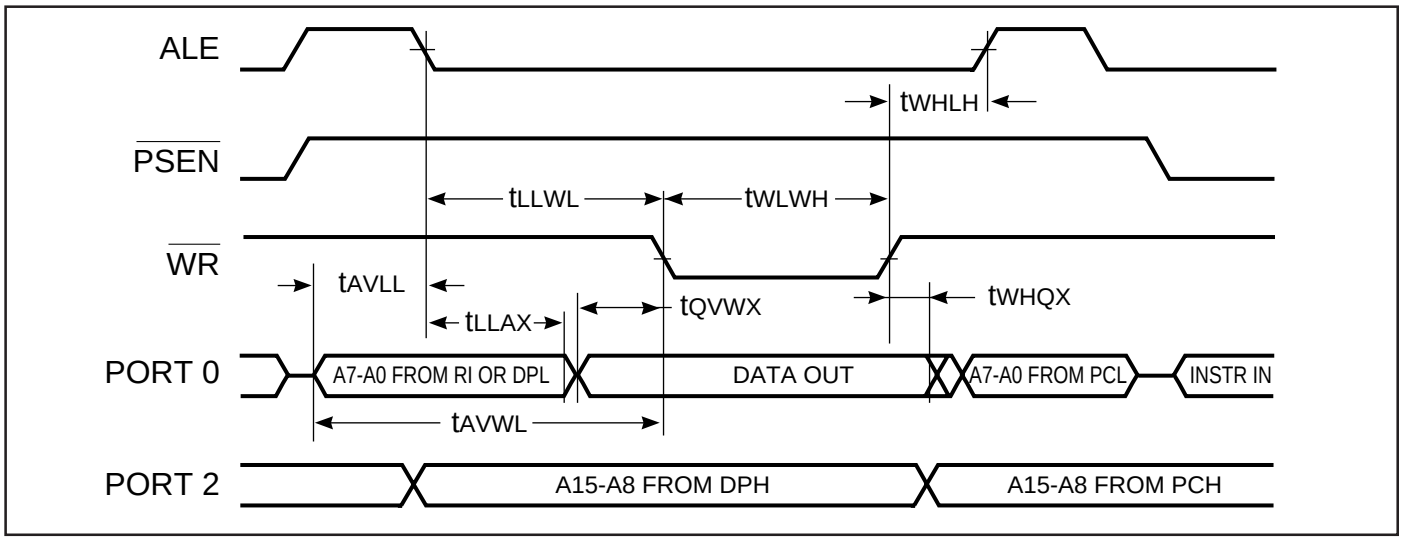


Figure 15. External Data Memory Write Cycle

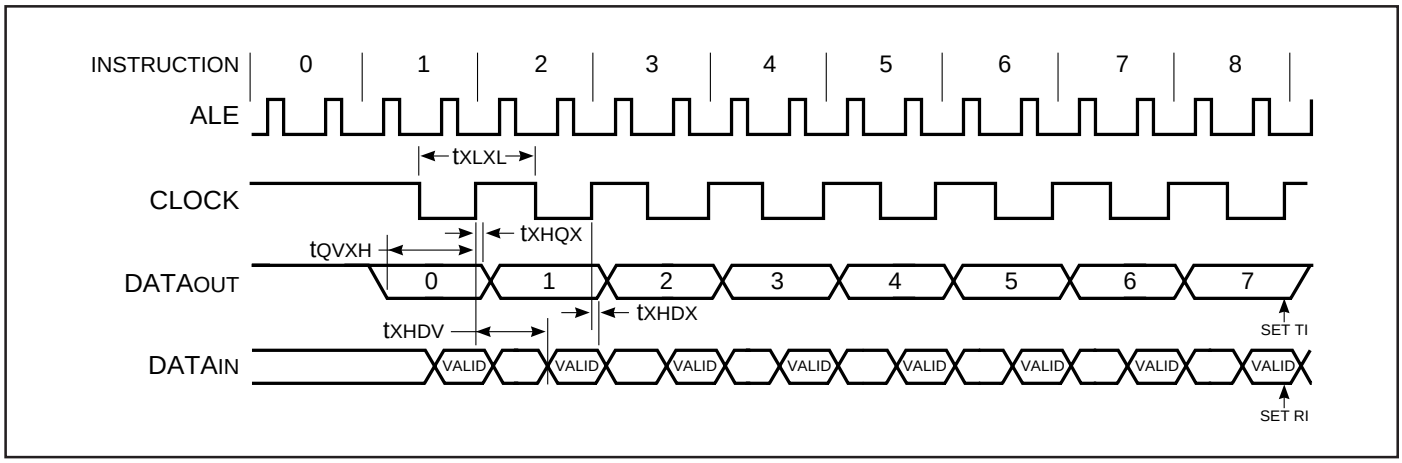


Figure 16. Shift Register Mode Timing Waveform

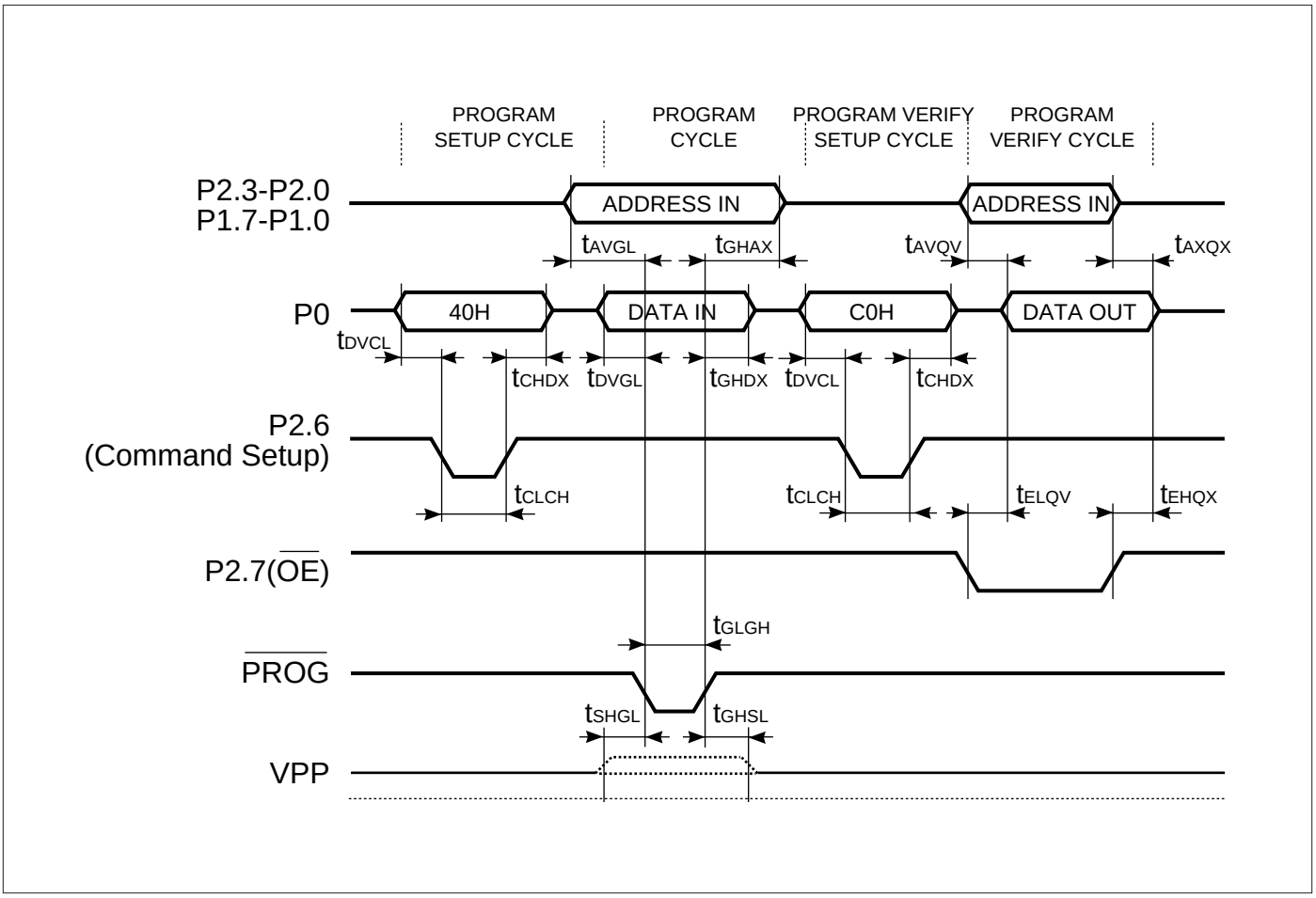


Figure 17. Programming Timing Wavform

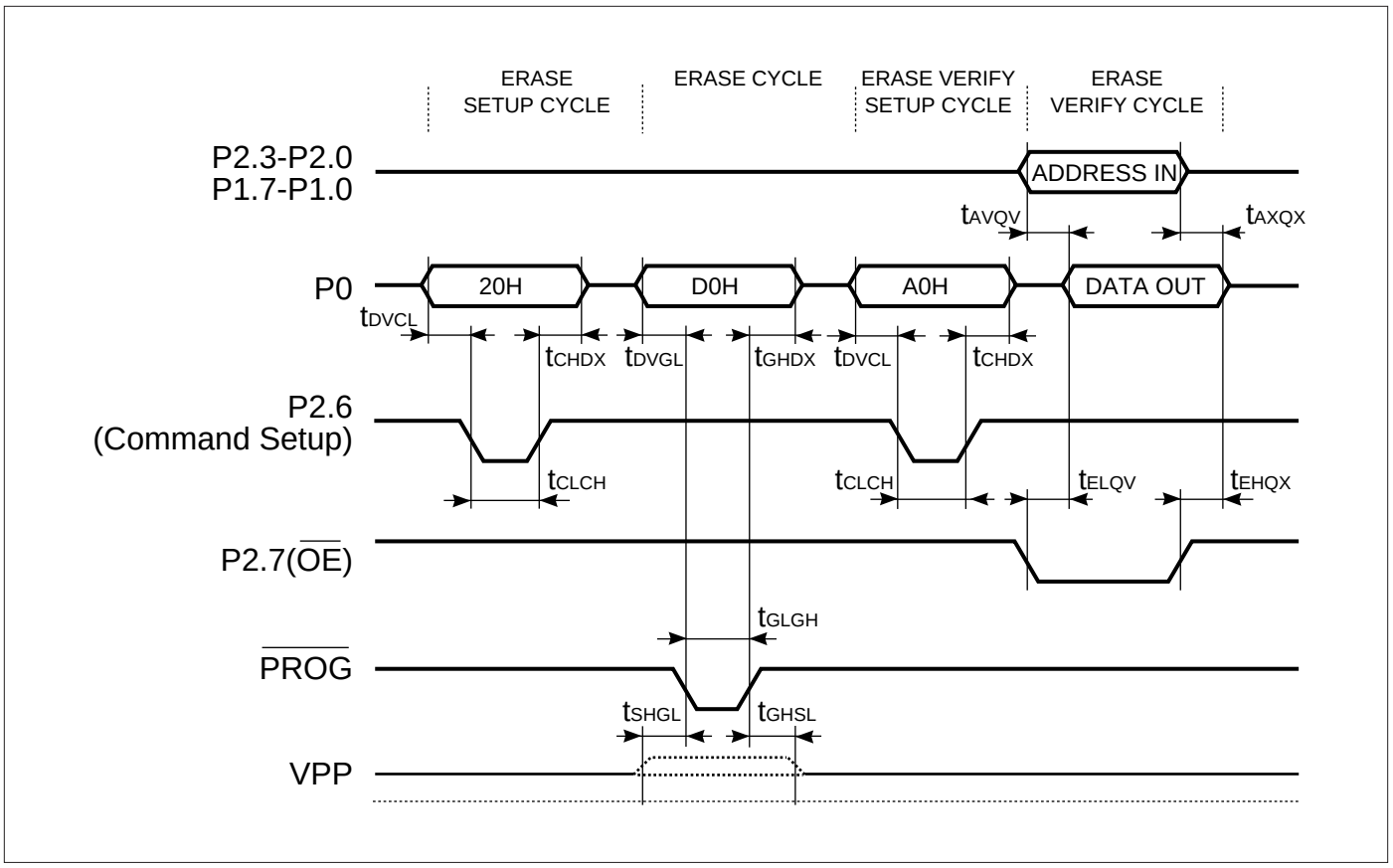


Figure 18. Erase Timing Waveform

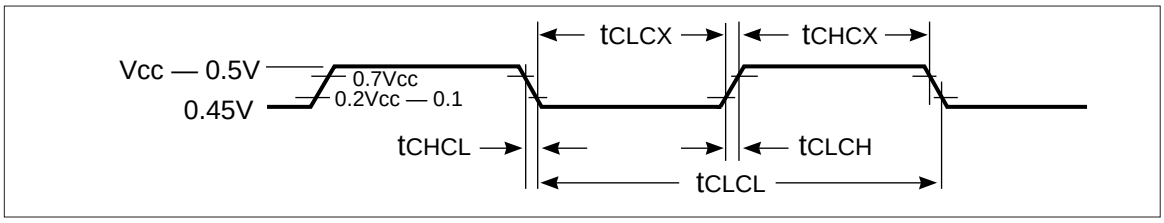


Figure 19. External Clock Drive Waveform

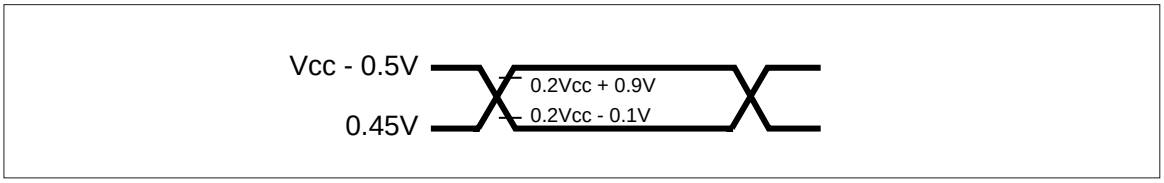


Figure 20. AC Test Point

Note:

1.AC inputs during testing are driven at Vcc-0.5v for logic “1” and 0.45V for logic “0”.

Timing measurements are made at Vih min for logic “1” and max for logic “0”.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
12 MHz	IC89LV52(51)A-12PL	PLCC
	IC89LV52(51)A-12W	600mil DIP
	IC89LV52(51)A-12PQ	PQFP
24 MHz	IC89LV52(51)A-24PL	PLCC
	IC89LV52(51)A-24W	600mil DIP
	IC89LV52(51)A-24PQ	PQFP

Integrated Circuit Solution Inc.
HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.
TEL: 886-3-5780333
Fax: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.
TEL: 886-2-26962140
FAX: 886-2-26962252
http://www.icsi.com.tw