



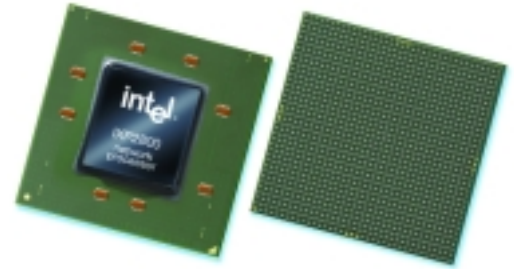
Intel® in
Communications

Intel® IXP2800 Network Processor

For OC-192/10 Gbps network edge
and core applications

Product Highlights

- Delivers 10 Gbps packet forwarding and traffic management on a single chip
- Introduces Hyper Task Chaining processing technology that enables deep packet inspection via software pipelining at line rate
- 16 fully programmable multi-threaded microengines support 23.1 giga-operations per second
- Integrates high-performance, low-power 32-bit Intel® XScale™ core for processing complex algorithms, route table maintenance, and system-level management functions
- Supports 60 million enqueue/dequeue packet operations per second, enabling deep packet processing of minimum 46-byte Packet-over-Sonet (PoS) packets with no loss of performance
- Supports standards-based interfaces for easy integration
- Comprehensive development environment, including Software Developers Kit, contains software tools, libraries and APIs and hardware development platform for rapid product development and prototyping
- Broad range of complementary technology from third-party software, silicon and board vendors for rapid time-to-market
- Low power consumption and small package size reduce system cost
- Intel® Internet Exchange Architecture (Intel® IXA) technology enables customers to reuse investments in Intel® network processors and software



faces for easy component integration and the ability to leverage software investments by reusing code can dramatically speed time-to-market and lower development costs.

The Intel® IXP2800 network processor is a member of Intel's second-generation network processor family. Based on the first-generation Intel® IXP1200, the IXP2800 is a programmable network processor that integrates a high-performance parallel processing design on a single chip for processing complex algorithms, deep packet inspection, traffic management, and forwarding at wire speed. Its store-and-forward architecture combines a high-performance Intel® XScale™ core with sixteen 32-bit independent multi-threaded microengines that cumulatively provide more than 23.1 giga-operations per second. The microengines provide the processing power to perform tasks that traditionally required expensive high-speed ASICs.

Intel's second-generation network processors are the first implementation of Intel's Hyper Task Chaining technology. This unique network processing approach allows a single stream packet/cell processing problem to be decomposed into multiple, sequential tasks that can be easily linked together. The hardware design uses fast and flexible sharing of data and event signals among threads and microengines to manage data-dependent operations among multiple parallel processing stages with low latency. Through this combination of flexible software pipelining and fast inter-process communication, Hyper Task Chaining delivers rich processing capability at OC-192/10 Gbps line rates. The Intel IXP2800 network processor delivers this enhanced performance with the programmability designed to speed the

(continued)

Product Overview

Equipment designed for network edge and core applications requires high levels of processing performance to support value-added network services at OC-192/10 Gbps line rates. While rapidly adding these new services, network equipment vendors must continue to minimize development time and cost. To support these services and to extend time-in-market network processors must combine performance with highly flexible control of processing resources. In addition, implementation of standards-based inter-

Product Overview *(continued)*

deployment of intelligent network services. A centerpiece of Intel Internet Exchange Architecture (Intel IXA), Intel's second-generation network processor architecture scales to successive generations of networking products and is supported by a common set of development tools, libraries, and example designs. With other Intel network processors, the IXP2800 provides the foundation for a comprehensive development environment that can dramatically accelerate time-to-market, while enabling customers to reuse their investments in software.

Application Flexibility

The ability of the Intel IXP2800 network processor to support OC-192/10 Gbs line rates makes it the optimal solution for a wide variety of high-performance applications such as Metropolitan Area Network (MAN) switches and routers, Internet edge and core switches and routers, multi-service switches, 10 Gbps enterprise switches and routers designed to meet the requirements of advanced data centers, storage area networks (SAN),

and content-aware server off-load/web switches. The network processor's programmability also makes it the right choice for IPSec and Virtual Private Network (VPN) solutions, and wireless infrastructure equipment. Functionality includes:

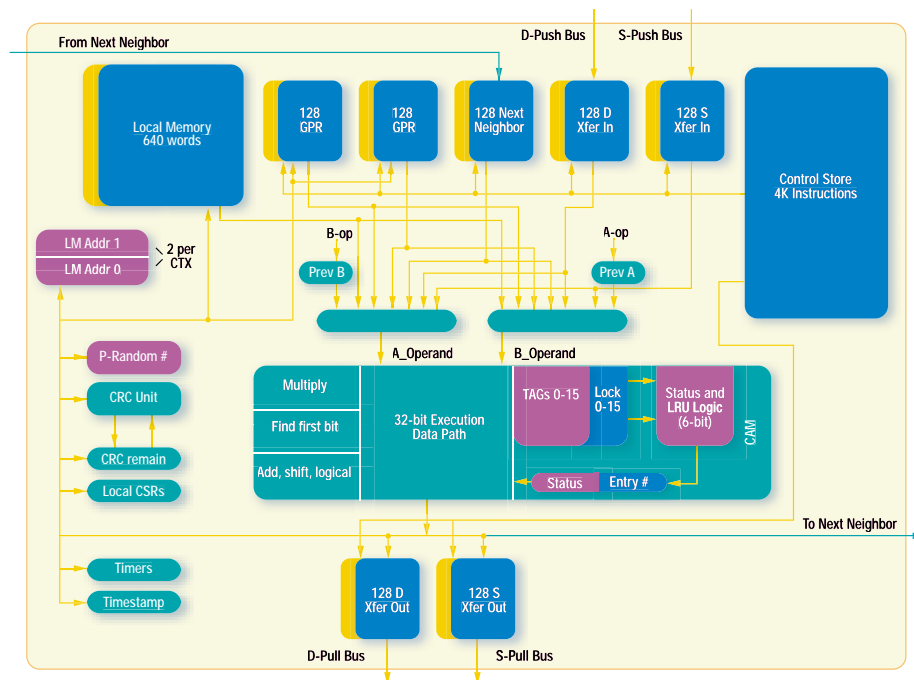
- Ethernet/POS/ATM Layer 4 forwarding in core, MAN and edge applications
- Protocol conversion, forwarding and aggregation for multi-service switches, cable headends and DSLAM aggregation
- ATM SAring and forwarding with advanced traffic shaping
- Content-aware load balancing, forwarding and policing
- Encryption for VPNs and IPSec applications
- GPPS Tunneling Protocol and IPv6 in wireless infrastructure applications
- TCP/IP termination for enterprise data center and SANs
- SSL/TLS acceleration

Features

- 16 integrated programmable microengines with 4K instruction program stores
- Integrated Intel® XScale™ Core
 - 32 Kbyte—Instruction cache
 - 32 Kbyte—Data cache
 - 2 Kbyte—Mini-data cache
- Two unidirectional 16-bit Low Voltage Differential Signaling (LVDS) data interfaces programmable to be SPI-4 Phase 2 or CSIX
- Three industry-standard RDRAM interfaces
- Four industry-standard 32-bit QDR SRAM interfaces
- PCI 2.2 I/O Interface
- 8-bit asynchronous control interface
- Hardware support for memory access queuing
- JTAG support
- Software SDK
- Hardware Development Platform
- Power Performance
- Additional integrated hardware features:
 - Hardware Hash Unit (48, 64, and 128 bit)
 - 16-Kbyte Scratchpad Memory
 - Serial UART port for debug
 - Four general-purpose I/O pins
 - Four 32-bit timers

Benefits

- Enhanced second-generation flexible multi-threaded RISC processors that can be programmed to deliver intelligent transmit and receive processing, with robust software development environment for rapid product development
- Embedded 32-bit RISC core for high-performance processing of complex algorithms, route table maintenance and system-level management functions. Lowers system cost and saves board space
- Supports industry-standard interfaces to media and fabric devices, delivering OC-192 and 10 Gbps Ethernet performance rates; simplifies design and interface to custom ASIC devices
- Memory subsystem to support the network processor store-and-forward processing model
- Memory subsystem for look-up tables and access lists
- Supports industry-standard connection to system host processors
- Provides control interface for connecting to maintenance port of PHY devices and flash memory
- Simplifies product development and reduces system cost
- Improve hardware debug ability
- Improves time-to-market via robust hardware and software development tools
- ~18 Watts typical, ~25 Maximum @ 1.4 GHz operation
- ~15 Watts typical, ~22 Maximum @ 1.0 GHz operation
- Simplifies development, reduces development cost, and saves board space



Microengine Version 2

Development Environment

Intel provides a comprehensive development environment that enables customers to rapidly develop applications for the Intel IXP2800 network processor and migrate existing applications from the IXP1200 network processor family. The development environment includes the Intel® Internet Exchange Architecture Software Developers Kit (Intel® IXA SDK) 3.0, complemented by a hardware development platform with supporting software and tools.

The Intel IXA SDK 3.0 enables hardware and software engineering to proceed in parallel. The SDK provides the software team with an easy-to-use graphical simulation environment for developing, debugging, and optimizing a network application at the same time that the hardware team is working on design and prototyping the device. By using the development tools, network building blocks and the Intel® IXA Portability Framework in the SDK, the design team can achieve an unparalleled time-to-market advantage.

Intel IXA SDK 3.0 preserves investments in software for the IXP1200 network processor by maintaining the familiar best-in-class Developer's Workbench programming environment and extending it to support the IXP2400 and IXP2800 network processors. Developers who use the Intel® IXA SDK portable macro library, Intel® Microengine C compiler and the Intel® Microengine C Networking Library and the programming framework with the IXP1200 will be able to retarget their code for the IXP2400 and IXP2800 by using the same or similar facilities in SDK 3.0.

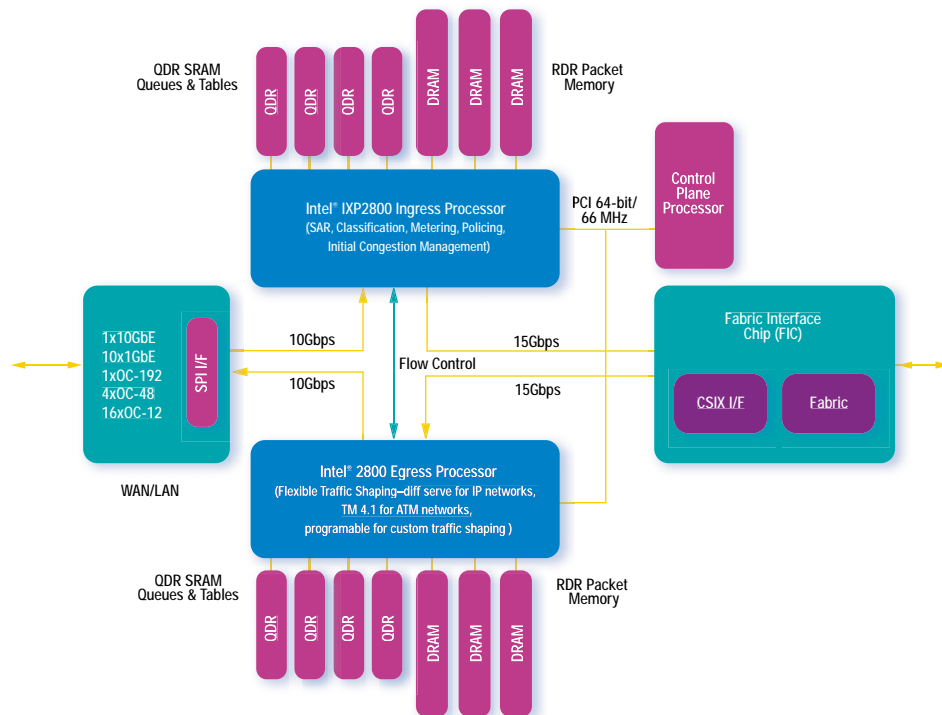
The Microengine Development Environment (Workbench/Transactor) provides an integrated development environment (IDE) for advanced, graphical, cycle-accurate

simulation, profiling, and debugging. It enables faster prototyping, intuitive optimization and fast time-to-market development of networking applications for the highly parallel, multi-threaded second-generation microengine architecture. The Transactor can be used to solve concurrency issues by simulating packets going into and out of the network processor, and it enables detailed visualization of processes and events within the network processor.

The Transactor identifies opportunities for code optimization by capturing history and statistics that show cycle-by-cycle interactions among the threads and memory units. The Transactor also includes a scripting engine for setting test configurations and creating test cases. Simulation tools include queue, memory, and thread histories which show memory and processor utilization, memory reference latencies, and queue depths.

The SDK provides high-level tools, an embedded real-time operating system, the Intel® IXA software portability framework and libraries to enable customers to evaluate, demonstrate, and tune performance of the network processor to meet product requirements.

The hardware development platform is comprised of an industry-standard form factor chassis, Intel IXP2800 base board, and a choice of modular media cards for maximum design flexibility. Complementary silicon and coprocessors will also be available from Intel or third parties. These components will be designed to work together to provide the flexibility, scalability, and performance levels required to meet the demands of tomorrow's high-performance networks.



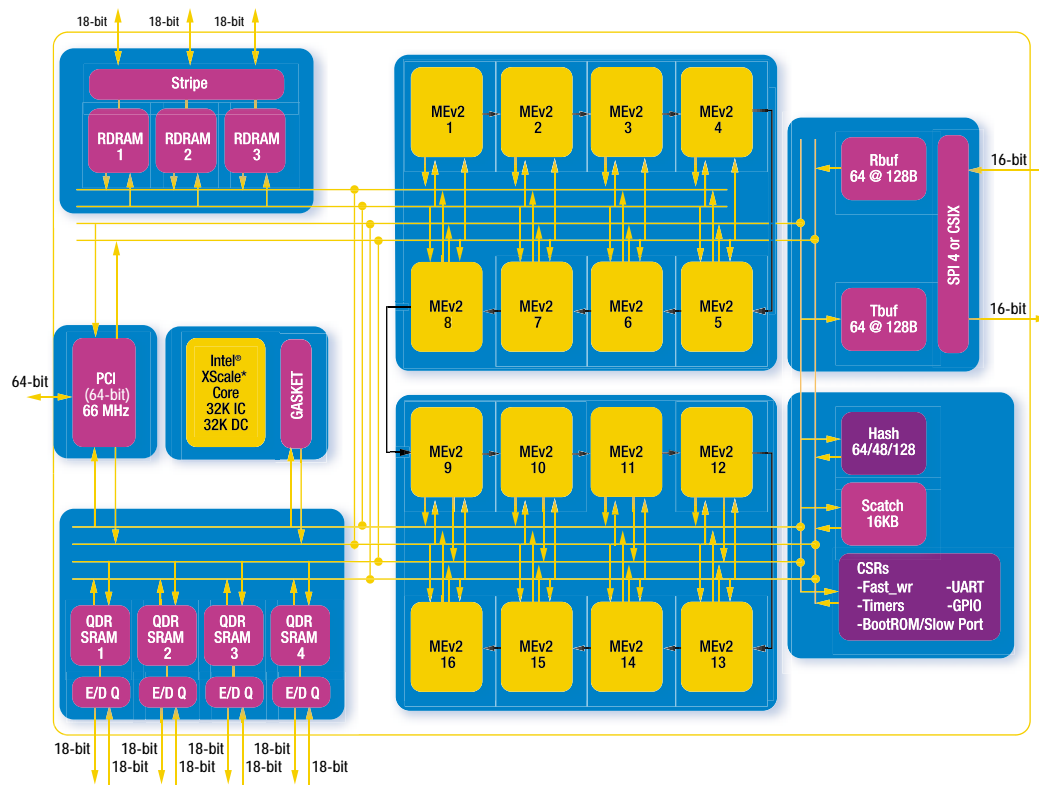
Multiple LAN/WAN configurations with the IXP2800 network processor

This diagram highlights a number of different LAN and WAN design configurations that can be implemented with the Intel® IXP2800 network processor in half-duplex mode. The IXP2800 features standard interfaces and has the ability to add a TCAM off the QDR SRAM interface to support multi-field searches.

Description

Specification

<ul style="list-style-type: none"> Microengine operating frequency 	<ul style="list-style-type: none"> 1.4 GHz, 1.0 GHz 32-bit data path
<ul style="list-style-type: none"> Microengine program control stores 	<ul style="list-style-type: none"> 4K Instructions
<ul style="list-style-type: none"> SPI-4 Phase 2 Operation 	<ul style="list-style-type: none"> 311–500 MHz (622–1,000 MTs) 16 bit LVDS (dual-edge) signaling
<ul style="list-style-type: none"> CSIX switch fabric interface 	<ul style="list-style-type: none"> 311–500 MHz (622–1,000 MTs) 16 bit LVDS (dual-edge) signaling
<ul style="list-style-type: none"> Intel® XScale™ core operating frequency 	<ul style="list-style-type: none"> 700 MHz, 500 MHz/32-bit data path
<ul style="list-style-type: none"> PCI interface 	<ul style="list-style-type: none"> 64 bit/66 MHz
<ul style="list-style-type: none"> SRAM interface (QDR) Four Channels 	<ul style="list-style-type: none"> Peak bandwidth of 1.6 Gbytes/sec per channel using 200 MHz SRAMs (800-Mbytes/sec read, 800-Mbytes/sec write)
<ul style="list-style-type: none"> RDRAM Three Channels 	<ul style="list-style-type: none"> Peak bandwidth 1.6 Gbytes/sec (12.8 Gbs) per channel (support 800- & 1,066-MHz RDRAM)
<ul style="list-style-type: none"> Operating temperature at 1.4 GHz Operating temperature at 1.0 GHz 	<ul style="list-style-type: none"> 0° to 70° C ambient -40° to 85° C; 0° to 70° C ambient
<ul style="list-style-type: none"> Power supply 	<ul style="list-style-type: none"> Vdd=1.35 V±5%
<ul style="list-style-type: none"> Power dissipation 	<ul style="list-style-type: none"> ~18 Watts typical, ~25 Maximum @ 1.4 GHz operation ~15 Watts typical, ~22 Maximum @ 1.0 GHz operation
<ul style="list-style-type: none"> Package 	<ul style="list-style-type: none"> 1356 Ball FCBGA 37.5 mm x 37.5 mm
<ul style="list-style-type: none"> Solder ball pitch 	<ul style="list-style-type: none"> 1 mm



Intel® IXP2800 Network Processor Block Diagram

Hyper Task Chaining

Hyper Task Chaining implements several significant innovations to ensure low latency communication among processes. These mechanisms include Next Neighbor registers, which enable individual microengines to rapidly pass data and state information to adjacent microengines. Reflector Mode pathways ensure that data and global event signals can be shared with multiple microengines, using 32 bit, unidirectional buses that connect the IXP2800 network processor's internal processing and memory resources. A third enhancement, Ring Buffer registers, provides a highly efficient mechanism for flexibly linking tasks among multiple software pipelines. Ring buffers allow developers to establish "producer-consumer" relationships among microengines, efficiently propagating results along the pipeline in FIFO order. To minimize latency associated with external memory references, register structures are complemented by 16 entries of Content Addressable Memory (CAM) associated with each microengine. Configured as a distributed cache, the CAM enables multiple threads and microengines to manipulate related data simultaneously while maintaining data coherency.

Second-generation Hardware Enhancements

In addition to Hyper Task Chaining, the Intel IXP2800 also implements additional, hardware-assisted features to increase performance and simplify development. These enhancements provide flexible, easy-to-use mechanisms to support a variety of complex packet/cell processing requirements, freeing developers to focus upon implementing their own unique features. In addition to local memory to improve processing performance, the IXP2800 includes built-in resources for tasks such as ATM Segmentation and Reassembly; pseudo-random number generation for table lookups; time stamps to support flow metering; and a multiply function for complex algorithm calculations such as Quality of Service. In addition, the network processor automates packet manipulation for byte alignment to improve developer productivity and streamline code flows.

Intel® Internet Exchange Architecture

Intel® IXA is a packet processing architecture that provides a foundation for software portability across multiple generations of network processors. Intel IXA is based on programmable microengine technology, the Intel XScale technology, and the Intel® IXA portability framework. Additional information on Intel IXA is available at www.intel.com/design/network/ixa.

Intel Access

Developer's Site	http://developer.intel.com/
Network Processor Web Site	http://www.intel.com/design/network.htm
Intel® Internet Exchange Architecture	http://www.intel.com/ixa.htm
Intel® in Communications	http://www.intel.com/communications/
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