PRELIMINARY

Integrated Circuit Systems, Inc.

ICS87972I

LOW SKEW, 1-TO-12 LVCMOS CLOCK MULTIPLIER/ZERO DELAY BUFFER

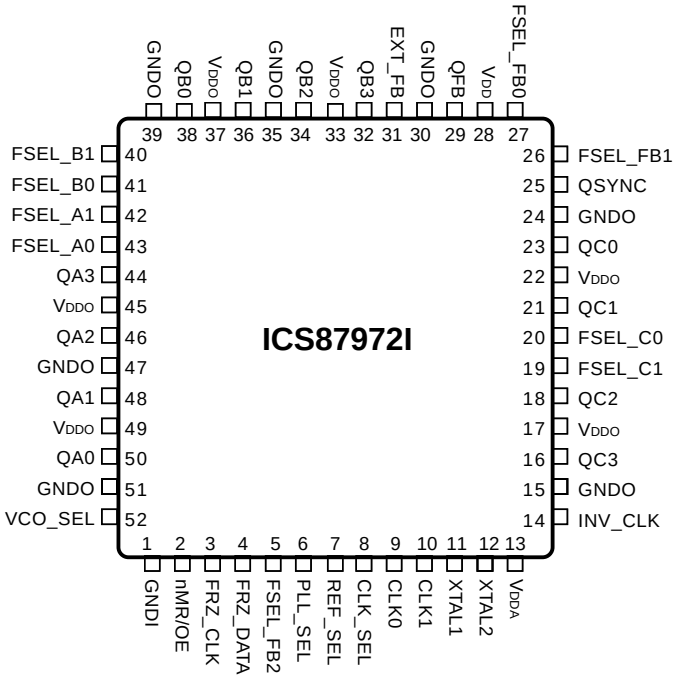
GENERAL DESCRIPTION

The ICS87972I is a low voltage, low skew, LVCMOS clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87972I has selectable CLK0, CLK1 or crystal inputs. The CLK0, CLK1 inputs accept LVCMOS or LVTTL input levels.

FEATURES

- Fully integrated PLL
- 14 LVCMOS outputs; (12) clocks, (1) feedback, (1) sync
- Selectable crystal oscillator interface or LVCMOS reference clock inputs
- CLK0, CLK1 can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 125MHz
- Output skew: 550ps (maximum)
- Cycle-to-cycle jitter: ±100ps (typical)
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Pin compatible with MPC972
- Compatible with PowerPC™ and Pentium™ Microprocessors

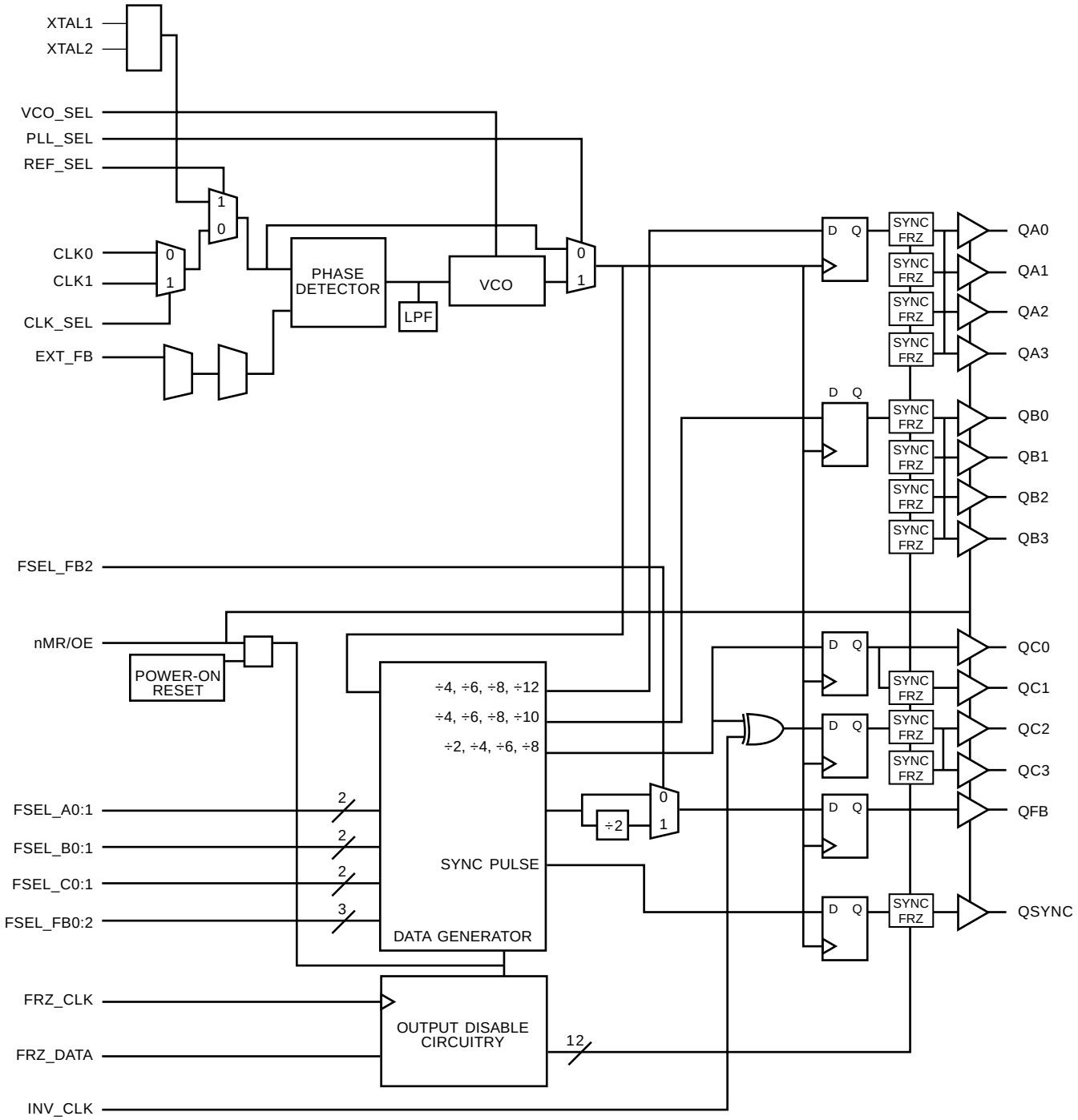
PIN ASSIGNMENT



52-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

BLOCK DIAGRAM



SIMPLIFIED BLOCK DIAGRAM

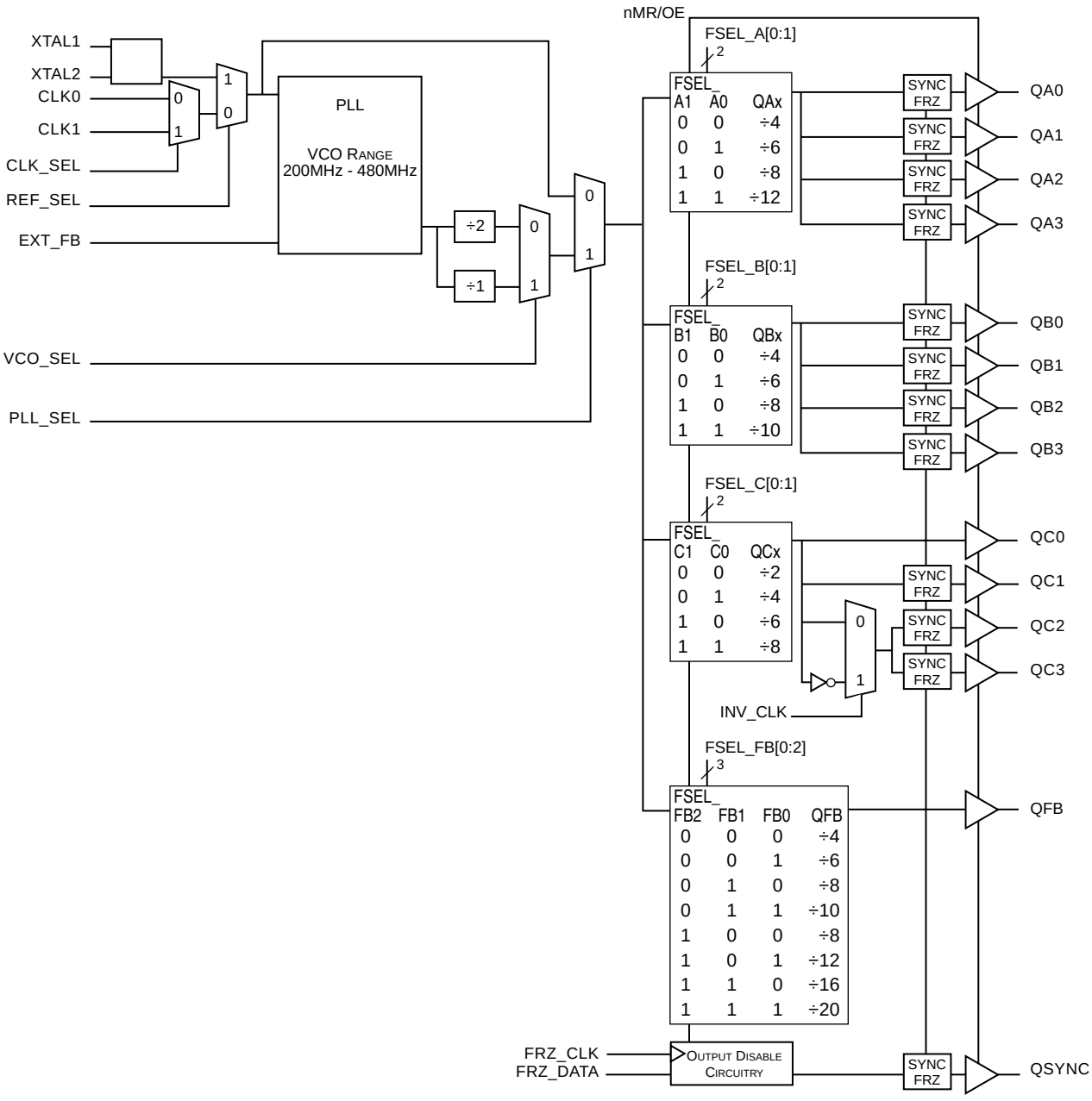


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	GNDI	Power		Power supply ground.
2	nMR/OE	Input	Pullup	Master reset and output enable. When HIGH, enables the outputs. When LOW, resets the outputs to tristate and resets output divide circuitry. Enables and disables all outputs. LVCMOS / LVTTL interface levels.
3	FRZ_CLK	Input	Pullup	Clock input for freeze circuitry.
4	FRZ_DATA	Input	Pullup	Configuration data input for freeze circuitry.
5, 26, 27	FSEL_FB2, FSEL_FB1, FSEL_FB0	Input	Pullup	Select pins control Feedback Divide value.
6	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL. LVCMOS / LVTTL interface levels.
7	REF_SEL	Input	Pullup	Selects between crystal and reference clock. When LOW, selects CLK0 or CLK1. When HIGH, selects crystal inputs. LVCMOS / LVTTL interface levels.
8	CLK_SEL	Input	Pullup	Clock select input. When LOW, selects CLK0. When HIGH, selects CLK1. LVCMOS / LVTTL interface levels.
9, 10	CLK0, CLK1	Input	Pullup	Reference clock inputs. LVCMOS / LVTTL interface levels.
11, 12	XTAL1, XTAL2	Input		Crystal oscillator inputs.
13	V_{DDA}	Power		Analog supply pin.
14	INV_CLK	Input	Pullup	Inverted clock select for QC2 and QC3 outputs.
15, 24, 30, 35, 39, 47, 51	GNDO	Power		Power supply ground.
16, 18, 21, 23	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
17, 22, 33 37, 45, 49	V_{DDO}	Power		Output supply pins.
25	QSYNC	Output		See Figure 1, Timing Diagrams.
28	V_{DD}	Power		Positive supply pins.
29	QFB	Output		Feedback clock output.
31	EXT_FB	Input	Pullup	External feedback. LVCMOS / LVTTL interface levels.
32, 34, 36, 38	QB3, QB2, QB1, QB0	Output		Bank B clock outputs.7Ω typical output impedance. LVCMOS / LVTTL interface levels.
40, 41	FSEL_B1, FSEL_B0	Input	Pullup	Selects pins for Bank B outputs.
42, 43	FSEL_A1, FSEL_A0	Input	Pullup	Selects pins for Bank A outputs.
44, 46, 48, 50	QA3, QA2, QA1, QA0	Output		Bank A clock outputs.7Ω typical output impedance. LVCMOS / LVTTL interface levels.
52	VCO_SEL	Input	Pullup	Selects VCO. When HIGH, selects VCO ÷ 1. When LOW, selects VCO ÷ 2. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDA}, V_{DD}, V_{DDO} = 3.465V		25		pF
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs	Inputs		Outputs	Inputs		Outputs
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

TABLE 3B. FEEDBACK CONFIGURATION SELECT FUNCTION TABLE

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

TABLE 3C. CONTROL SELECT FUNCTION TABLE

Inputs		
Control Pin	Logic 0	Logic 1
VCO_SEL	VCO/2	VCO
REF_SEL	CLK0 or CLK1	XTAL
CLK_SEL	CLK0	CLK1
PLL_SEL	BYPASS PLL	Enable PLL
nMR/OE	Master Reset/Output Hi Z	Enable Outputs
INV_CLK	Non-Inverted QC2, QC3	Inverted QC2, QC3

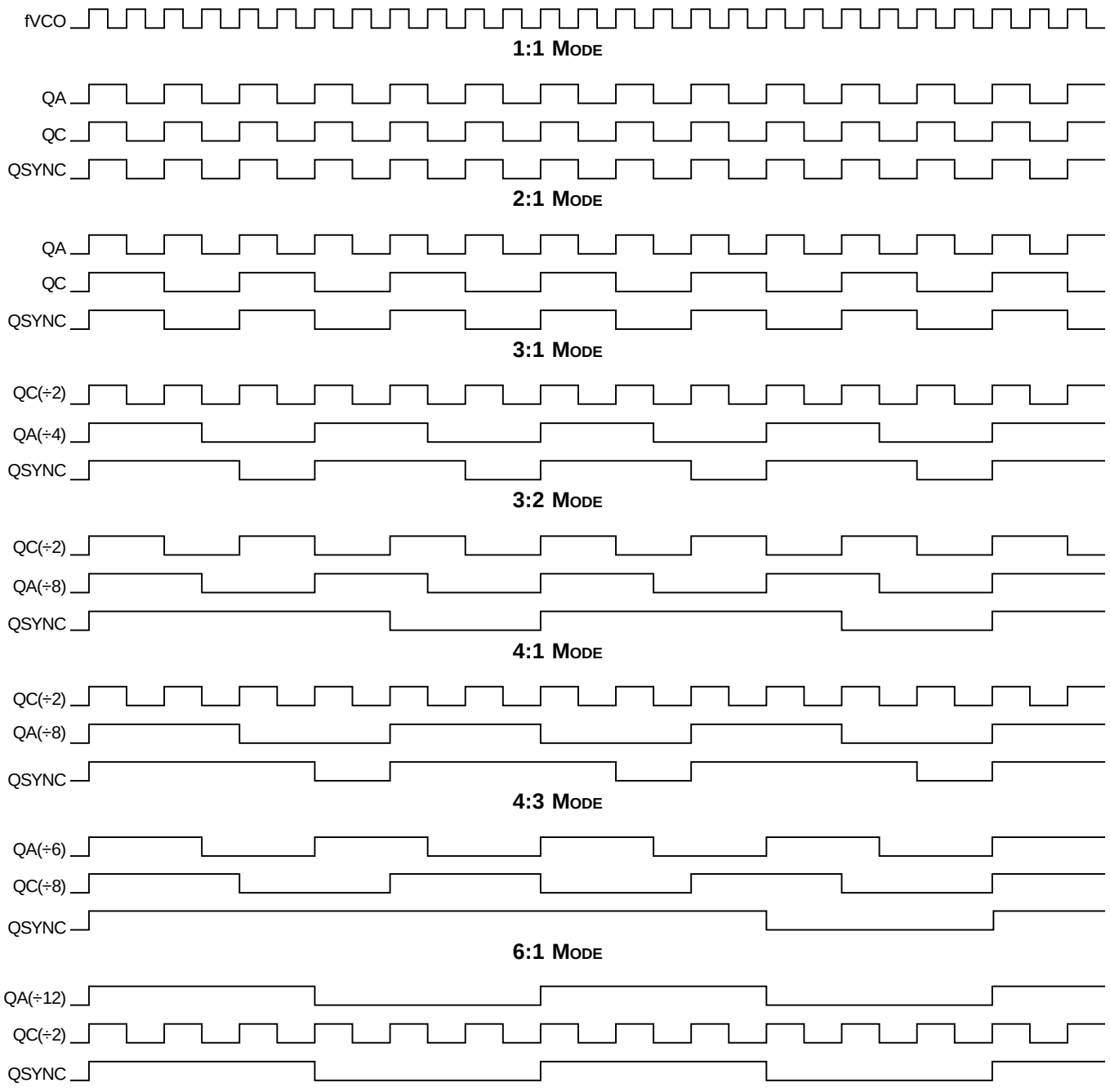


FIGURE 1 - TIMING DIAGRAMS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Positive Supply Current	All power pins			215	mA
I_{DDA}	Analog Supply Current				20	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		3.6	V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current				±120	µA
V_{OH}	Output High Voltage; NOTE 1		2.4			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK0, CLK1; NOTE 1				120	MHz
		XTAL1, XTAL2		10		25	MHz
		FRZ_CLK				20	MHz

NOTE 1: Input frequency depends on Feedback divide ratio to ensure the clock * Feedback Divide is in the VCO range of 200MHz - 480MHz.

TABLE 6. CRYSTAL CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

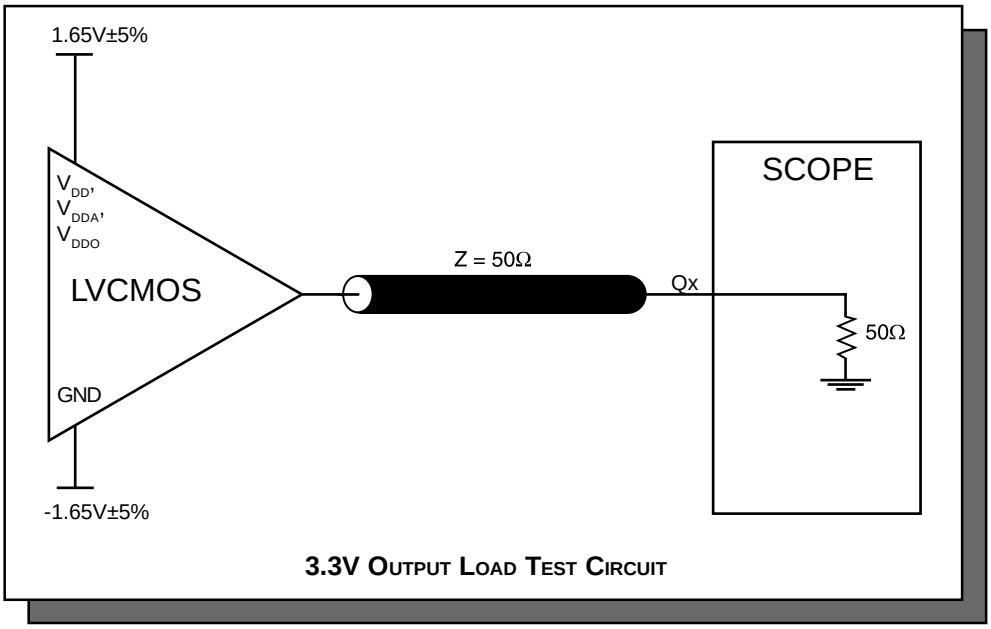
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF

TABLE 7. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

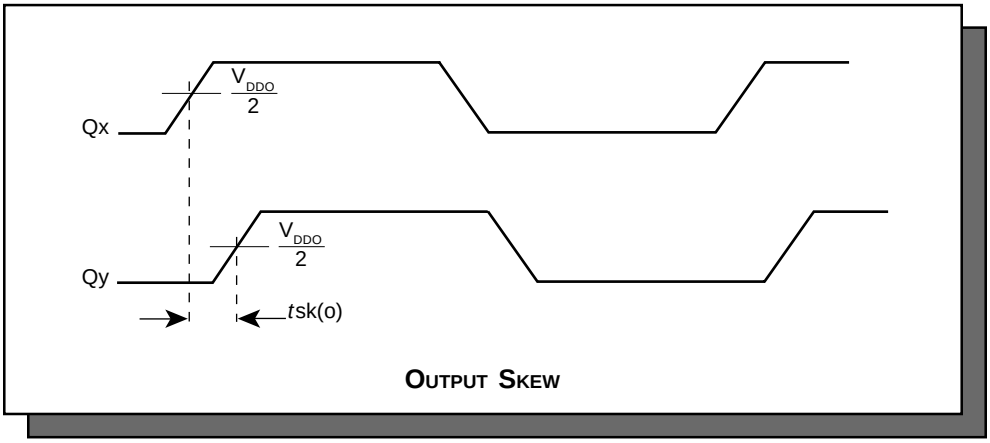
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		÷2			125	MHz
			÷4			120	MHz
			÷6			80	MHz
			÷8			60	MHz
t(Ø)	Static Phase Offset; NOTE 1	CLK0	QFB ÷ 8	TBD - 400	TBD	TBD + 400	ns
		CLK1	QFB ÷ 8	TBD - 400	TBD	TBD + 400	ns
*t*sk(o)	Output Skew; NOTE 2, 4					550	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4				±100		ps
f_{VCO}	PLL VCO Lock Range			200		480	MHz
t_{LOCK}	PLL Lock Time					10	ms
t_R	Output Rise Time; NOTE 3		0.8V to 2V	0.15		1.2	ns
t_F	Output Fall Time; NOTE 3		0.8V to 2V	0.15		1.2	ns
t_{PW}	Output Pulse Width			tCycle/2 - 750	tCycle/2±500	tCycle/2 + 750	ps
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 3					10	ns
t_{PLZ}, t_{PHZ}	Output Disable TIme; NOTE 3					8	ns

All parameters measured at 125MHz unless noted otherwise.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

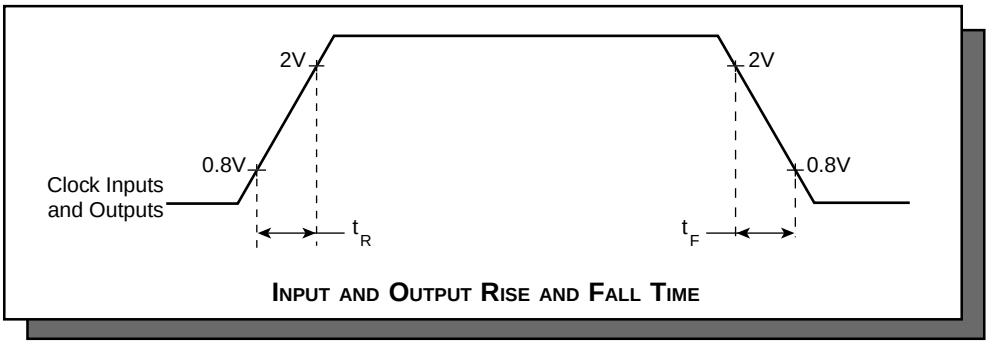
PARAMETER MEASUREMENT INFORMATION



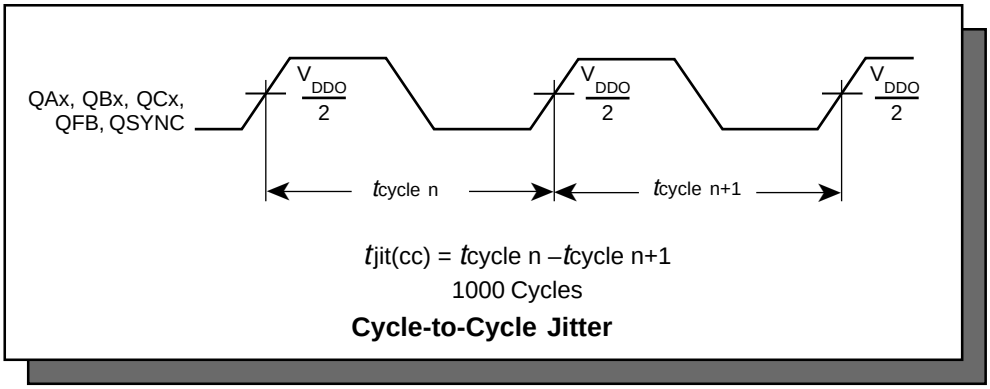
3.3V OUTPUT LOAD TEST CIRCUIT



OUTPUT SKEW



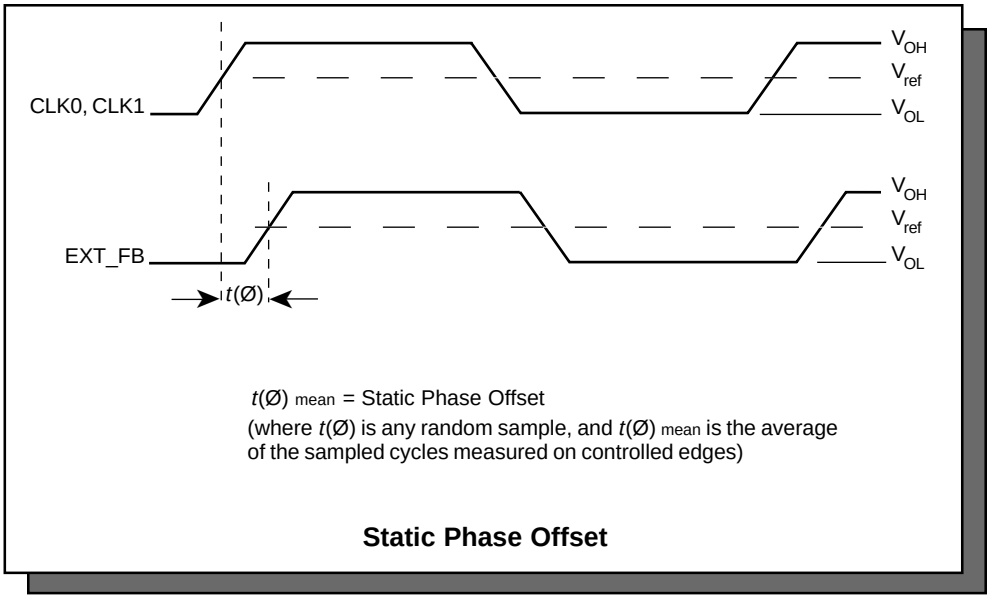
INPUT AND OUTPUT RISE AND FALL TIME



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

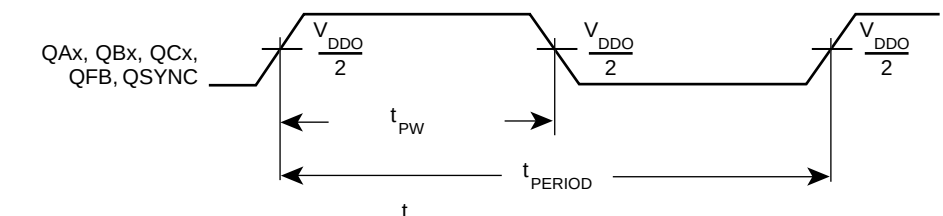
1000 Cycles

Cycle-to-Cycle Jitter



$t(Ø)_{mean}$ = Static Phase Offset
(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

Static Phase Offset



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

t_{PW} & t_{PERIOD}

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87972I is: 8364

PACKAGE OUTLINE - Y SUFFIX

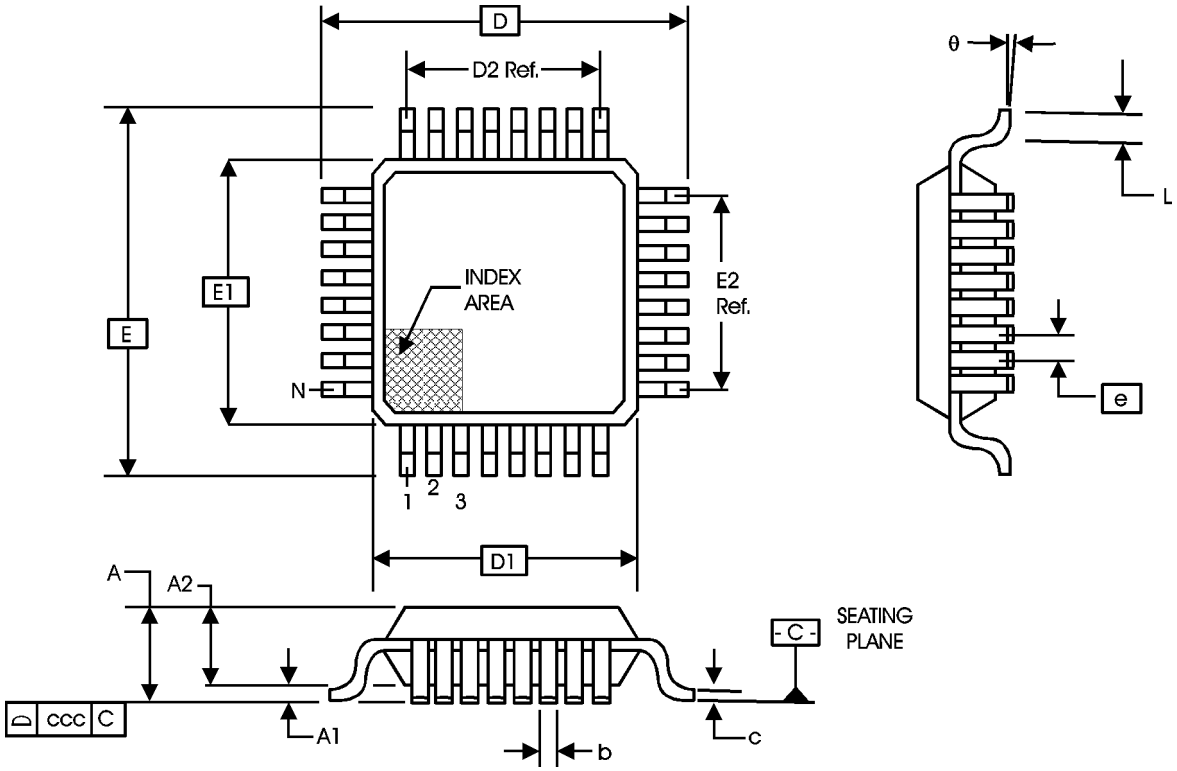


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N		52	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
b1	0.22	0.30	0.33
D		12.00 BASIC	
D1		10.00 BASIC	
E		12.00 BASIC	
E1		10.00 BASIC	
e		0.65 BASIC	
ccc	0.45	--	0.10
ddd	--	--	0.13

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87972BYI	ICS87972BYI	52 Lead LQFP	160 per tray	-40°C to 85°C
ICS87972BYIT	ICS87972BYI	52 Lead LQFP on Tape and Reel	500	-40°C to 85°C