



Integrated
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Systems, Inc.

PRELIMINARY

ICS8520

Low Skew, 1-to-16 DIFFERENTIAL-TO-LVHSTL FANOUT BUFFER

GENERAL DESCRIPTION



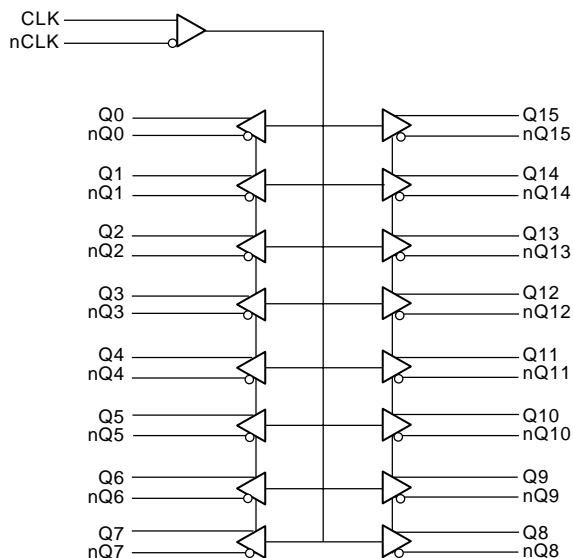
The ICS8520 is a low skew, high performance 1-to-16 Differential-to-LVHSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8520 has 1 clock input pair. The CLK, nCLK pair can accept most standard differential input levels.

Guaranteed output skew, part-to-part skew and crossover voltage characteristics make the ICS8520 ideal for interfacing to today's most advanced microprocessor and static RAMs.

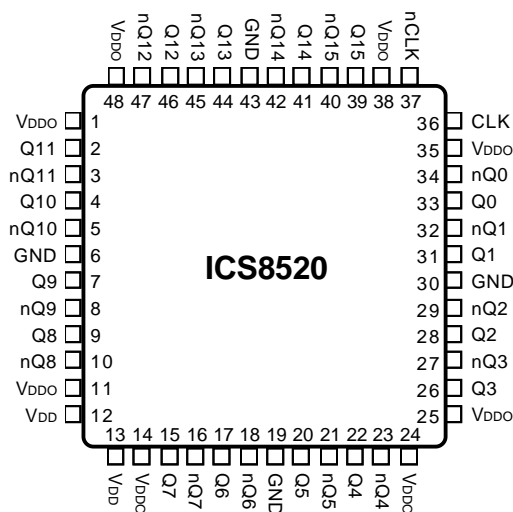
FEATURES

- 16 differential LVHSTL compatible outputs each with the ability to drive 50Ω to ground
- 1 differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 500MHz
- Translates single ended input levels to LVHSTL levels with resistor bias nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.6ns (maximum)
- V_{OH} : 1.2V (maximum)
- 40% of $V_{OH} \leq V_{crossover} \leq 60\%$ of V_{OH}
- 3.3V core, 1.8V output operating supply voltages
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm body package
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 11, 14, 24, 25, 35, 38, 48	V _{DDO}	Power		Output supply pins.
2, 3	Q11, nQ11	Output		Differential output pair. LVHSTL interface levels.
4, 5	Q10, nQ10	Output		Differential output pair. LVHSTL interface levels.
6, 19, 30, 43	GND	Power		Power supply ground.
7, 8	Q9, nQ9	Output		Differential output pair. LVHSTL interface levels.
9, 10	Q8, nQ8	Output		Differential output pair. LVHSTL interface levels.
12, 13	V _{DD}	Power		Positive supply pins.
15, 16	Q7, nQ7	Output		Differential output pair. LVHSTL interface levels.
17, 18	Q6, nQ6	Output		Differential output pair. LVHSTL interface levels.
20, 21	Q5, nQ5	Output		Differential output pair. LVHSTL interface levels.
22, 23	Q4, nQ4	Output		Differential output pair. LVHSTL interface levels.
26, 27	Q3, nQ3	Output		Differential output pair. LVHSTL interface levels.
28, 29	Q2, nQ2	Output		Differential output pair. LVHSTL interface levels.
36	CLK	Input	Pulldown	Non inverting differential clock input.
37	nCLK	Input	Pullup	Inverting differential clock input.
39, 40	Q15, nQ15	Output		Differential output pair. LVHSTL interface levels.
41, 42	Q14, nQ14	Output		Differential output pair. LVHSTL interface levels.
44, 45	Q13, nQ13	Output		Differential output pair. LVHSTL interface levels.
46, 47	Q12, nQ12	Output		Differential output pair. LVHSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance				4	pF
R _{PULLUP}	Input Pullup Resistor			51		KΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		KΩ

TABLE 3. FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information Section, "Wiring the Differential input to accept single ended levels".



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDX}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				120	mA
I_{DDO}	Output Supply Current					mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK $V_{IN} = V_{DD} = 3.465V$			150	μA
		nCLK $V_{IN} = V_{DD} = 3.465V$			1	μA
I_{IL}	Input Low Current	CLK $V_{IN} = 0V$, $V_{DD} = 3.465V$	-1			μA
		nCLK $V_{IN} = 0V$, $V_{DD} = 3.465V$	-150			μA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Voltage Range; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Common mode voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{DD} + 0.3V$.

TABLE 4C. LVHSTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1		1.2	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		$40\% \times (V_{OH} - V_{OL}) + V_{OL}$		$60\% \times (V_{OH} - V_{OL}) + V_{OL}$	V

NOTE 1: Outputs terminated with 50Ω to ground.



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TABLE 5. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				500	MHz
t_{PD}	Propagation Delay, Low-to-High; NOTE 1	$f \leq 250MHz$	1		1.6	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				50	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

All parameters measured at 250MHz unless noted otherwise

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



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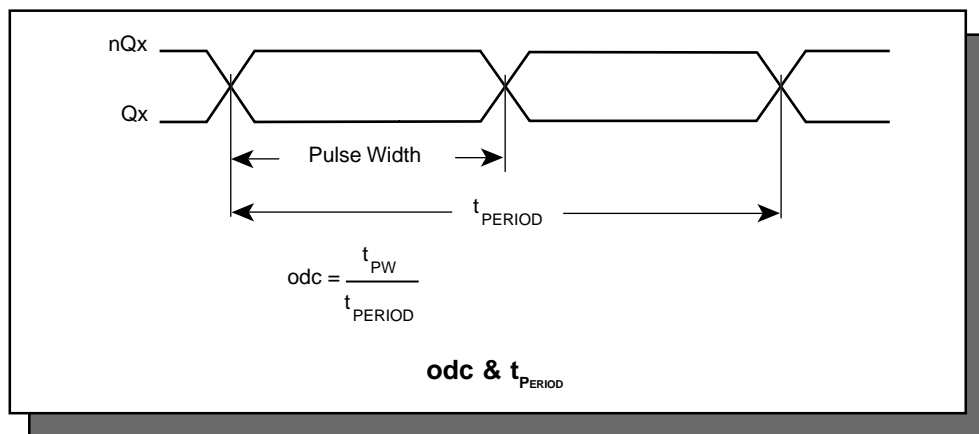
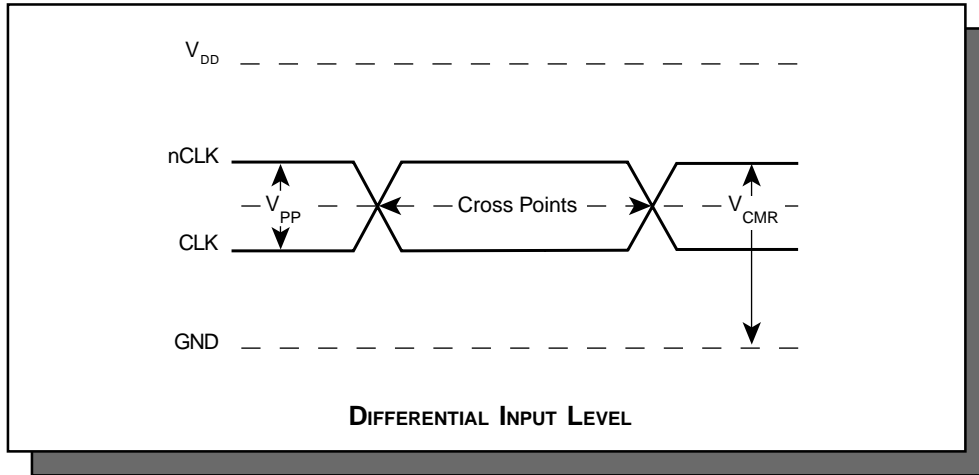
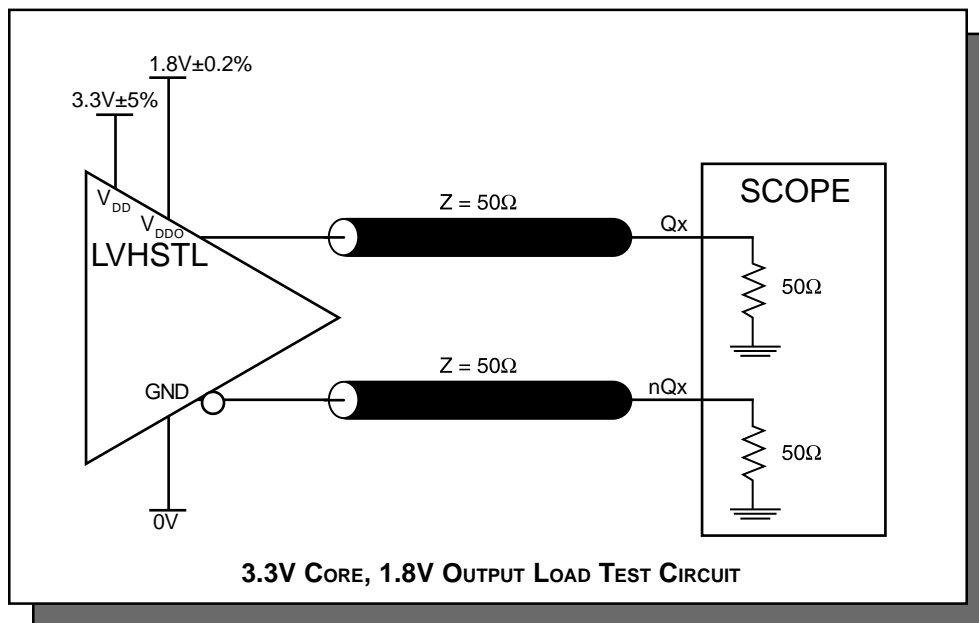
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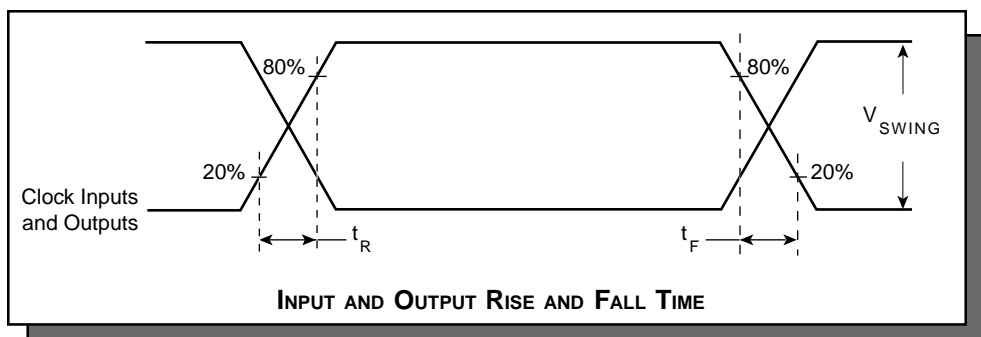
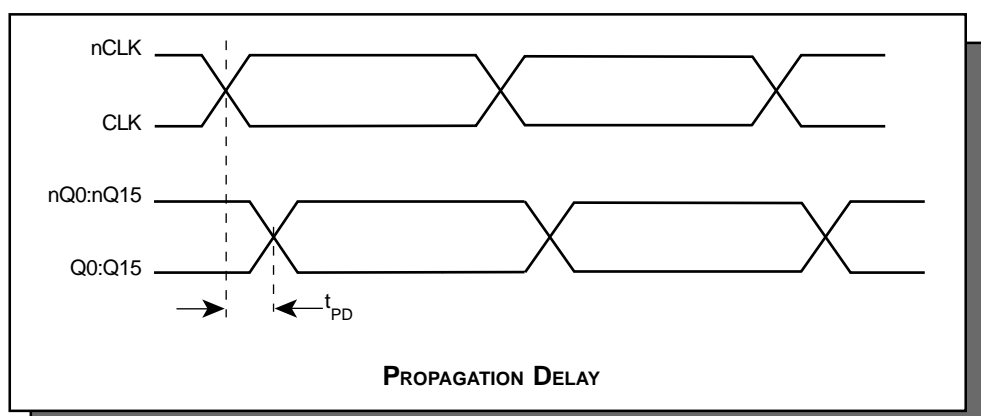
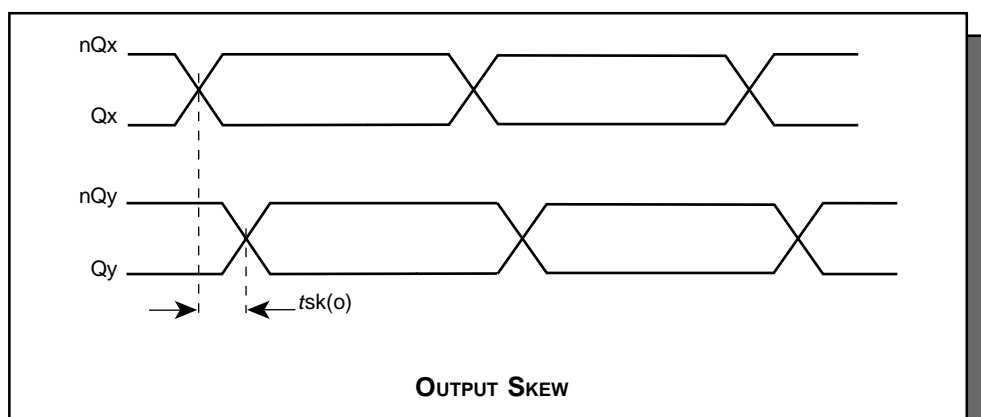
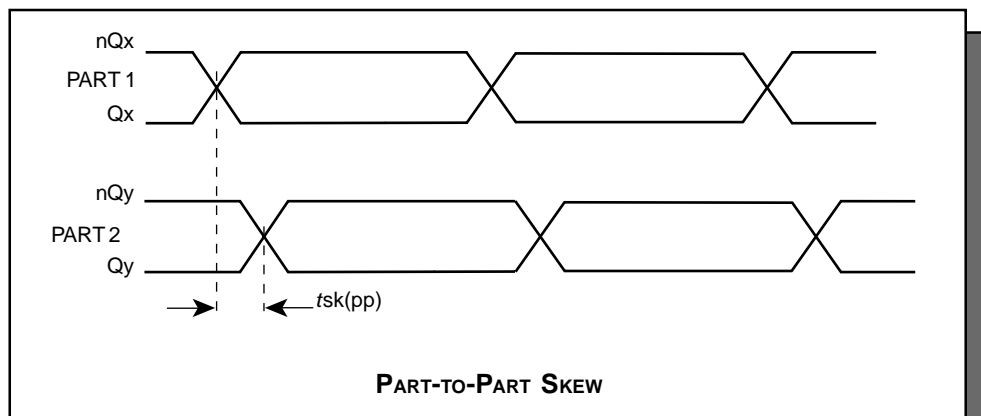
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PARAMETER MEASUREMENT INFORMATION







POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8520. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8520 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 3.465V * 120mA = 416mW$
- Power (outputs)_{MAX} = **32.8mW/Loaded Output pair**
If all outputs are loaded, the total power is $16 \times 32.8mW = 525mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 416mW + 525mW = 941mW$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.941W * 42.1^\circ C/W = 110^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, FORCED CONVECTION

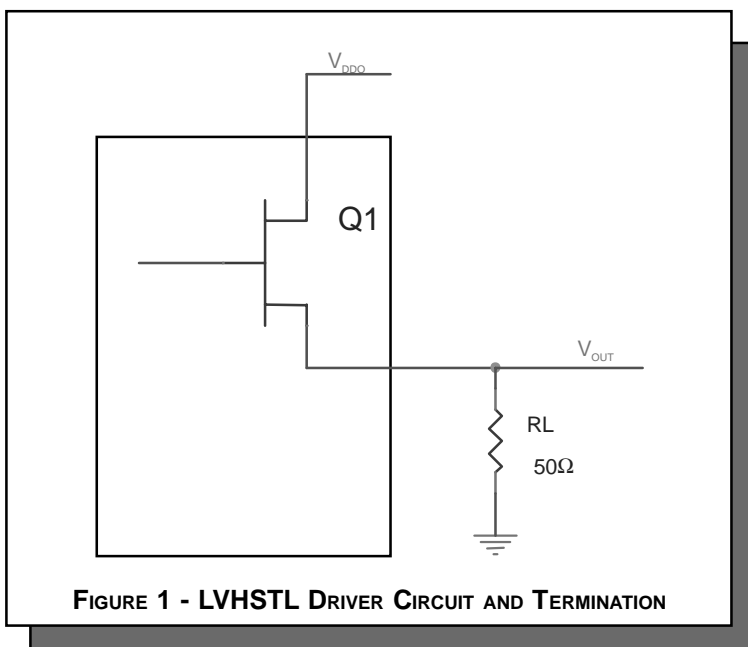
θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 1*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH_MIN} / R_L) * (V_{DDO_MAX} - V_{OH_MIN})$$

$$Pd_L = (V_{OL_MAX} / R_L) * (V_{DDO_MAX} - V_{OL_MAX})$$

$$Pd_H = (1V/50\Omega) * (2V - 1V) = \mathbf{20mW}$$

$$Pd_L = (0.4V/50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{32.8mW}$$



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RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS8520 is: TBD



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PACKAGE OUTLINE - Y SUFFIX

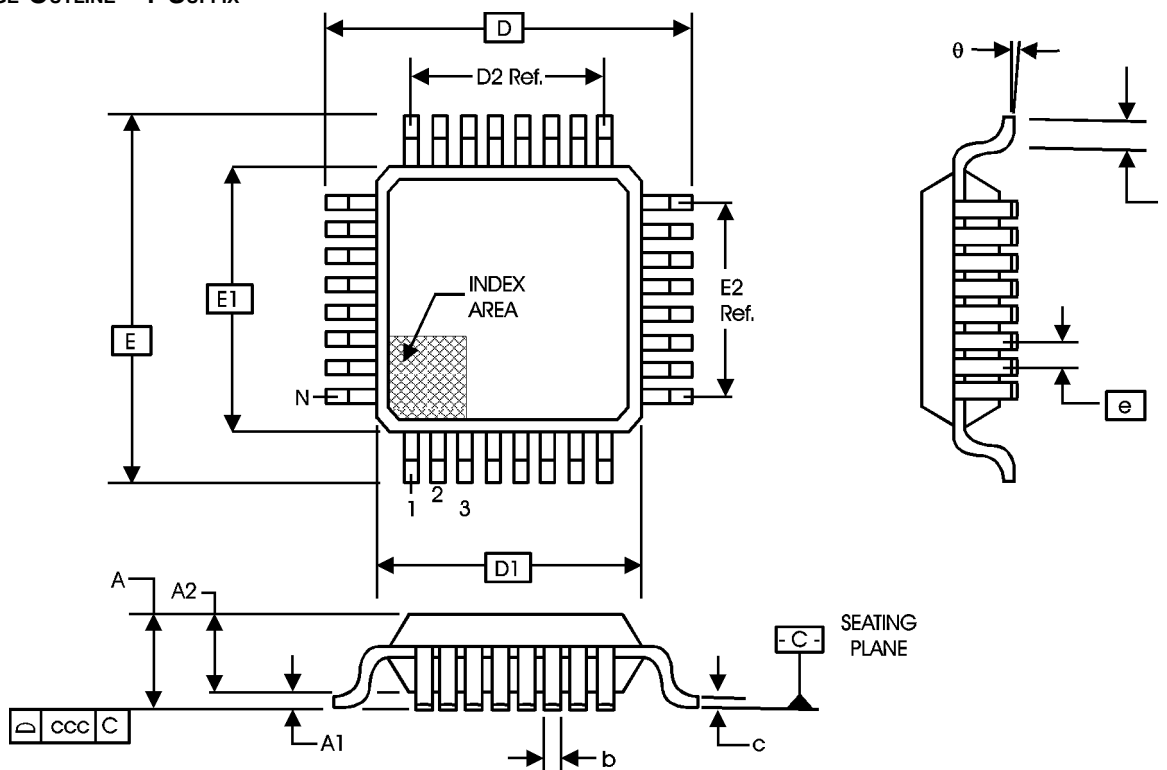


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026



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TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8520DY	ICS8520DY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8520DYT	ICS8520DY	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C

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