ICS525-04
OSCaR™ User Configurable PECL Clock

Description

The ICS525-04 OSCaR™ is the most flexible way to generate a high quality, high accuracy, high frequency differential PECL clock output from a crystal or CMOS clock input. The name OSCaR stands for OSCillator Replacement, as it is designed to replace crystal oscillators in almost any electronic system. The user can easily configure the device to produce nearly any output frequency from any input frequency by grounding or floating the select pins. Neither microcontroller nor software nor device programmer are needed to set the frequency. Using Phase-Locked-Loop (PLL) techniques, the device accepts a crystal or clock to produce output clocks up to 156 MHz at 3.3 V, keeping them frequency locked together.

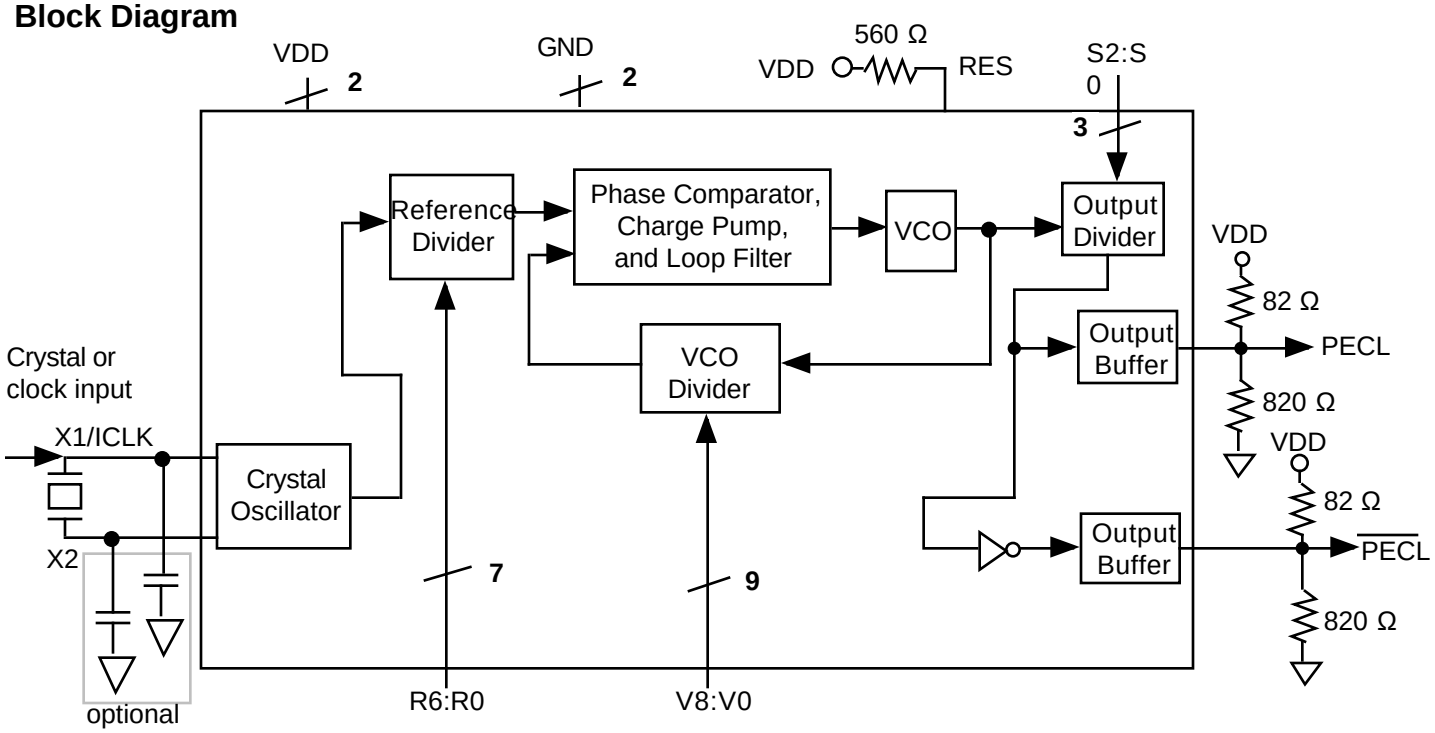
For simple multipliers to produce common frequencies, refer to the LOCO family of parts, which are smaller and more cost effective.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed. For applications which require defined input to output timing, use the ICS527-02.

Features

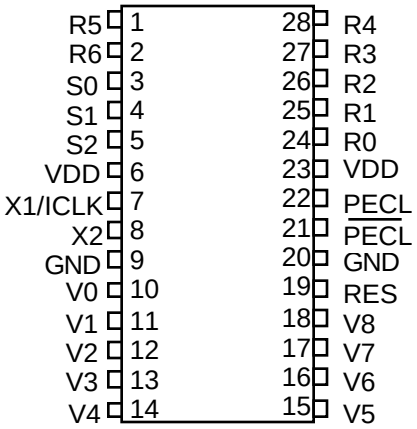
- Packaged as 28 pin SSOP (150 mil body)
- Highly accurate frequency generation
- User determines the output frequency by setting all internal dividers
- Eliminates need for custom oscillators
- No software needed
- Pull-ups on all select inputs
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 156 MHz at 3.3 V
- Very low jitter
- PECL levels set by external resistors
- Operating voltages of 3.3 V or 5 V
- Ideal for oscillator replacement
- Industrial temperature version available
- Advanced, low power CMOS process

Block Diagram



Integrated Circuit Systems, Inc. • 525 Race Street •San Jose• CA • 95126• (408)295-9800tel• www.icst.com

Pin Assignment



Output Divider and Maximum Output Frequency Table

S2	S1	S0	CLK	Max. Output Frequency (MHz)			
pin 5	pin 4	pin 3	Output Divider	VDD = 5V		VDD = 3.3V	
				0-70	-40-+85	0-70	-40-+85
0	0	0	6			26	
0	0	1	2			77	
0	1	0	8			19	
0	1	1	4			39	
1	0	0	5			31	
1	0	1	7			22	
1	1	0	1			156	
1	1	1	3			52	

Pin Description

Pin #	Name	Type	Description
1, 2, 24-28	R5, R6, R0-R4	I(PU)	Reference divider word input pins determined by user. Forms a binary number from 0 to 127.
3, 4, 5	S0, S1, S2	I(PU)	Select pins for output divider determined by user. See table above.
6, 23	VDD	P	Connect to VDD.
7	X1/ICLK	I	Crystal connection. Connect to a parallel resonant crystal, or input clock.
8	X2	I	Crystal connection. Connect to a crystal, or leave unconnected for clock.
9, 20	GND	P	Connect to ground.
10-18	V0-V8	I(PU)	VCO divider word input pins determined by user. Forms a binary number from 0 to 511.
19	RES	I	Bias resistor input. Connect a resistor between this pin and VDD.
21	$\overline{\text{PECL}}$	O	Complementary PECL output. Connect resistor load to this pin.
22	PECL	O	PECL output. Connect resistor load to this pin.

Key: I(PU) = Input with internal pull-up resistor; X1, X2 = Crystal connections; O = Output; P = Power supply connection

Determining (setting) the output frequency

The user has full control in setting the desired output frequency over the range shown in the table on page 2. To replace a standard oscillator, the user should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout, so that the ICS525-04 automatically produces the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports to switch frequencies. By choosing divides carefully, the number of inputs which need to be changed can be minimized. Observe the restrictions on allowed values of VDW and RDW.

The output of the ICS525 can be determined by the following simple equation:

$$\text{PECL frequency} = \text{Input frequency} \bullet \frac{(VDW+8)}{(RDW+2)(OD)}$$

Where Reference Divider Word (RDW) = 0 to 127
VCO Divider Word (VDW) = 0 to 511
Output Divider (OD) = values on page 2

Also, the following operating ranges should be observed:

$$\text{TBD MHz} < \text{Input frequency} \bullet \frac{(VDW+8)}{(RDW+2)} < \text{TBD MHz at 5.0V or} < \text{TBD MHz at 3.3V}$$

See Table on Page 2 for full details of maximum output.

$$200\ \text{kHz} < \frac{\text{Input Frequency}}{(RDW+2)}$$

The dividers are expressed as integers, so that if a 66.66 MHz output is desired from a 14.31818 input, the Reference Divider Word (RDW) should be 59, and the VCO Divider Word (VDW) should be 276, with an Output divider (OD) of 2. In this example, R6:R0 is 0111011, V8:V0 is 100010100, and S2:S0 is 001. Since all of these inputs have pull-up resistors, it is only necessary to ground the zero pins, namely V7, V6, V5, V3, V1, V0, R6, R2, S2, and S1.

To determine the best combination of VCO, reference, and output divider, use the ICS525 Calculator on our Web site: http://www.icst.com. This online form is easy to use and quickly shows you up to three options for these settings.

You may also fax this page to ICS at 408 295 9818(fax), or contact us via our Web site at http://www.icst.com. Be sure to indicate the following:

Your Name _____ Company Name_____ Telephone_____

Respond by e-mail (list your e-mail address) _____or fax number _____

Desired input crystal/clock (in MHz) _____ Desired output frequency_____

VDD = 3.3V or 5V _____

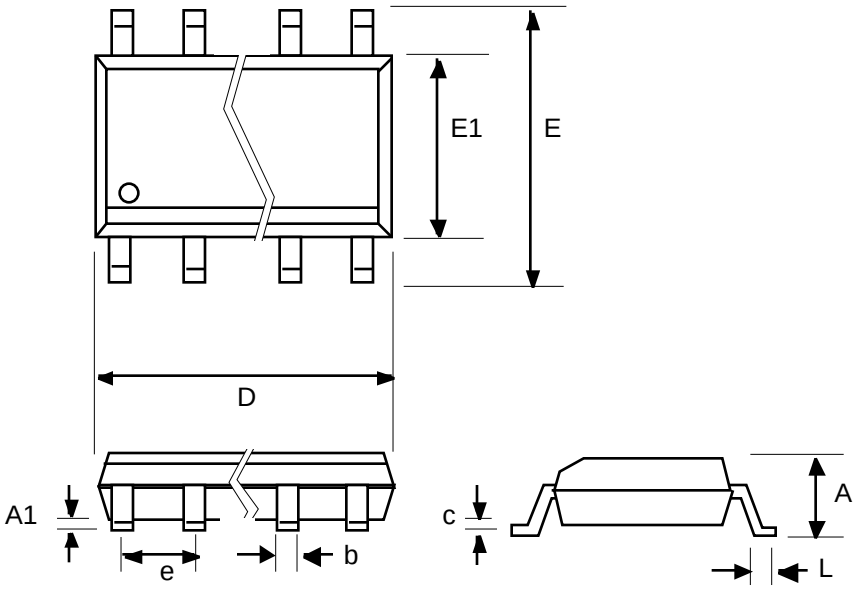
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature	ICS525-01R	0		70	ºC
	ICS525-01RI	-40		85	ºC
Soldering Temperature	Max of 10 seconds			260	ºC
Storage Temperature		-65		150	ºC
DC CHARACTERISTICS (VDD = 3.3 V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Input High Voltage, VIH, X1/ICLK only		(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, X1/ICLK only			VDD/2	(VDD/2)-1	V
IDD Operating Supply Current, 15 MHz crystal	No Load, 60MHz out		TBD		mA
IDD Operating Supply Current, 15 MHz crystal	60MHz out, VDD=5 V		TBD		mA
On-Chip Pull-up Resistor	V, R, S select pins		270		kΩ
Input Capacitance	V, R, S select pins		4		pF
AC CHARACTERISTICS (VDD = 3.3 V unless otherwise noted)					
Input Frequency, crystal input		5		27	MHz
Input Frequency, clock input		2		50	MHz
Output Frequency with OD=2, VDD = 4.5 to 5.	0 C to 70 C	1		TBD	MHz
	-40 C to +85 C	1		TBD	MHz
Output Frequency with OD=2, VDD = 3.0 to 3.	0 C to 70 C	1		TBD	MHz
	-40 C to +85 C	1		TBD	MHz
Absolute Clock Period Jitter	Deviation from mean		±50		ps
One Sigma Clock Period Jitter			20		ps

External Components / Crystal Selection

The ICS525-04 requires two 0.01µF decoupling capacitors to be connected between VDD and GND, one on each side of the chip. They must be connected close to the ICS525-04 to minimize lead inductance. No external power supply filtering is required for this device. A 560 Ω resistor must be connected between RES (pin 19) and VDD. A total of four resistors are needed for the PECL outputs as shown on the block diagram on page 1. The value of these resistors are shown, but they can be varied to change the differential pair output swing, and the common mode voltage. Consult application note MAN09 for more information. The total on-chip capacitance for a crystal is approximately 16 pF, so a parallel resonant, fundamental mode crystal with this value of load (correlation) capacitance should be used. For crystals with a specified load capacitance greater than 16 pF, crystal capacitors may be connected from each of the pins X1 and X2 to Ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = (C_L-16)*2, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions
(For current dimensional specifications, see JEDEC Publication No. 95.)



28 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.102	0.254
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.191	0.254
D	0.386	0.394	9.804	10.008
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.791	6.198
E1	0.150	0.157	3.810	3.988
L	0.016	0.050	0.406	1.270

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS525R-04	ICS525R-04	28 pin narrow SSOP	0 to 70 °C
ICS525R-04T	ICS525R-04	28 pin SSOP on tape and reel	0 to 70 °C
ICS525R-04I	ICS525R-04I	28 pin narrow SSOP	-40 to +85 °C
ICS525R-04IT	ICS525R-04I	28 pin SSOP on tape and reel	-40 to +85 °C