



# ICS525-03 PECL Input OSCaR™ User Configurable Clock

## Description

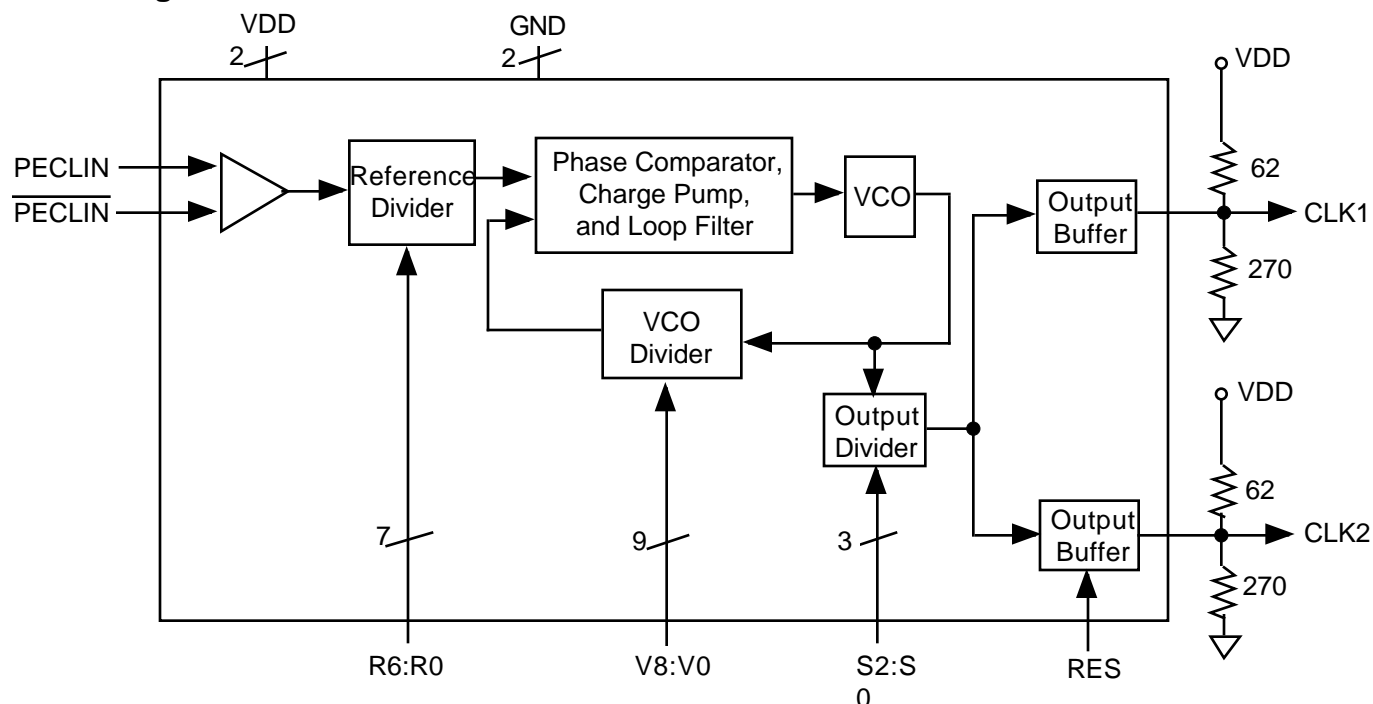
The ICS525-03 OSCaR™ is the most flexible way to generate a high quality, high accuracy, high frequency clock output from a PECL clock input. The name OSCaR stands for OSCillator Replacement, as it is designed to replace crystal oscillators in almost any electronic system. The user can easily configure the device to produce nearly any output frequency from any input frequency by grounding or floating the select pins. Neither microcontroller nor software nor device programmer are needed to set the frequency. Using Phase-Locked-Loop (PLL) techniques, the device accepts a PECL clock to produce output clocks up to 250 MHz, keeping them frequency locked together. Resistors are for PECL outputs only. For simple multipliers to produce common frequencies, refer to the LOCO family of parts, which are smaller and more cost effective.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed.

## Features

- Packaged as 28 pin SSOP (QSOP)
- Highly accurate frequency generation
- User determines the output frequency by setting all internal dividers
- Eliminates need for custom oscillators
- No software needed
- Pull-ups on all select inputs
- Selectable PECL or CMOS outputs
- PECL input clock frequency of 0.5 to 250 MHz
- Output clock frequencies up to 250 MHz
- Very low jitter
- Operating voltages of 3.0 to 5.5V
- 25mA drive capability at TTL levels
- Ideal for oscillator replacement
- Industrial temperature
- Advanced, low power CMOS process

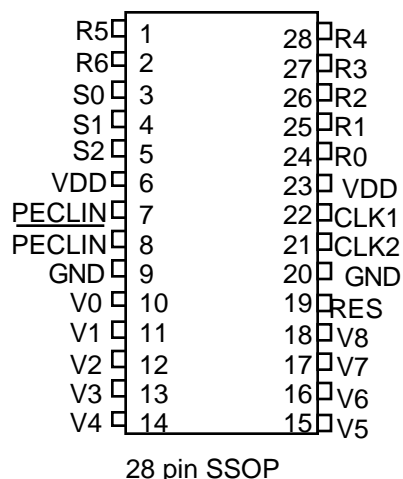
## Block Diagram





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## Pin Assignment



## RES Value Table

RES	CLK1	CLK2	Pre-Divide (P)
0	CMOS	CMOS	2
1.1 k Resistor to VDD	PECL	PECL	1

## Output Divider and Maximum Output Frequency Table

S2	S1	S0	CLK	Max. Output Frequency (MHz)			
pin 5	pin 4	pin 3	Output Divider	VDD = 5V		VDD = 3.3V	
			(OD)	RES=0	RES=1.1 k	RES=0	RES=1.1 k
0	0	0	6	67	34	40	20
0	0	1	2	200	100	120	60
0	1	0	8	50	25	30	15
0	1	1	4	100	50	60	30
1	0	0	5	80	40	48	24
1	0	1	7	57	29	34	17
1	1	0	1	250	200	200	125
1	1	1	3	133	67	80	40

0 = connect directly to GND, 1 = connect directly to VDD.

## Pin Description

Pin #	Name	Type	Description
1, 2, 24-28	R5, R6, R0-R4	I(PU)	Reference divider word input pins determined by user. Forms a binary number from 0 to 127.
3, 4, 5	S0, S1, S2	I(PU)	Select pins for output divider determined by user. See table above.
6, 23	VDD	P	Connect to VDD.
7	PECLIN	I	PECL input
8	$\overline{\text{PECLIN}}$	I	Complementary PECL input.
9, 20	GND	P	Connect to ground.
10-18	V0-V8	I(PU)	VCO divider word input pins determined by user. Forms a binary number from 0 to 511.
19	RES	I	Select for either PECL or CMOS outputs. See table above.
21	CLK1	O	Output Clock. Either PECL or CMOS determined by RES.
22	CLK2	O	Output Clock. Either PECL or CMOS determined by RES.

Key: I(PU) = Input with internal pull-up resistor; I = Input; O = Output; P = Power supply connection

## Output Clock Selection

If RES is connected directly to ground, CLK1 and CLK2 are low skew, CMOS output clocks. They are not complementary. If RES is connected to VDD through a 1.1 k resistor, then CLK1 and CLK2 become complementary PECL outputs which require the external resistor network shown in the block diagram. Refer to Application Note MAN09 for additional information.



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## Determining (setting) the output frequency

The user has full control in setting the desired output frequency over the range shown in the table on page 2. To replace a standard oscillator, a user should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout, so that the ICS525-03 automatically produces the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports to switch frequencies. By choosing dividers carefully, the number of inputs which need to be changed can be minimized. Observe the restrictions on allowed values of VDW and RDW.

The output of the ICS525 can be determined by the following simple equation:

$$\text{CLK frequency} = \text{Input frequency} \cdot P \cdot \frac{(\text{VDW}+8)}{(\text{RDW}+2)(\text{OD})}$$

Where: Reference Divider Word (RDW) = 0 to 127

VCO Divider Word (VDW) = 0 to 511

Output Divider (OD) = values on page 2 under Output Divider Table

Pre-divide (P) = values on page 2 under RES Value Table

Also, the following operating ranges should be observed:

$$500 \text{ MHz} < \text{Input frequency} \cdot P \cdot \frac{(\text{VDW}+8)}{(\text{RDW}+2)} < \begin{matrix} 350 \text{ MHz at 5.0V or} \\ 250 \text{ MHz at 3.3V} \end{matrix}$$

See Table on Page 2  
for full details of  
maximum output.

$$200 \text{ kHz} < \frac{\text{Input Frequency}}{(\text{RDW}+2)}$$

The dividers are expressed as integers, so that if a 66.66 MHz PECL output is desired from a 14.31818 PECL input, the Reference Divider Word (RDW) should be 59, and the VCO Divider Word (VDW) should be 276, with an Output divider (OD) of 1. To select PECL outputs, the RES pin should be tied to VDD with a 1.1 k resistor. In this example, R6:R0 is 0111011, V8:V0 is 100010100, and S2:S0 is 110. Since all of these inputs have pull-up resistors, it is only necessary to ground the zero pins, namely V7, V6, V5, V3, V1, V0, R6, R2, and S0.

To determine the best combination of VCO, reference, and output divider, use the ICS525-03 Calculator on our Web site: <http://www.icst.com>. This online form is easy to use and quickly shows you up to three options for these settings.

You may also fax this page to ICS at 408 295 9818(fax), or contact us via our website at <http://www.icst.com>. Be sure to indicate the following:

Your Name \_\_\_\_\_ Company Name \_\_\_\_\_ Telephone \_\_\_\_\_

Respond by e-mail (list your e-mail address) \_\_\_\_\_ or fax number \_\_\_\_\_

Desired input clock (in MHz) \_\_\_\_\_ Desired output frequency \_\_\_\_\_

VDD = 3.3V or 5V \_\_\_\_\_



# ICS525-03 PECL Input OSCaR™ User Configurable Clock

## Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
<b>ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)</b>					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage Temperature		-65		150	°C
<b>DC CHARACTERISTICS (VDD = 3.3 V unless otherwise noted)</b>					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Peak to peak input voltage	PECLIN, $\overline{\text{PECLIN}}$	0.3		1	V
Common mode range	PECLIN, $\overline{\text{PECLIN}}$	VDD - 1.4		VDD - 0.6	V
Output High Voltage, VOH	IOH=-25mA, CMOS out	2.4			V
Output Low Voltage, VOL	IOL=25mA, CMOS out			0.4	V
IDD Operating Supply Current	No Load, 60MHz out		15		mA
Short Circuit Current, CMOS out			±70		mA
On-Chip Pull-up Resistor	V, R, S select pins		270		k
Input Capacitance	V, R, S select pins		4		pF
<b>AC CHARACTERISTICS (VDD = 3.3 V unless otherwise noted)</b>					
Input Frequency		0.5		250	MHz
Output Frequency with OD=1, VDD = 4.5 to 5.5V		1		250	MHz
Output Frequency with OD=1, VDD = 3.0 to 3.6V		1		200	MHz
Output Clock Rise Time, CMOS clock	0.8 to 2.0V		1		ns
Output Clock Fall Time, CMOS clock	2.0 to 0.8V		1		ns
Output Clock Duty Cycle, even output dividers	at VDD/2	45		55	%
Output Clock Duty Cycle, odd output dividers	at VDD/2	40		60	%
Absolute Clock Period Jitter	Deviation from mean		±85		ps
One Sigma Clock Period Jitter			30		ps

## External Components

The ICS525-03 requires two 0.01µF decoupling capacitors to be connected between VDD and GND, one on each side of the chip. They must be connected close to the ICS525-03 to minimize lead inductance. No external power supply filtering is required for this device.

If PECL outputs are desired, RES should be tied to VDD with a 1.1 k resistor. Each output needs a resistive network of 62 and 270 per the block diagram on page 1. Application Note MAN09 gives more information about resistor selection.

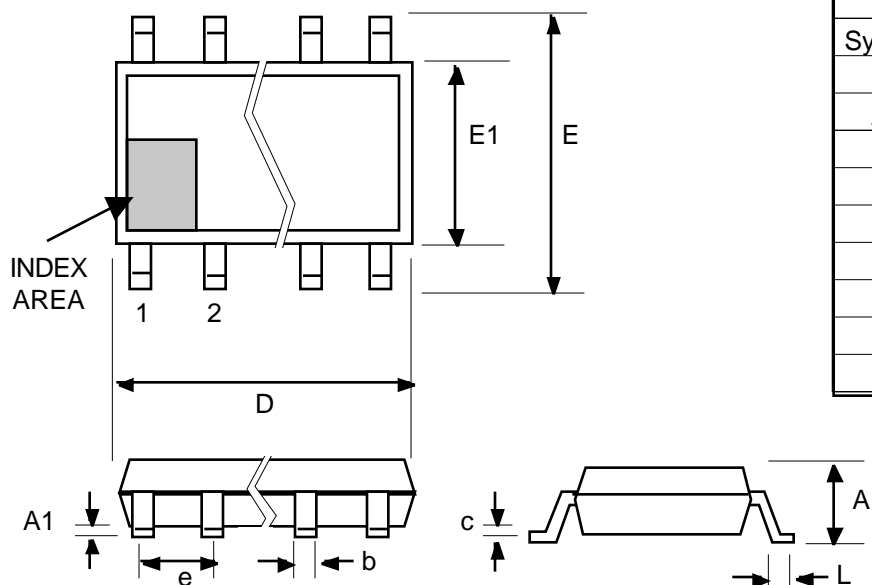


# ICS525-03 PECL Input OSCaR™ User Configurable Clock

## Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

### 28 pin SSOP (QSOP)



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.01
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27

## Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS525R-03I	ICS525R-03	28 pin narrow SSOP	-40 to +85 °C
ICS525R-03IT	ICS525R-03	28 pin SSOP on tape and reel	-40 to +85 °C

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