PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8761

LOW VOLTAGE, LOW SKEW, PCI / PCI-X CLOCK GENERATOR

GENERAL DESCRIPTION

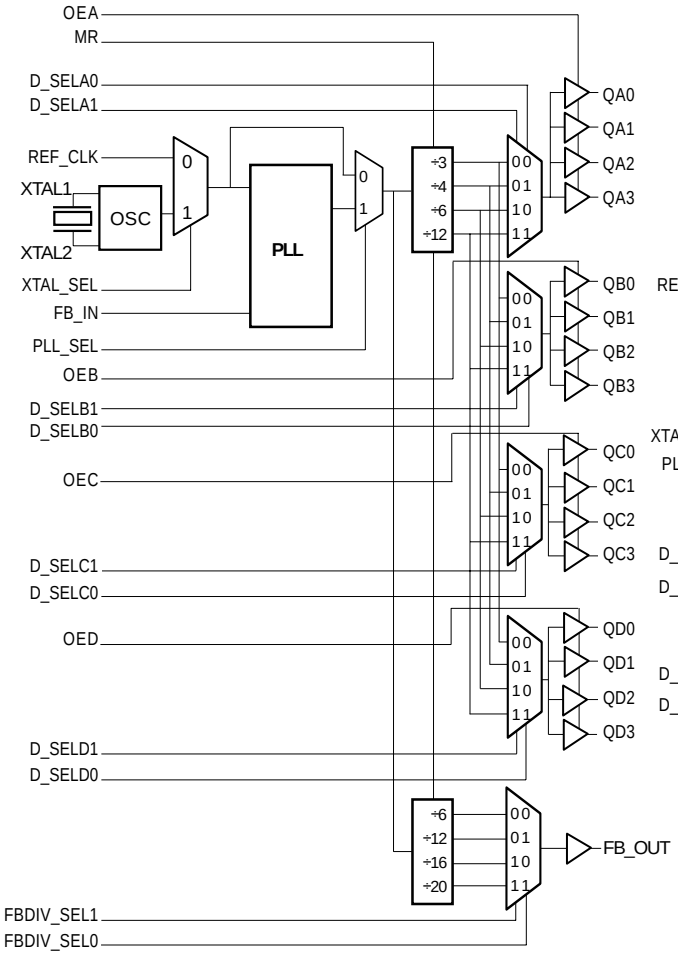
The ICS8761 is a low voltage, low skew PCI / PCI-X clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8761 has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTL input levels. The ICS8761 has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiplying and regenerating clocks with "zero delay". Using a 20MHz or 25MHz crystal or a 33.333MHz or 66.666MHz reference frequency, the ICS8761 will generate output frequencies of 33.333MHz, 66.666MHz, 100MHz and 133.333MHz simultaneously.

The low impedance LVCMOS outputs of the ICS8761 are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout of each output can be doubled by utilizing the ability of each output to drive two series terminated transmission lines.

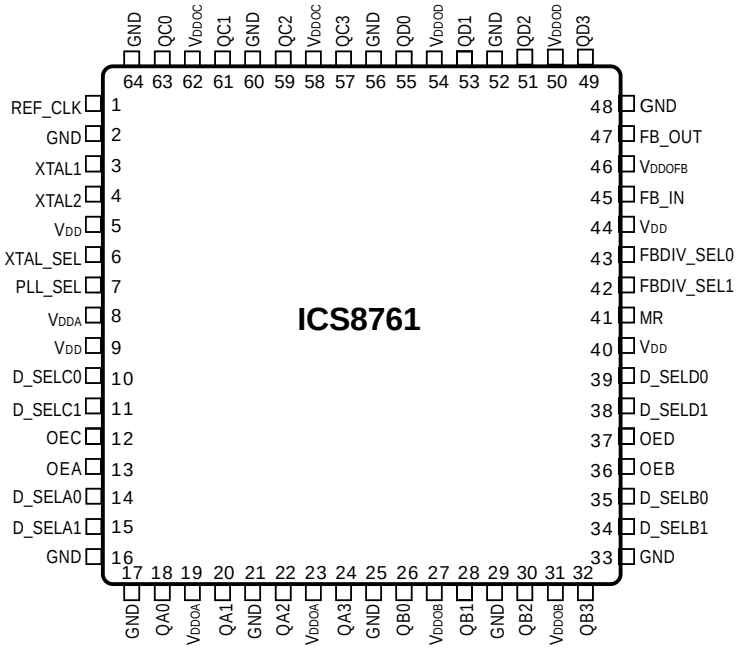
FEATURES

- Fully integrated PLL
- 17 LVCMOS outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS REF_CLK
- Maximum output frequency: 166.67MHz
- Maximum crystal input frequency: 38MHz
- Maximum REF_CLK input frequency: 83.33MHz
- Individual banks with selectable output dividers for generating 33.333MHz, 66.66MHz, 100MHz and 133.333MHz simultaneously
- Separate feedback control for generating PCI / PCI-X frequencies from a 20MHz or 25MHz crystal or 33.333MHz or 66.666MHz reference frequency
- Cycle-to-cycle jitter: TBD
- Phase jitter: TBD
- Output skew: 200ps (maximum)
- Bank skew: TBD
- Full 3.3V or 3.3V core, 2.5V multiple output supply modes
- 0°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



64-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	REF_CLK	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.
2, 16, 17, 21, 25, 29, 33, 48, 52, 56, 60, 64	GND	Power		Power supply ground.
3, 4	XTAL1, XTAL2	Input		Crystal oscillator inputs.
5, 9, 40, 44	V_{DD}	Power		Positive supply pins.
6	XTAL_SEL	Input	Pullup	Selects between crystal or reference inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_CLK when low. LVCMOS / LVTTL interface levels.
7	PLL_SEL	Input	Pullup	Selects between PLL and bypass mode. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
10, 11	D_SELC0, D_SELC1	Input	Pulldown	Selects divide value for bank C outputs as described in Table 3. LVCMOS / LVTTL interface levels.
12	OEC	Input	Pullup	Determines state of Bank C outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
13	OEA	Input	Pullup	Determines state of Bank A outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
14, 15	D_SELA0, D_SELA1	Input	Pulldown	Selects divider value for Bank A outputs as described in Table 3. LVCMOS / LVTTL interface levels.
18, 20, 22, 24	QA0, QA1, QA2, QA3	Output		Bank A clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
19, 23	V_{DDOA}	Power		Output supply pins for Bank A outputs.
26, 28, 30, 32	QB0, QB1, QB2, QB3	Output		Bank B clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
27, 31	V_{DDOB}	Power		Output supply pins for Bank B outputs.
34, 35	D_SELB1, D_SELB0	Input	Pulldown	Selects divider value for Bank B outputs as described in Table 3. LVCMOS / LVTTL interface levels.
36	OEB	Input	Pullup	Determines state of Bank B outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
37	OED	Input	Pullup	Determines state of Bank D outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
38, 39	D_SELD1, D_SELD0	Input	Pulldown	Selects divider value for bank D outputs as described in Table 3. LVCMOS / LVTTL interface levels.
41	MR	Input	Pulldown	Master reset. Resets the output divider. LVCMOS / LVTTL interface levels.
42, 43	FBDIV_SEL1, FBDIV_SEL0	Input	Pulldown	Selects divider value for bank feedback output as described in Table 3. LVCMOS / LVTTL interface levels.
45	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay". Connect to pin 47. LVCMOS / LVTTL interface levels.
46	V_{DDOFB}	Power		Output supply pin for FB_Out output.
47	FB_OUT	Output		Feedback output. Connect to FB_IN. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
49, 51, 53, 55	QD3, QD2, QD1, QD0	Output		Bank D clock outputs. 15Ω typical output impedance. LVCMOS, LVTTL interface levels.
50, 54	V_{DDOD}	Power		Output supply pins for Bank D outputs.
57, 59, 61, 63	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 15Ω typical output impedance. LVCMOS, LVTTL interface levels.
58, 62	V_{DDOC}	Power		Output supply pins for Bank C outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor				51	KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51	KΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDA}, V_{DDOx} = 3.465V				pF
R_{OUT}	Output Impedance			15		Ω

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, V_{DDOFB}.

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Inputs					Outputs			
MR	OEA	OEB	OEC	OED	QA0:QA3	QB0:QB3	QC0:QC3	QD0:QD3
1	1	1	1	1	LOW	LOW	LOW	LOW
0	1	1	1	1	Active	Active	Active	Active
X	0	0	0	0	HiZ	HiZ	HiZ	HiZ

TABLE 3B. OPERATING MODE FUNCTION TABLE

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

TABLE 3C. PLL INPUT FUNCTION TABLE

Inputs	
XTAL_SEL	PLL Input
0	REF_CLK
1	XTAL Oscillator

TABLE 3D. CONTROL FUNCTION TABLE

Inputs					Outputs		
					PLL_SEL =1	Frequency	
D_SELx1	D_SELx0	FBDIV_SEL1	FBDIV_SEL0	Reference Frequency Range (MHz)	QX0:QX3	QX0:QX3 (MHz)	FB_OUT (MHz)
0	0	0	0	33.33 - 83.33	x 2	66.67 - 166.67	33.33 - 83.33
0	0	0	1	16.67 - 41.67	x 4	66.67 - 166.67	16.67 - 41.67
0	0	1	0	12.5 - 31.25	x 5.33	66.67 - 166.67	12.5 - 31.25
0	0	1	1	10 - 25	x 6.67	66.67 - 166.67	10 - 25
0	1	0	0	33.33 - 83.33	x 1.5	50 - 125	33.33 - 83.33
0	1	0	1	16.67 - 41.67	x 3	50 - 125	16.67 - 41.67
0	1	1	0	12.5 - 31.25	x 4	50 - 125	12.5 - 31.25
0	1	1	1	10 - 25	x 5	50 - 125	10 - 25
1	0	0	0	33.33 - 83.33	x 1	33.33 - 83.33	33.33 - 83.33
1	0	0	1	16.67 - 41.67	x 2	33.33 - 83.33	16.67 - 41.67
1	0	1	0	12.5 - 31.25	x 2.67	33.33 - 83.33	12.5 - 31.25
1	0	1	1	10 - 25	x 3.33	33.33 - 83.33	10 - 25
1	1	0	0	33.33 - 83.33	÷ 2	16.67 - 41.67	33.33 - 83.33
1	1	0	1	16.67 - 41.67	÷ 1	16.67 - 41.67	16.67 - 41.67
1	1	1	0	12.5 - 31.25	x 1.33	16.67 - 41.67	12.5 - 31.25
1	1	1	1	10 - 25	x 1.67	16.67 - 41.67	10 - 25

NOTE: D_SELx1 denotes D_SELA1, D_SELB1, D_SELC1, and D_SELD1.
D_SELx0 denotes D_SELA0, D_SELB0, D_SELC0, and D_SELD0.
QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.

TABLE 3E. CONTROL FUNCTION TABLE (PCI CONFIGURATION)

Inputs					Outputs		
					PLL_SEL = 1	Frequency	
D_SELx1	D_SELx0	FBDIV_SEL1	FBDIV_SEL0	Reference Frequency (MHz)	QX0:QX3	QX0:QX3 (MHz)	FB_OUT (MHz)
0	0	0	0	66.67	x 2	133	66.67
0	0	0	1	33.33	x 4	133	33.33
0	0	1	0	25	x 5.33	133	25
0	0	1	1	20	x 6.67	133	20
0	1	0	0	66.67	x 1.5	100	66.67
0	1	0	1	33.33	x 3	100	33.33
0	1	1	0	25	x 4	100	25
0	1	1	1	20	x 5	100	20
1	0	0	0	66.67	x 1	66.67	66.67
1	0	0	1	33.33	x 2	66.67	33.33
1	0	1	0	25	x 2.67	66.67	25
1	0	1	1	20	x 3.33	66.67	20
1	1	0	0	66.67	÷ 2	33.33	66.67
1	1	0	1	33.33	÷ 1	33.33	33.33
1	1	1	0	25	x 1.33	33.33	25
1	1	1	1	20	x 1.67	33.33	20

NOTE: D_SELx1 denotes D_SELA1, D_SELB1, D_SELC1, and D_SELD1.
D_SELx0 denotes D_SELA0, D_SELB0, D_SELC0, and D_SELD0.
QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD}+0.5 V
Outputs, V_O	-0.5V to V_{DDOx}+0.5V
Package Thermal Impedance, θ_{JA}	41.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = 0°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDOx}	Output Supply Current; NOTE 2			TBD		mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOFB}.
NOTE 2: I_{DDOx} denotes I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}, and I_{DDOFB}.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, T_A = 0°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1:D_SELD1, PLL_SEL, FBDIV_SEL0, FBDIV_SEL1		2		V_{DD} + 0.3	V
		REF_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1, D_SELD1, PLL_SEL		-0.3		0.8	V
		REF_CLK		-0.3		1.3	V
I_{IH}	Input High Current	D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL0, FBDIV_SEL1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		XTAL_SEL, PLL_SEL, OEA:OED	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL0, FBDIV_SEL1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		XTAL_SEL, PLL_SEL, OEA:OED	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low					TBD	µA
I_{OZH}	Output Tristate Current High					TBD	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDOx}/2. See Parameter Measurement Information section, "3.3V Output Load Test Circuit".

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1			TBD		ps
*t*sk(b)	Bank Skew; NOTE 2, 7				200	ps
*t*sk(o)	Output Skew; NOTE 3, 7			TBD		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4, 7			TBD		ps
*t*jit(Ø)	Phase Jitter; NOTE 5, 7			TBD		ps
t_L	PLL Lock Time				1	ms
t_R	Output Rise Time	20% to 80% @ 50MHz	200		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	200		700	ps
odc	Output Duty Cycle; NOTE 6			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 4: Jitter performance using XTAL inputs.
NOTE 5: Phase jitter is dependent on the input source used.
NOTE 6: Measured using REF_CLK. For XTAL input, refer to Application Note.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDOx} = 2.5V±5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDOx}	Output Supply Current; NOTE 2			TBD		mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOFB}.
NOTE 2: I_{DDOx} denotes I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}, and I_{DDOFB}.

TABLE 4D. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDOx} = 2.5V±5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1:D_SELD1, PLL_SEL, FBDIV_SEL0, FBDIV_SEL1		2		V_{DD} + 0.3	V
		REF_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1:D_SELD1, PLL_SEL, FBDIV_SEL0, FBDIV_SEL1		-0.3		0.8	V
		REF_CLK		-0.3		1.3	V
I_{IH}	Input High Current	D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL0, FBDIV_SEL1	$V_{DD} = V_{IN} = 3.465V$			150	µA
		XTAL_SEL, PLL_SEL, OEA:OED	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL0, FBDIV_SEL1	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		XTAL_SEL, PLL_SEL, OEA:OED	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V
I_{OZL}	Output Tristate Current Low					TBD	µA
I_{OZH}	Output Tristate Current High					TBD	µA

NOTE 1: Outputs terminated with 50Ω to $V_{DDOx}/2$. See Parameter Measurement Information section, "3.3V/2.5V Output Load Test Circuit".

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDOx} = 2.5V±5\%$, $T_A = 0°C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE			TBD		ps
*t*sk(b)	Bank Skew; NOTE 2, 7				200	ps
*t*sk(o)	Output Skew; NOTE 3, 7			TBD		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4, 7			TBD		ps
*t*jit(Ø)	Phase Jitter; NOTE 5, 7			TBD		ps
t_L	PLL Lock Time				1	ms
t_R	Output Rise Time	20% to 80% @ 50MHz	200		700	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	200		70	ps
odc	Output Duty Cycle; NOTE 6			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 4: Jitter performance using XTAL inputs.
NOTE 5: Phase jitter is dependent on the input source used.
NOTE 6: Measured using REF_CLK. For XTAL input, refer to Application Note.
NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

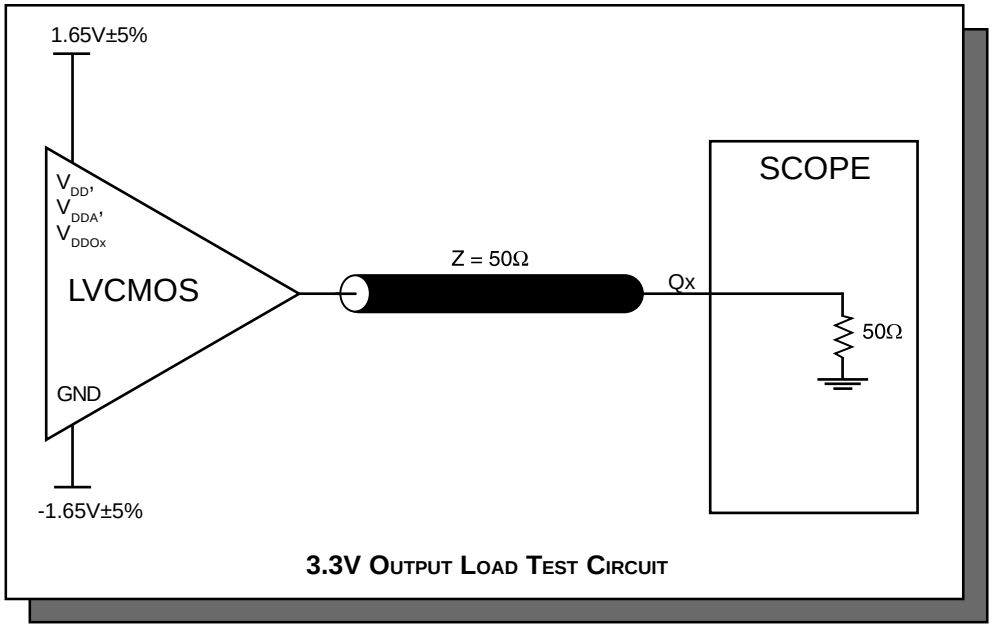
TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		38	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance			7		pF

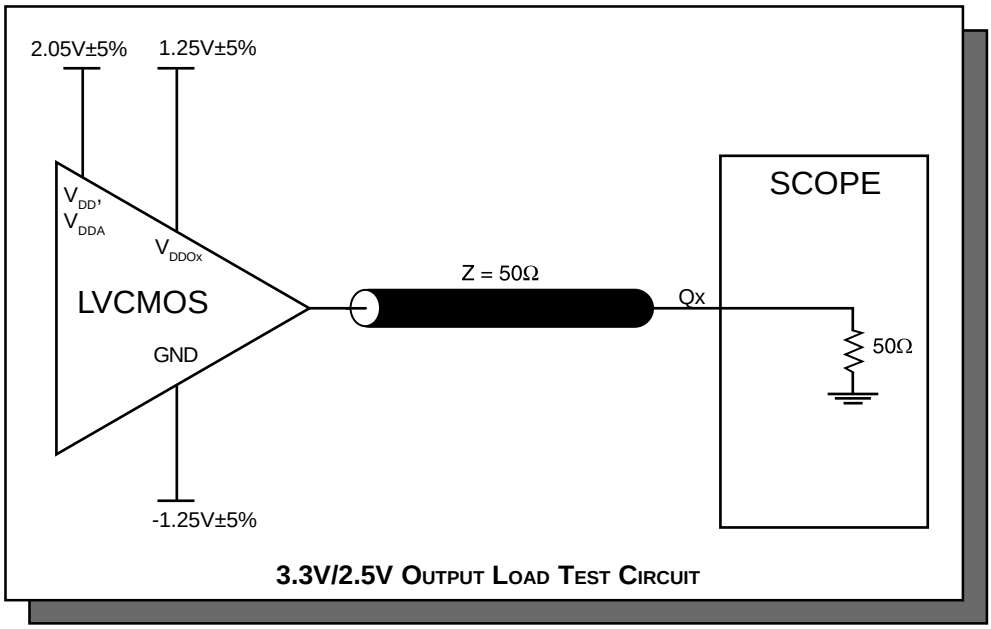
TABLE 7. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, $T_A = 85C$ TO $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Reference Frequency		10		83.33	MHz

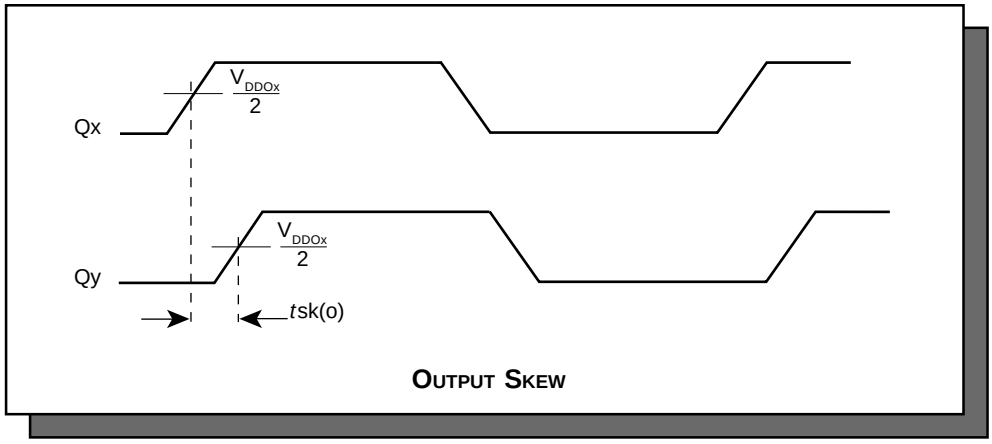
PARAMETER MEASUREMENT INFORMATION



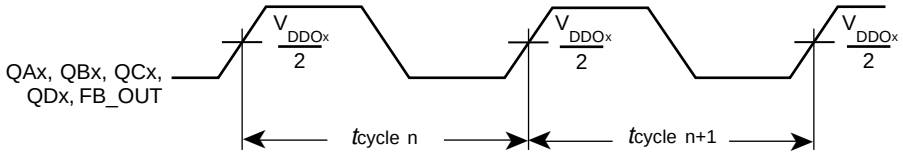
3.3V OUTPUT LOAD TEST CIRCUIT



3.3V/2.5V OUTPUT LOAD TEST CIRCUIT



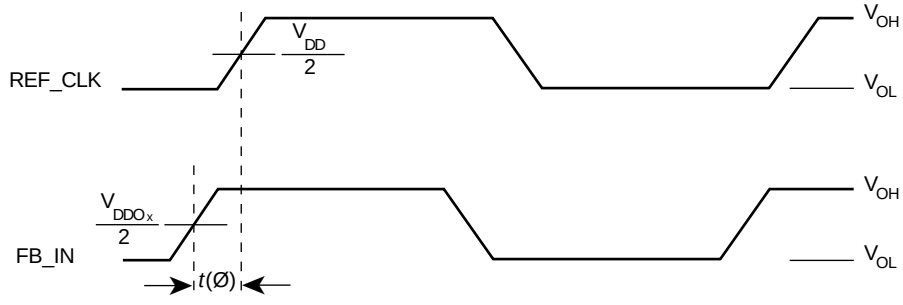
OUTPUT SKEW



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

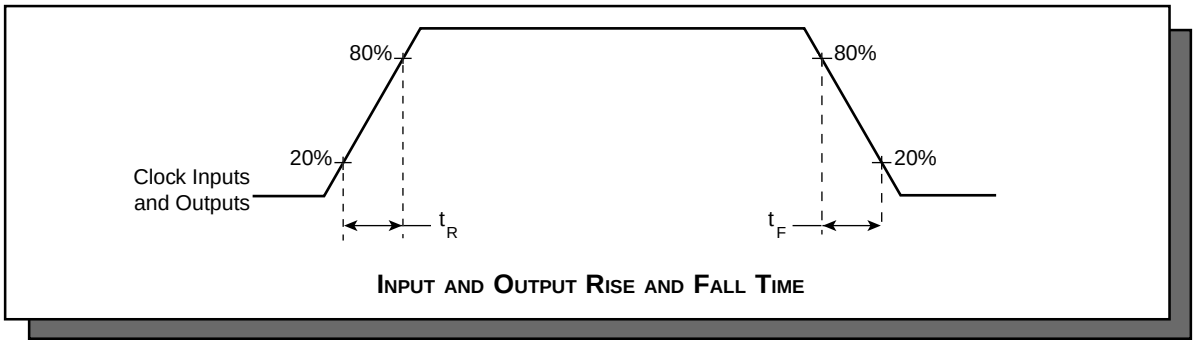
Cycle-to-Cycle Jitter



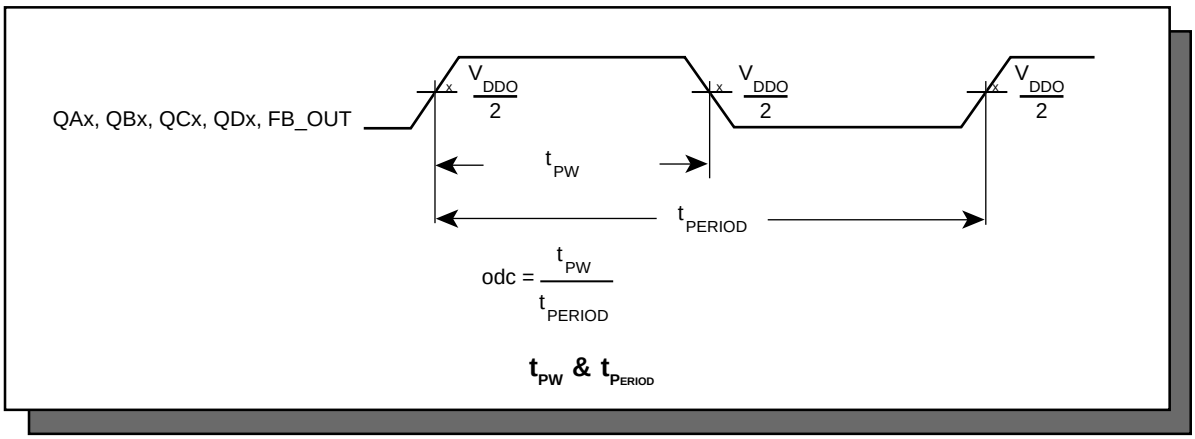
$t_{jit(Ø)} = |t(Ø) - t(Ø)_{mean}|$ = Phase Jitter $t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

PHASE JITTER AND STATIC PHASE OFFSET



INPUT AND OUTPUT RISE AND FALL TIME



t_{PW} & t_{PERIOD}

TABLE 8. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.8°C/W	48.5°C/W	43.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	41.1°C/W	35.8°C/W	33.6°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8761 is: 6000

PACKAGE OUTLINE - Y SUFFIX

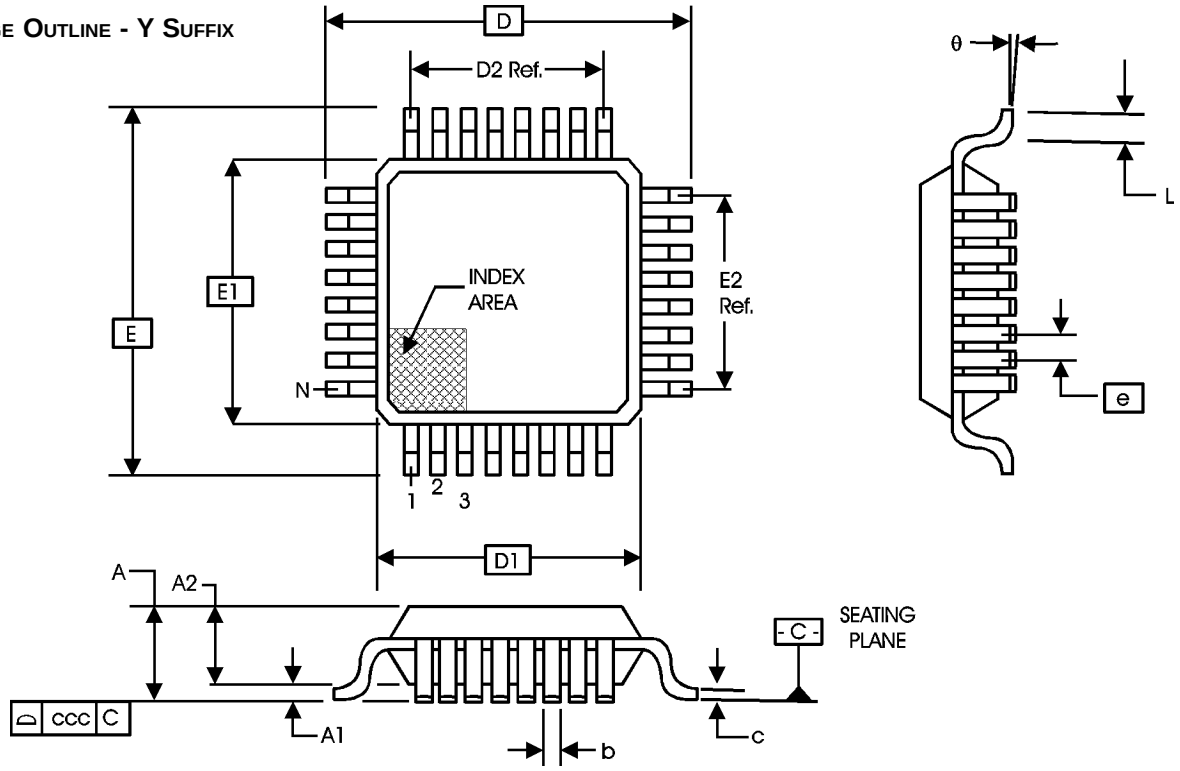


TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCD		
	MINIMUM	NOMINAL	MAXIMUM
N		64	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	--	0.27
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
D2		7.50 Ref.	
E		12.00 BASIC	
E1		10.00 BASIC	
E2		7.50 Ref.	
e		0.50 BASIC	
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8761CY	ICS8761CY	64 Lead LQFP	160 per tray	0°C to 70°C
ICS8761CYT	ICS8761CY	64 Lead LQFP on Tape and Reel	500	0°C to 70°C