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Impala Linear Corporation

June 1996

ILC5061

SOT-23 Power Supply Reset Monitor

General Description

All-CMOS Monitor circuits in a 3-lead SOT-23 package offer the best performance in power consumption and accuracy.

The ILC5061 comes in a series of ±1% accurate trip voltages to fit most microprocessor applications. Even though its output can sink 2mA, the device draws only 1µA in normal operation.

Additionally, a built-in hysteresis of 5% of detect voltage simplifies system design.

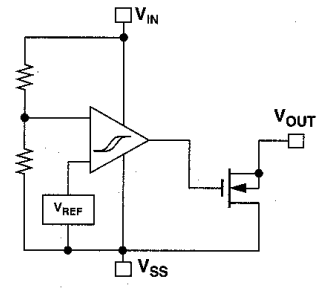
Features

- All-CMOS design in SOT-23 and SOT-89 package
- ±1% precision in Reset Detection
- Only 1µA of Iq
- 2mA of sink current capability
- Built-in hysteresis of 5% of detection voltage
- Voltage options of 2.6, 2.9, 3.1, 4.4, and 4.6V fit most supervisory applications

Applications

- Microprocessor reset circuits
- Memory battery back-up circuitry
- Power-on reset circuits
- Portable and battery powered electronics

Block Diagram

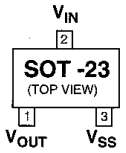


N - Channel Open Drain Output

Ordering Information*	
ILC5061AM-26	2.6V±1% Monitor in SOT-23
ILC5061AM-29	2.9V±1% Monitor in SOT-23
ILC5061AM-31	3.1V±1% Monitor in SOT-23
ILC5061AM-44	4.4V±1% Monitor in SOT-23
ILC5061AM-46	4.6V±1% Monitor in SOT-23

* Standard product offering comes in tape & reel, quantity 3000 per reel, orientation right.

Pin-Package Configurations



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Absolute Maximum Ratings (T_A=25°C)

Parameter		Symbol	Ratings	Units
Input Voltage		V_{IN}	12	V
Output Current		I_{OUT}	50	mA
Output Voltage		V_{OUT}	V_{SS}-0.3~V_{IN}+03	V
Continuous Total Power Dissipation	SOT-23	P_d	150	mW
Operating Ambient Temperature		T_{opr}	-30~+80	°C
Storage Temperature		T_{stg}	-40~+125	°C

Electrical Characteristics ILC5061 (T_A=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detect Fail Voltage	V_{DF}		V_{DF} X 0.99	V_{DF}	V_{DF} X 1.01	V
Hysteresis Range	V_{HYS}		V_{DF} X 0.02	V_{DF} X 0.05	V_{DF} X 0.08	V
Supply Current	I_{SS}	V_{IN} =1.5V V_{IN} =2.0V V_{IN} =3.0V V_{IN} =4.0V V_{IN} =5.0V		0.9 1.0 1.3 1.6 2.0	2.6 3.0 3.4 3.8 4.2	µA
Operating Voltage	V_{IN}	V_{DF} =2.1 ~ 6.0V	1.5		10.0	V
Output Current	I_{OUT}	N-ch V_{DS}=0.5V V_{IN}=1.0V V_{IN}=2.0V V_{IN}=3.0V V_{IN}=4.0V V_{IN}=5.0V		2.2 7.7 10.1 11.5 13.0		mA
Temperature Characteristics	$\Delta V_{DF}/(\Delta T_{opr} \bullet V_{DF})$	-30°C≤T_{opr}≤80°C		±100		ppm/°C
Delay Time (Release Voltage→ Output Inversion)	t_{DLY} (V_{DR}→V_{OUT} Inversion)				0.2	ms

Note:

1. An additional resistor between the V_{IN} pin and supply voltage may cause deterioration of the characteristics due to increasing of V_{DR}

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Functional Description

The following designators 1~6 refer to the timing diagram below.

1. While the input voltage (V_{IN}) is higher than the detect voltage (V_{DF}); the V_{OUT} output pin is at high impedance state.

2. When the input V_{IN} voltage falls lower than V_{DF}, V_{OUT} drops near to ground voltage

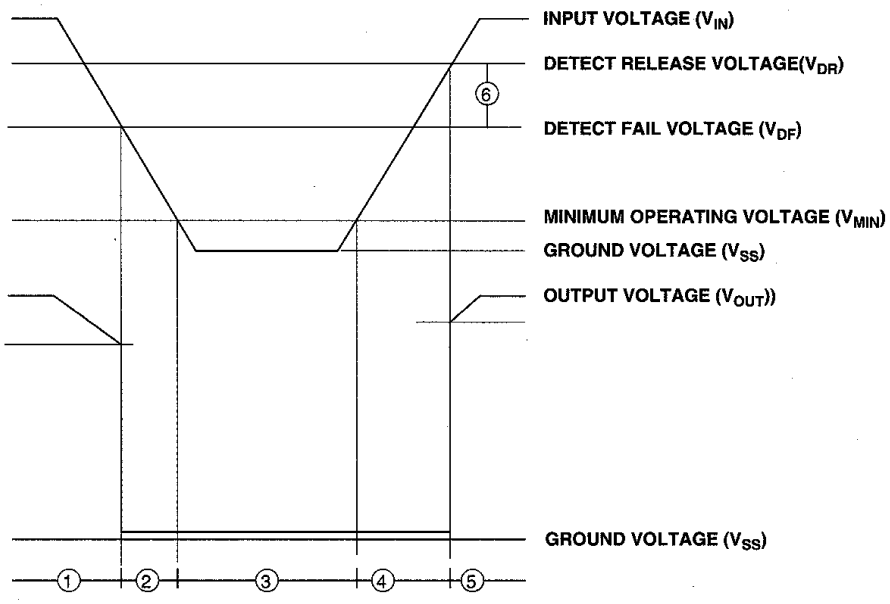
3. If the input voltage further decreases below the minimum operating voltage (V_{MIN}), the V_{OUT} output becomes unstable. In this condition, if the V_{OUT} pin is pulled up, V_{OUT} indicates the V_{IN} voltage.

4. During an increase of the input voltage from the V_{SS} voltage, V_{OUT} is not stable in the voltage below the V_{MIN}. Exceeding that level, the output stays at the ground level (V_{SS}) between the minimum operating voltage (V_{MIN}) and detect release voltage (V_{DR}).

5. If the input voltage further increase more than V_{DR}; the V_{OUT} output pin is at high impedance state.

6. The difference between V_{DR} and V_{DF} is the hysteresis in the system.

Timing Diagram



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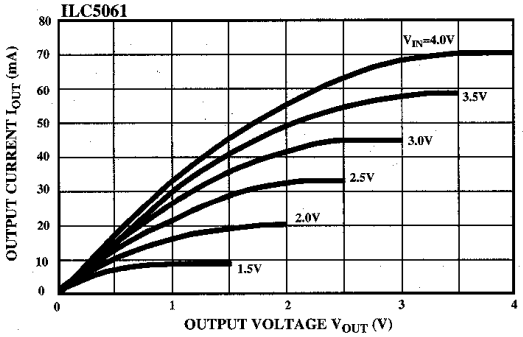
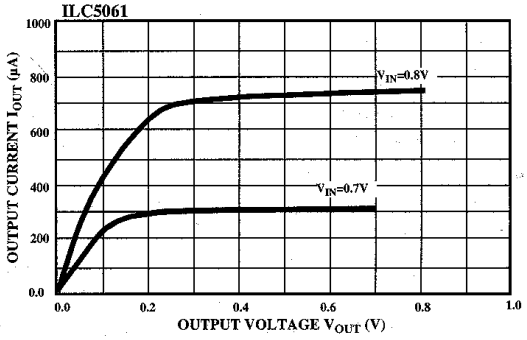
Typical Performance Characteristics General conditions for all curves.

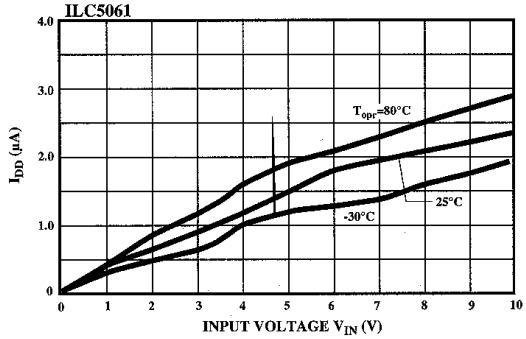
OUTPUT VOLTAGE vs OUTPUT CURRENT



OUTPUT VOLTAGE vs OUTPUT CURRENT

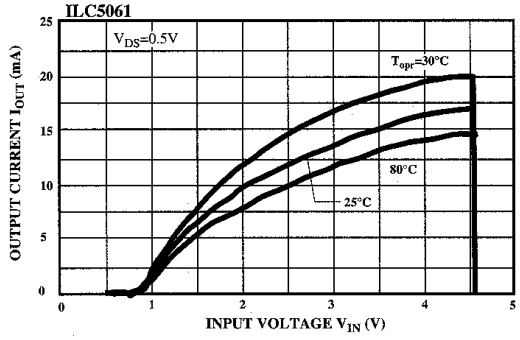


I_{DD} vs INPUT VOLTAGE *



* A spike of ½ to 1 µA may appear as Vin crosses V_{DR} or V_{DF}

OUTPUT CURRENT vs INPUT VOLTAGE



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