



20-BIT BUS EXCHANGE SWITCH

IDT74FST1632383

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance: 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in SSOP and TSSOP packages

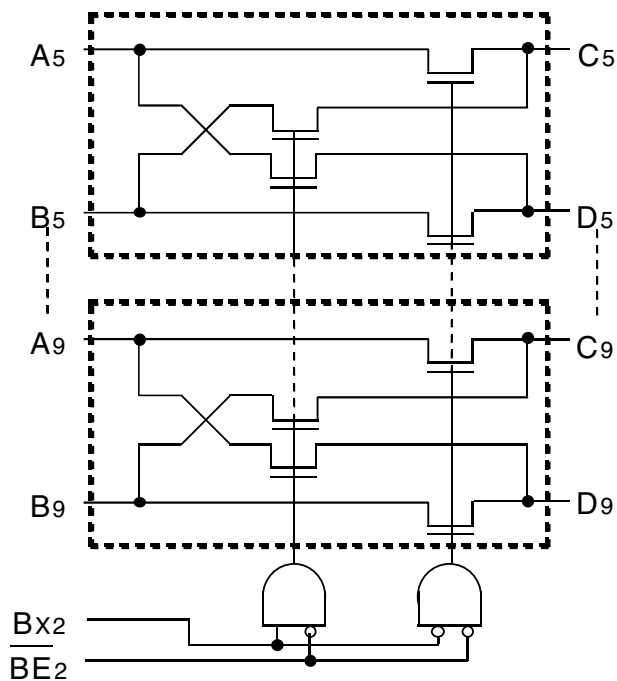
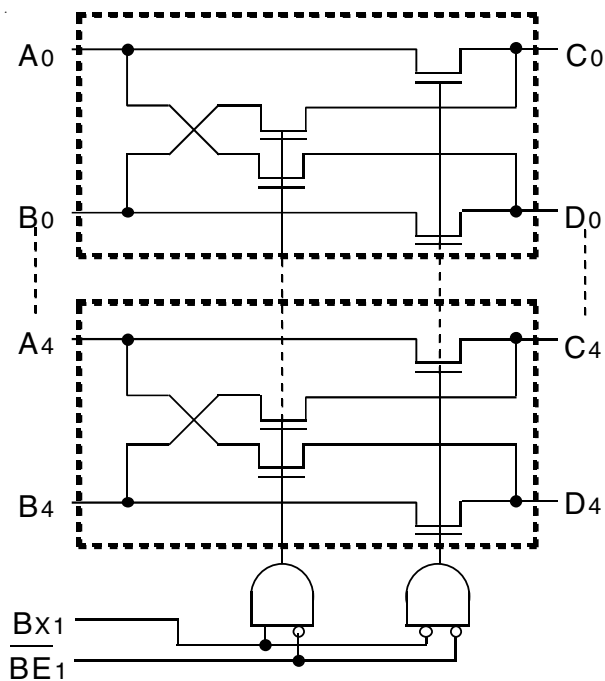
DESCRIPTION:

The FST1632383 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no V_{CC} applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST1632383 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors. It also provides four 4-bit TTL-compatible ports that supports 2 way bus exchange. The BX pin controls the bus exchange and the BE pin serves as the enable pin.

FUNCTIONAL BLOCK DIAGRAM

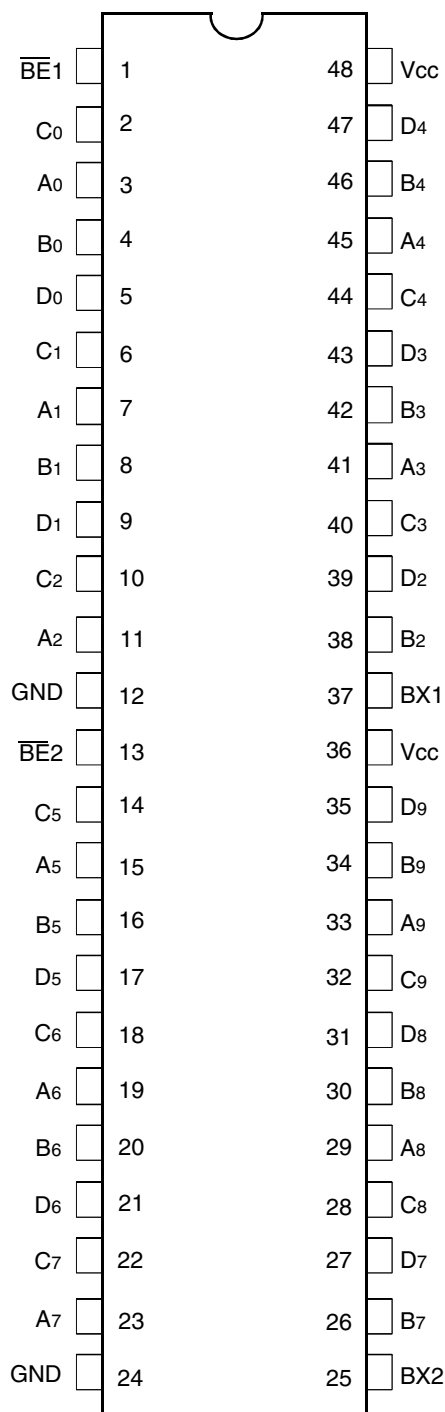


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INDUSTRIAL TEMPERATURE RANGE

MAY 2002

PIN CONFIGURATION



SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	Maximum Continuous Channel Current	128	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{cc}, Control, and Switch terminals.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
C _{IN}	Control Input Capacitance		4	pF
C _{I/O}	Switch Input/Output Capacitance	Switch Off		pF

NOTES:

- Capacitance is characterized but not tested.
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V.

PIN DESCRIPTION

Pin Names	I/O	Description
A0-9, B0-9	I/O	Buses A, B
C0-9, D0-9	I/O	Buses C, D
BE _{1,2}	I	Bus Switch Enable (Active LOW)
BE _{1,2}	I	Bus Exchange

FUNCTION TABLE⁽¹⁾

BE ₁	BX ₁	A0-4	B0-4	Description
H	X	Z	Z	Disconnect
L	L	C0-4	D0-4	Connect
L	H	D0-4	C0-4	Exchange

BE ₂	BX ₂	A5-9	B5-9	Description
H	X	Z	Z	Disconnect
L	L	C5-9	D5-9	Connect
L	H	D5-9	C5-9	Exchange

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_I = V_{CC}$	—	—	± 1	μA
I_{IL}	Input LOW Current		—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output Pins)	$V_{CC} = \text{Max.}$ $V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			—	—	± 1	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}^{(3)}$	—	300	—	mA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}$, $V_{IN} = 0\text{V}$, $I_{ON} = 30\text{mA}$	17	28	40	Ω
		$V_{CC} = \text{Min.}$, $V_{IN} = 2.4\text{V}$, $I_{ON} = 15\text{mA}$	20	35	48	
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$	—	—	± 1	μA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_I = \text{GND}$ or V_{CC}	—	0.1	3	μA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(3)}$	—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling 50% Duty Cycle	—	30	40	$\mu\text{A}/\text{MHz}/\text{Switch}$
I_C	Total Power Supply Current ⁽⁵⁾	$V_{CC} = \text{Max.}$ Outputs Open Enable Pins Toggling (20 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	—	6	8	mA
		$V_{IN} = V_{CC}$ $V_{IN} = 3.4\text{V}$	—	6.5	9.5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4\text{V}$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4\text{V})$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_i = \text{Control Input Frequency}$
 $N = \text{Number of Control Inputs Toggling at } f_i$

All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

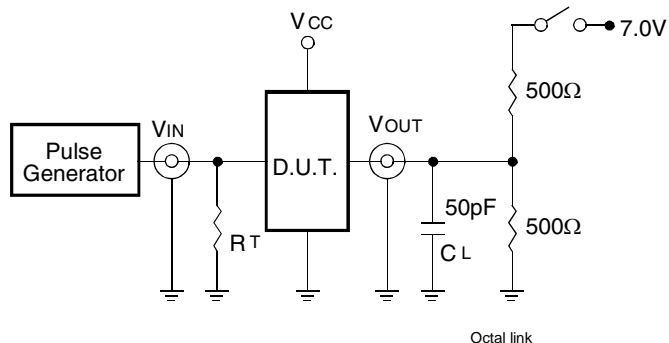
Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Description ⁽¹⁾	Condition	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay Ax to Cx, Dx and/or Bx to Cx and/or Dx ^(3,4)	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	—	1.25	ns
t_{BX}	Switch Multiplex Delay BX to Ax, Bx, Cx, Dx		1.5	—	7.5	ns
t_{PZH} t_{PZL}	Switch Turn On Delay BE to Ax, Bx, Cx, Dx		1.5	—	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn Off Delay BE to Ax, Bx ⁽³⁾		1.5	—	5.5	ns
$ Q_{CI} $	Charge Injection, Typical ^(5,6)		—	1.5	—	pC
$ Q_{DCI} $	Charge Injection, Typical ^(6,7)		—	0.5	—	

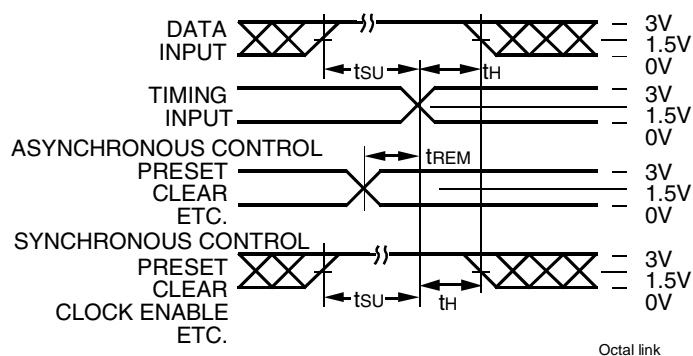
NOTES:

1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 2.5ns for 50pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay on the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 M Ω scope probe, $V_{IN} = 0.0$ volts.
6. Characterized parameter. Not 100% tested.
7. Measured at switch turn off through bus multiplexer, (e.g.- A to C = >A to D), load = 50 pF in parallel with 10 M Ω scope probe, V_{IN} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.

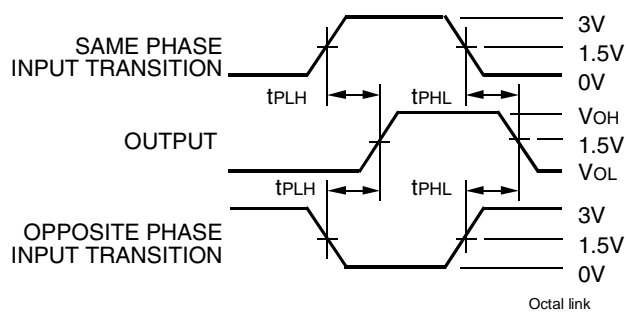
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



Propagation Delay

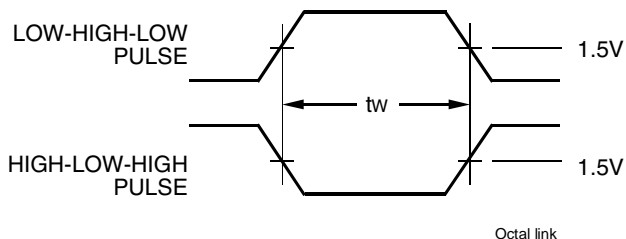
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

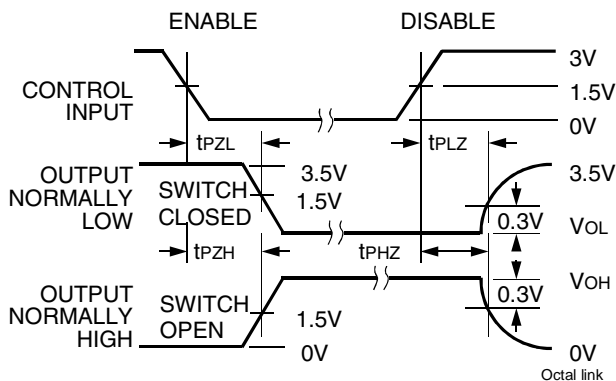
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION

IDT	XX	FST	XXX	XXX	X	
	Temp. Range		Family	Device Type	Package	
					PV	Shrink Small Outline Package
					PA	Thin Shrink Small Outline Package
					2383	20-Bit Bus Exchange Switch
					163	Double-Density Bus Switch
					74	−40°C to +85°C

DATA SHEET DOCUMENT HISTORY

5/28/2002 Removed TVSOP package



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459