

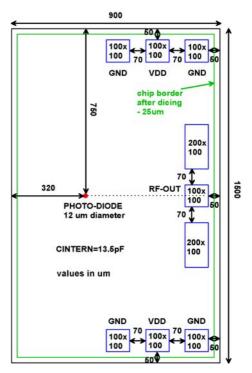
IPD48C-40z: 40 GHz PIN Diode

Applications

The series IPD48 PINs are applicable for building up the next generation of high bit rate opto-electronic receivers for SONET/SDH (OC-768) and Ethernet applications.

Features

- True bandwidth of 40 GHz (-3dB)
- High optical input power (+6 dBm)
- High linear phase characteristic
- Low bias voltage (< 4 V)
- Low leakage current
- On-chip biasing: IPD48C-40B
 External biasing: IPD48C-40N
- Customized layouts possible



note: all coordinates are center-coordinates relative to the center of the PIN diode (all coordinates in µm)

Description

The IPD48 series are vertical PIN diode devices suitable for hybrid integration in opto-electronic receivers and measurement testsets. The IPD48 offer high optical input power capability and high linear phase behavior. The PINs comprise anti-reflection coating and passivation. Depending on application, types with and without on-chip bias networks are available. For frequencies below 2 GHz external blocking capacitors are necessary.

Optical / Electrical Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks
Maximum Optical Input Power	P _{max}		10	dBm	
Maximum Reverse Voltage	$V_{r,max}$	10		>	
Maximum Forward Current	$I_{f,max}$		2	mA	
Storage Temperatures	t _{st}	-10	+80	°C	
Operating Temperatures	t _{op}	+10	+70	°C	+150 °C short term
Peak Temperature (unbiased)	t _{pe}		+300	°C	30 sec.
Humidity		5	65	% r.h.	



IPAG - Innovative Processing AG

IPD48C-40z: 40 GHz PIN Diode

Optical / Electrical Parameters

Parameter	Symbol	Min	Тур	Max	Unit	Remarks
Optical Wavelength	λ	1520		1620	nm	typ. 1550 nm
Optical Input Power	$P_{o,in}$			6	dBm	@ 1 dB compression
Polarization Dependence				± 0.1	dB	
Responsivity	R	0.4			A/W	@ B = 40 GHz 1)
Small Signal Bandwidth	В		40	45	GHz	$f_{\sf 3dB}$
Lower Frequency Limit 2)	f _{cl}	1	2		GHz	2)
Group Delay Time Variations	$ au_{grp}$		± 4	± 5	ps	
Bias Voltage 4)	V_{pin}	-2.5	-3.0	-3.5 ³⁾	V	
Leakage Current	I _{rev}		10	100	nA	@ V _{pin} = -3 V

¹⁾ and 1550 nm optical wavelength

- 2) external blocking capacitor enables lower frequency limits down to 100kHz
- 3) this is the maximum bias voltage to achieve the desired responsivity, see also Maximum Ratings
- 4) on-chip biasing IPD48C-40B; or external biasing IPD48C-40N

Small signal models for the description of the PIN diode frequency behavior are available on request.

Mechanical Parameters

Parameter	Тур.	Unit	Remarks
Chip size	1500 x 900	μm	changes after dicing 1)
Thickness	500	μm	
Pad sizes	100 x 100	μm	200 x 100 for RF-OUT
Active Optical Region Radius	6	μm	

¹⁾ absolute chip size varies within $\pm 100 \, \mu m$, rf-out pads are always as close as possible to edge of chip

For further information, contact Markus Lenders at IPAG - Innovative Processing AG:

phone: ++49 (0)203 / 379-3841 fax: ++49 (0)203 / 379-4094

or the following:

INTERNET: http://www.ipag35.com E-Mail: sales@ipag35.com

IPAG - Innovative Processing AG reserves the right to make changes to the product(s) or information contained here without notice

No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such product(s).

© Copyright 2002 IPAG - Innovative Processing AG. All Rights Reserved. January 2002 IPD48X-40z