256K X 32 SRAM Module

Features

- 4.5V - 5.5V Operation
- Variable speed CMOS SRAMs modules
- Low active power
  —2.64W (max.)
- Low standby power
  —11.0 mW (max.)
- Automatic power-down when deselected
- High Density 8 mega bit SRAM module
- SMD Technology
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and $\overline{OE}$ options
- Data Retention Function
- Fully Static No Clocks

High Density Packaging
- Available in 64 -pin ZIP version
- Single +5V(±10%) Supply Operation

Functional Description

The IMM1841 are high performance 8-megabit static RAM modules. Four chip select ($\overline{CS}1$, $\overline{CS}2$, $\overline{CS}3$, $\overline{CS}4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of chip selects

Writing to each byte is accomplished by taking appropriate Chip enable ($\overline{CE}$) and Write enable (WE) inputs LOW. Data on the eight I/O pins(I/O_0 through I/O_{31})is then written into the location specified on the address pins (A_0 through A_{17}).

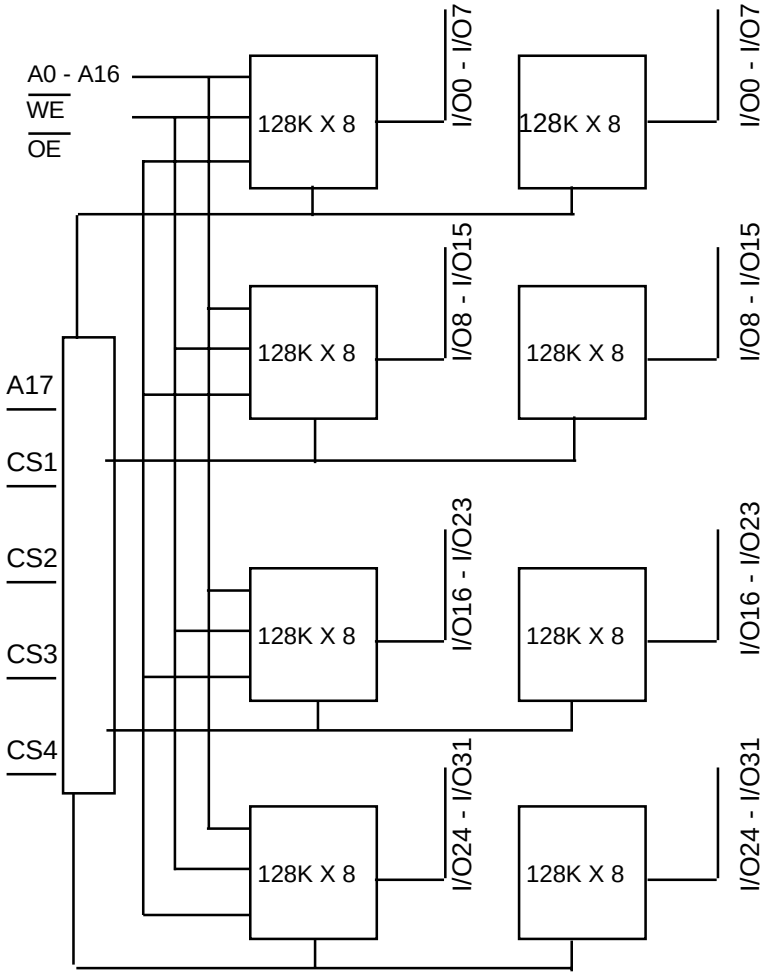
Reading from the device is accomplished by taking Chip enable ($\overline{CE}$) and Output enable ($\overline{OE}$) LOW while forcing Write enable ($\overline{WE}$) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The thirty two input/output pins(I/O0 through I/O31) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

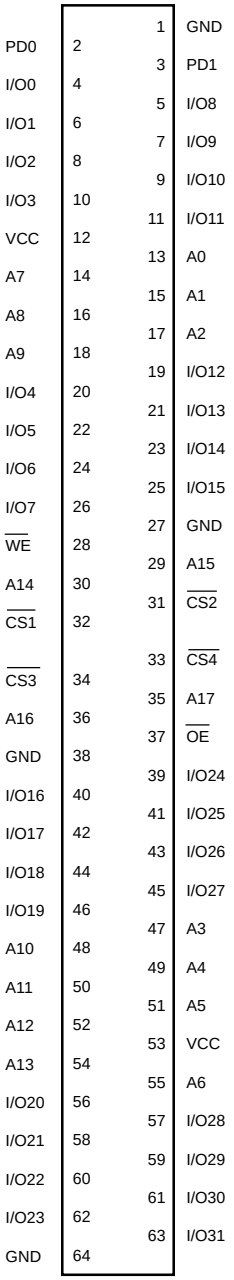
Two pins PD0 and PD1 are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged. The IMM1841 utilizes corner power and ground SRAM's

256K X 32 SRAM Module

BLOCK DIAGRAM



PIN CONFIGRATION



Pin Names

A0 – A17	Address Inputs
CS1- CS4	Chip Enable
WE	Write Enable
OE	Output Enable
I/O0 – I/O31	Data Input/Output
Gnd	Ground
Vcc	Power Supply +5V
PD0-PD1	Memory Density Identifier

Selection Guide

	IMM1841-35	IMM1841-45
Maximum Access time	35	45
Maximum Operating Current	960	960
Maximum CMOS Standby Current (mA)	480	480

Maximum Ratings (Above which the useful life may be impaired. For user guide lines, not tested)

Storage Temperature.....-55°C to +125°C
Ambient Temperature..... 0°C to 85°C
Supply voltage on Vcc relative to Gnd.....-0.5 V to 7.0V
Current into Outputs (LOW).....20mA
DC Input Voltage.....0.5 v to Vcc + 0.5V

Operating Range

Range	Ambient Temperature	Vcc
Commercial	0°C to 70°C	4.5V - 5.5V

Electrical Characteristics

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{OH}	Output HIGH voltage	Vcc = Min, I_{OH} = -4mA	2.4		V
V_{OL}	Output LOW voltage	Vcc = Min, I_{OL} = 8mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	Vcc	
V_{IL}	Input LOW Voltage		-0.5	0.8	V
I_{IX}	Input Load Current	Gnd < V1 < Vcc	-16	16	mA
I_{OZ}	Output Leakage Current	Gnd < V_0 < Vcc, Output Disable	-10	10	mA
I_{CC}	Vcc Operating	Vcc = Max., I_{OUT} = 0mA		960	mA
	Supply Current	$\overline{CS}$ < V_{IL}			
I_{SB1}	Automatic $\overline{CE}$	Max V_{CC}, $\overline{CE}$ > V_{IH}		480	mA
	Power-Down Current	V_{IN} > V_{IH} or V_{IN} < V_{IH}, Min Duty			
	TTL Inputs	cycle = 100%			
I_{SB2}	Automatic $\overline{CE}$	Max V_{CC}, $\overline{CE}$ > V_{CC} - 0.2		200	mA
	Power-Down Current	V_{IN} > VCC - 0.2, or V_{IN} < 0.2			

Switching Characteristics over the Operating Range

Parameter	Description	IMM1841- 35		IMM1841- 45		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		45		ns
t_{AA}	Address to Data Valid		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7,8]		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7,8]		20		20	ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		35		45	ns
t_{WC}	Write Cycle Time	35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		40		ns
t_{AW}	Address Set-Up to Write End	30		40		ns
t_{HA}	Address Hold from Write End	2		2		ns
t_{SA}	Address Set-up to write start	2		2		ns
t_{PWE}	WE Pulse Width	30		35		ns
t_{SD}	Data Set-up to Write End	20		25		ns
t_{HD}	Data Hold from Write End	2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to LOW Z[8]	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7,8]	0	15	0	15	ns

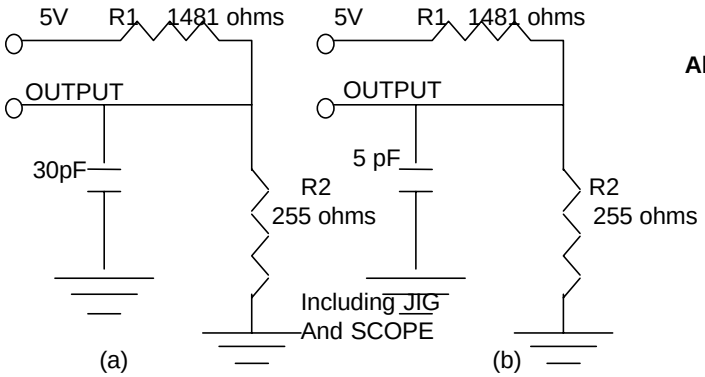
Notes:

1. A pullup resistor on CS input is required to keep the device deselected during Vcc power-up, oterwise I_{SB} will exceed values
2. 20 pF on CS and 70 pF on all others

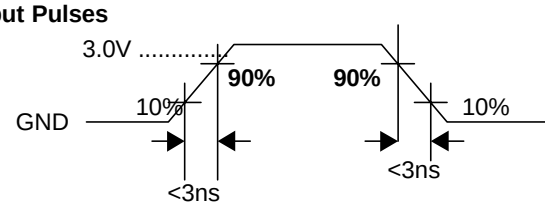
Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^oC$, f = 1 MHz, V_{CC} = 5.0V	70/20	pF
C_{OUT}	Output Capacitance		20	pF

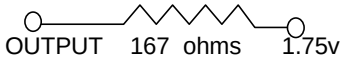
AC Test Loads and Waveforms



All Input Pulses



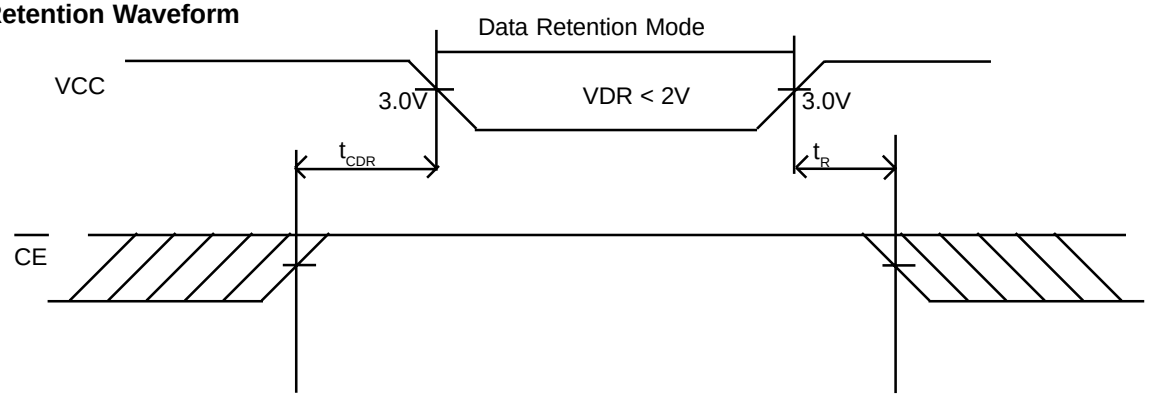
Equivalent To: THEVENIN EQUIVALENT



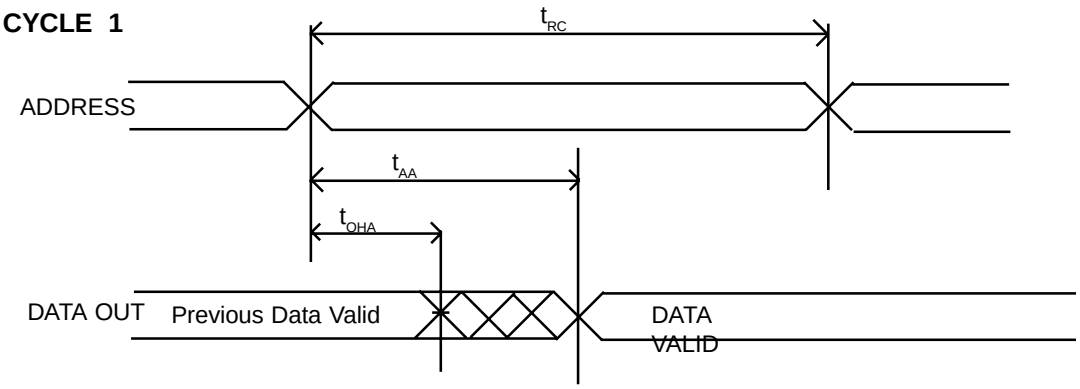
Data Retention Characteristics over the Operating Range

Parameter	Description		Test Conditions	Min.	Typ[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0			V
I_{CCDR}	Data Retention Current	Com'l	No input may exceed V_{CC} + 0.3V			1.7	mA
			$V_{CC} = V_{DR} = 3.0V$, $\overline{CE} \geq V_{CC} - 0.3V$		16	200	µA
		L	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$				
t_{CDR}[5]	Chip Deselect to Data Retention Time			0			ns
t_R	Operation Recovery Time			t_{RC}			ns

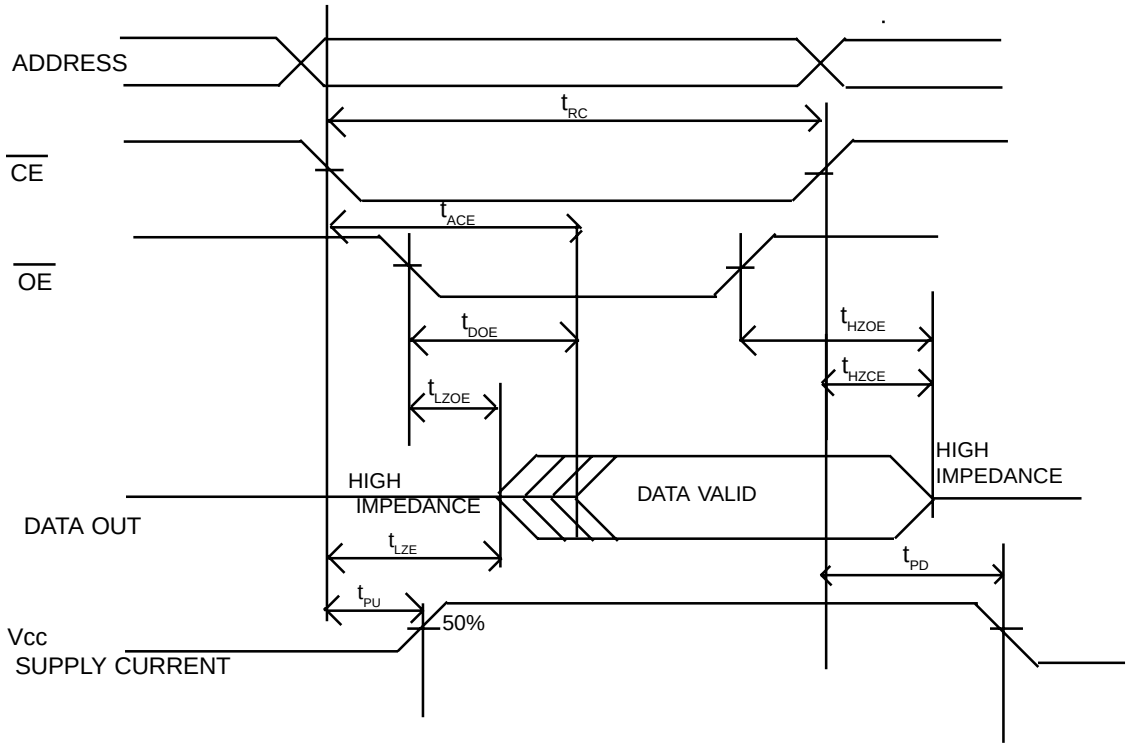
Data Retention Waveform



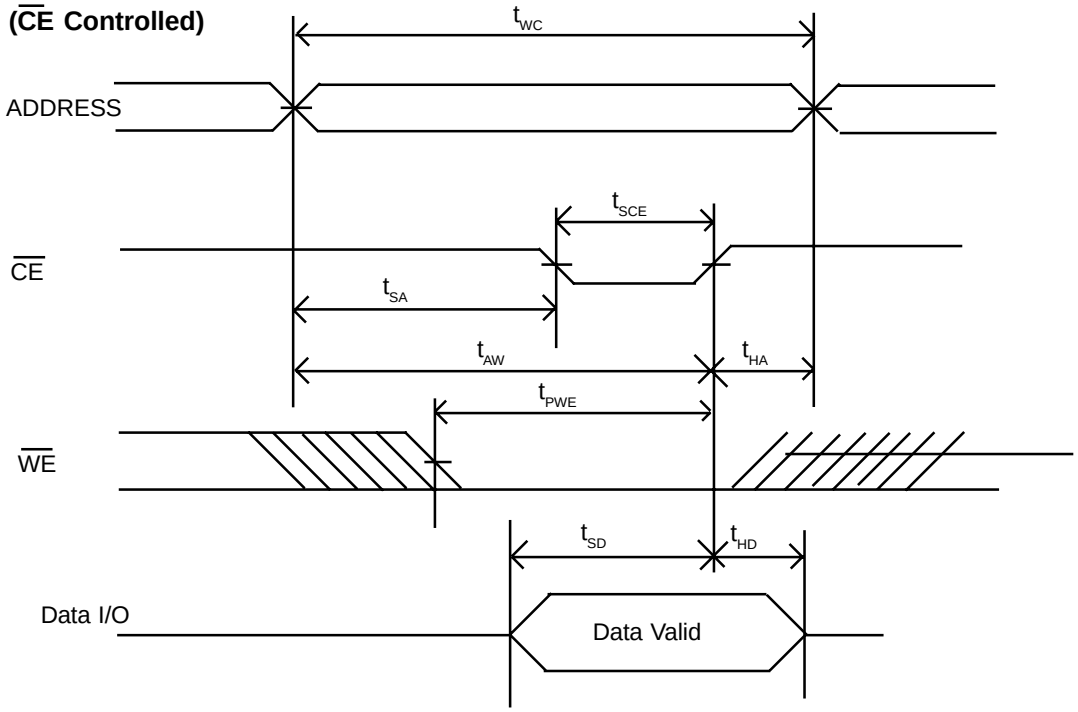
READ CYCLE 1



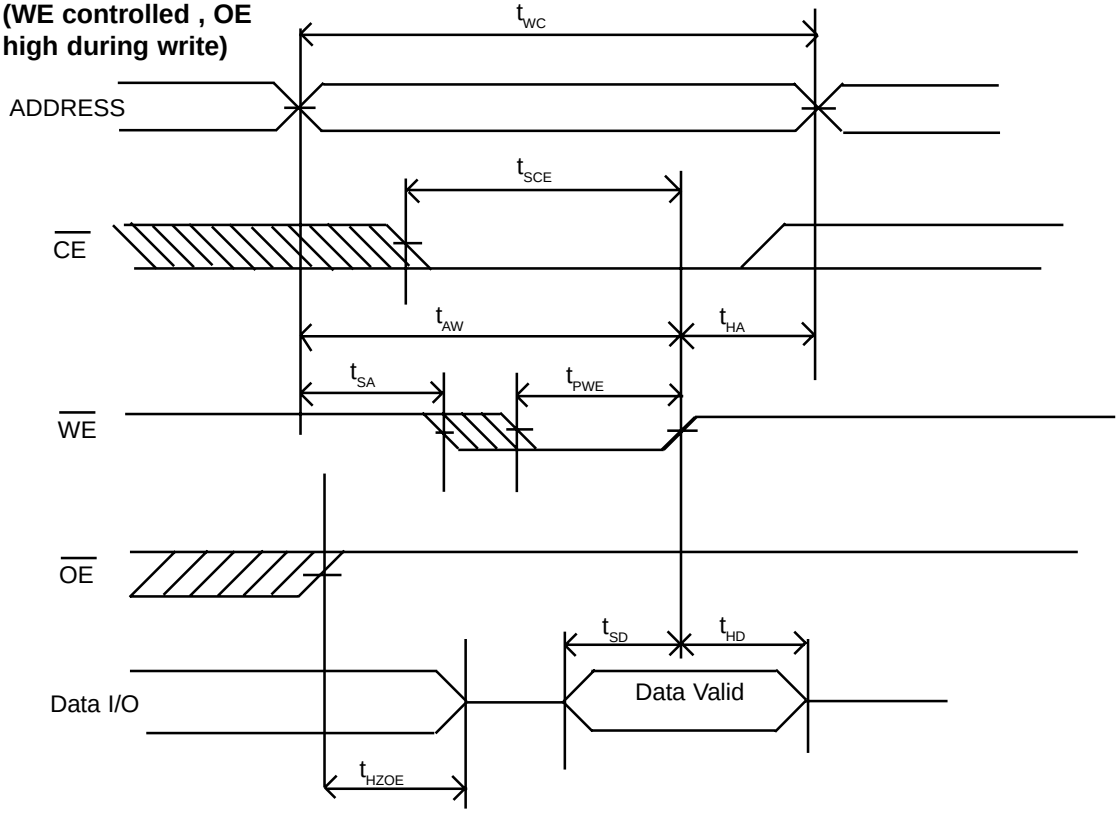
READ CYCLE 2



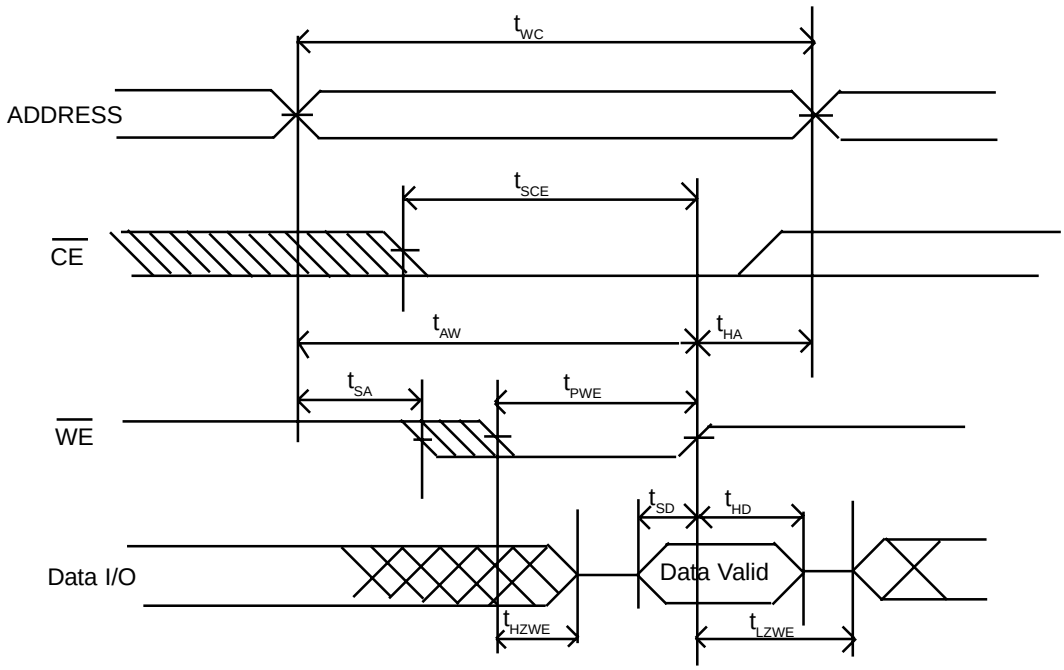
WRITE CYCLE 1
($\overline{CE}$ Controlled)



WRITE CYCLE 2
($\overline{WE}$ controlled , $\overline{OE}$ high during write)



WRITE CYCLE 3
($\overline{WE}$ controlled, $\overline{OE}$ LOW)



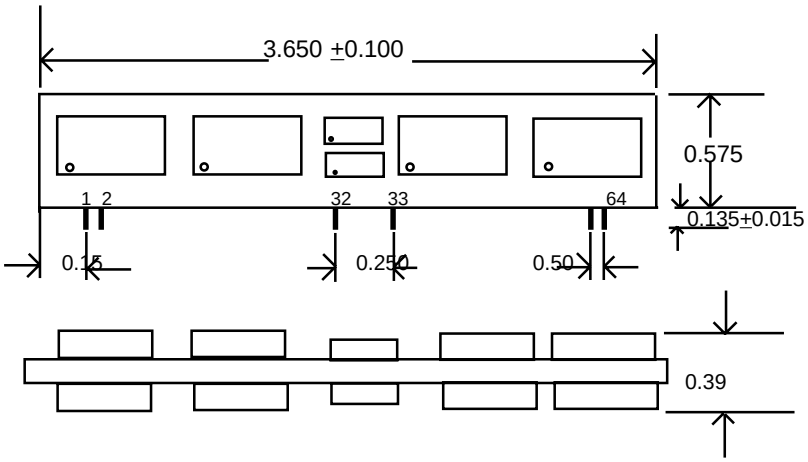
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O0-I/O31	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active(I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed(ns)	Ordering Code	Package Type
45	IMM1841APZ-45C	64- PIN Plastic ZIP Module
35	IMM1841APZ-35C	64- PIN Plastic ZIP Module

C



All dimensions in inches