512K X 8 Ultra Low Power CMOS SRAM

FEATURES

- Wide Vcc operaation voltage : 2.7V-3.6V
- Very low power consumption:
  Vcc = 3.0V 20mA(Max.)write current
  10mA(Max.) CMOS standby current
  1*u*A(Typ.) CMOS standby current
- High speed 70 ns access time.
- Input levels are CMOS compatible.
- Automatic power down when chip is deselected.
- Three state outputs.
- Fully static operation.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with $\overline{CE}$ and $\overline{OE}$ options.

PIN CONFIGURATIONS

TSOP PACKAGE

A11	1	32	$\overline{OE}$
A9	2	31	A10
A8	3	30	$\overline{CE}$
A1	4	29	I/O7
$\overline{WE}$	5	28	I/O6
A17	6	27	I/O5
A15	7	26	I/O4
Vcc	8	25	I/O3
A18	9	24	GND
A16	10	23	I/O2
A14	11	22	I/O1
A12	12	21	I/O0
A7	13	20	A0
A6	14	19	A1
A5	15	18	A2
A4	16	17	A3

PIN NAMES

A0-A18	Address Input
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O0-I/O7	Input/Output
Vcc	Power Supply
Gnd	Ground

DESCRIPTION

The IM624000LL is a high performance,very low power CMOS Static Random Access Memory organized as 524,288 words by 8 bits and operates from an very low range of 2.7V to 3.6V supply voltage.

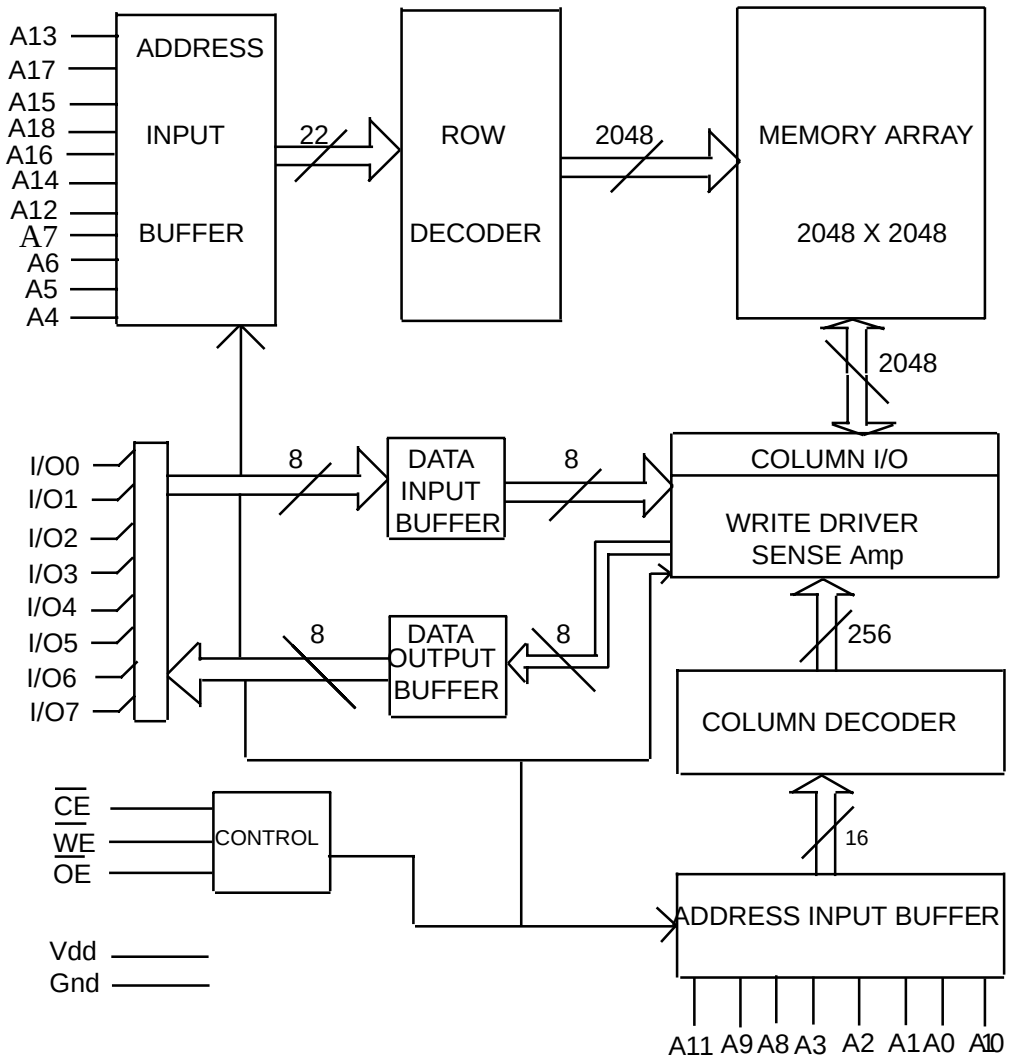
Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.01uA and maximum access time of 70ns in 3V operation.

Easy memory expansion is provided by an active LOW chip enable($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state output drivers.

The IM624000LL has an automatic power down features, reducing the power consumption significantly when chip is deselected.

The IM624000LL is avaible in the JEDEC standard 32 pin Plastic TSOP and STSOP packages.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Terminal Voltage with respesct to GND..... -0.5 to +6.0
Temperature under Bias..... -40 to +125 °C
Storage Temperature ..... -60 to +150 °C
Power Dissipation ..... 1.0 W
DC Output Current..... 20 mA

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O OPERATION	Vcc CURRENT
Not selected	X	H	X	High Z	I_{CCSB},I_{CCSB1}
Output Disable	H	L	H	High Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

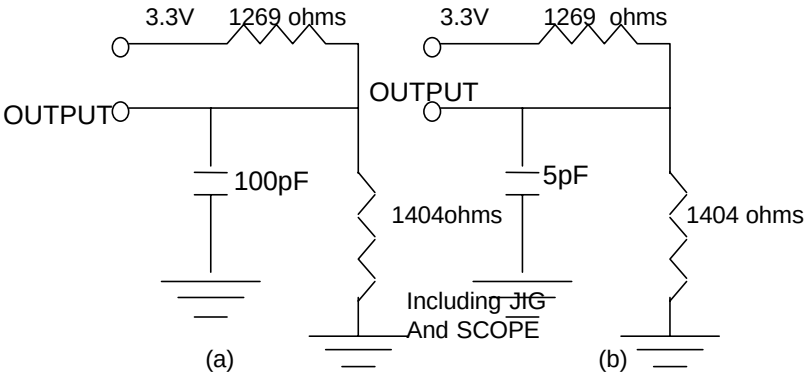
CAPACITANCE (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	VIN = 0V	6	pF
C_{DQ}	Input/Output Capacitance	VI/O = 0V	8	pF

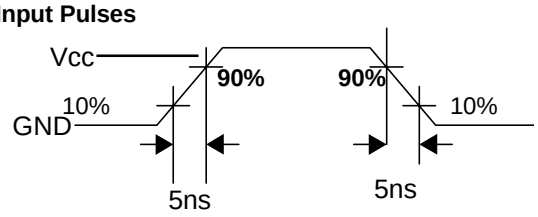
AC TEST CONDITION

Input Pulses Levels Vcc/0V
Input Rise and Fall Times..... 5ns
Input and Output Timing Reference Level..... 0.5 Vcc

AC Test Loads and Waveforms



All Input Pulses



THEVENIN EQUIVALENT

DC ELECTRICAL CHARACTERISTICS(TA=0 TO + 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Guaranted Input Low Voltage	V_{IL}		-0.5		0.3Vcc	V
Guaranteed Input High Voltage	V_{IH}		2.0		Vcc+0.2	V
Input Leakage Current	I_{IL}	Vcc=Max, V_{IN}=0V to Vcc			1	uA
Output Leakage Current	I_{OL}	Vcc=Max,$\overline{CE}$=V_{IH},or $\overline{OE}$=V_{IH} , $V_{I/O}$=0V to Vcc			1	uA
Output Low Voltage	V_{OL}	Vcc=Max, I_{OL} = 2mA			0.4	V
Output High Voltage	V_{OH}	Vcc=Max, I_{OH} =-1mA	2.4			V
Operating Power Supply Current	I_{CC}	$\overline{CE}$=V_{IH} OR $I_{I/O}$=0mA			20	mA
Standby Power Supply Current	I_{CCSB}	$\overline{CE}$=V_{IH} OR $I_{I/O}$=0mA			1	mA
Power Down Supply Current	I_{CCSB1}	$\overline{CE}$>Vcc-0.2V, V_{IH}>Vcc-0.2V or V_{IH} < 0.2V		1	12	uA

AC ELECTRICAL CHARACTERISTICS
READ CYCLE

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_{RC}	Read Cycle Time	70			ns
t_{AA}	Address Access Time			70	ns
t_{ACS}	Chip Select Access Time			70	ns
t_{OE}	Output Enable to Output Valid			40	ns
t_{CLZ}	Chip Select to Output Low Z	10			ns
t_{OLZ}	Chip Enable to Output in Low Z	5			ns
t_{CHZ}	Chip Deselect To Output in High Z	0		30	ns
t_{OHZ}	Output Disable to output in High Z	0		25	ns
t_{OH}	Output Disable to Output Address Change	10			ns

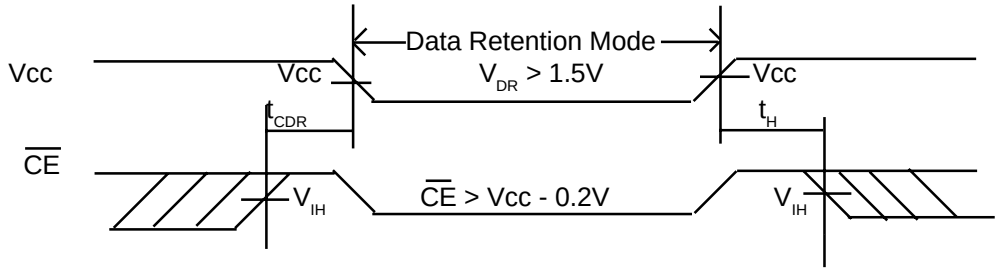
WRITE CYCLE

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
t_{WC}	Write Cycle Time	70			ns
t_{CW}	Chip Select to End of Write	70			ns
t_{AS}	Address Set up Time	0			ns
t_{AW}	Address Valid to End of Write	70			ns
t_{WP}	Write Pulse Width	50			ns
t_{WR}	Write Recovery Time	0			ns
t_{WHZ}	Write to Output in High Z	0		30	ns
t_{DW}	Data to Write Time Overlap	35			ns
t_{DH}	Data Hold From Write Time	0			ns
t_{OHZ}	Output Disable to Output In High Z	0		30	ns
t_{OW}	End of Write to Output Active	5			ns

DATA RETENTION CHARACTERISTICS (TA = 0 to + 70°C)

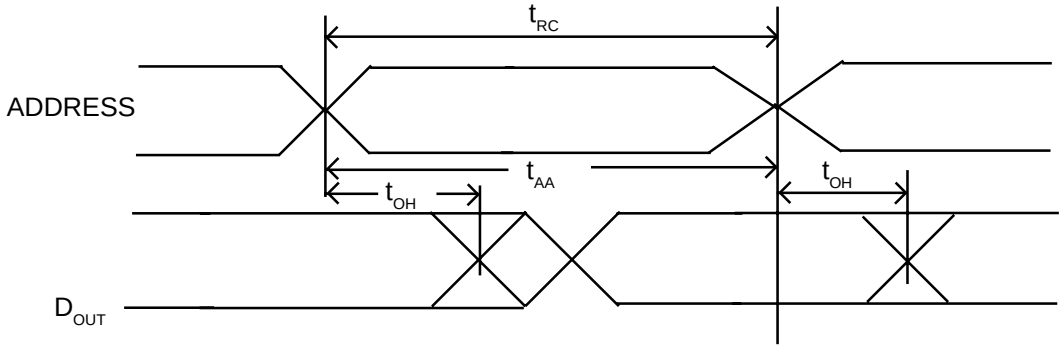
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{DR}	Vcc for Data Retention	CE > Vcc- 0.2V VIN>Vcc-0.2V or VIN<0.2V	1.5			V
I_{CCDR}	Data Retention Current	CE > Vcc- 0.2V VIN>Vcc-0.2V or VIN<0.2V		0.3	8	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t_R	Operation Recovery Time	See Retention Waveform	T_{RC}			ns

LOW Vcc DATA RETENTION WAVEFORM

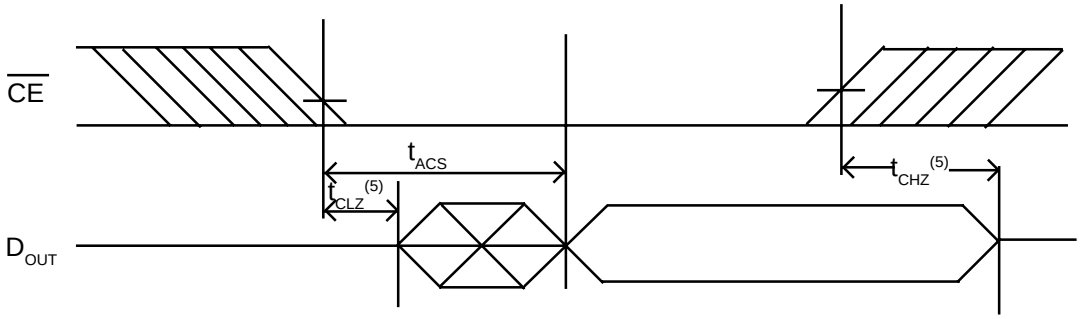


SWITCHING WAVEFORMS (READ CYCLE)

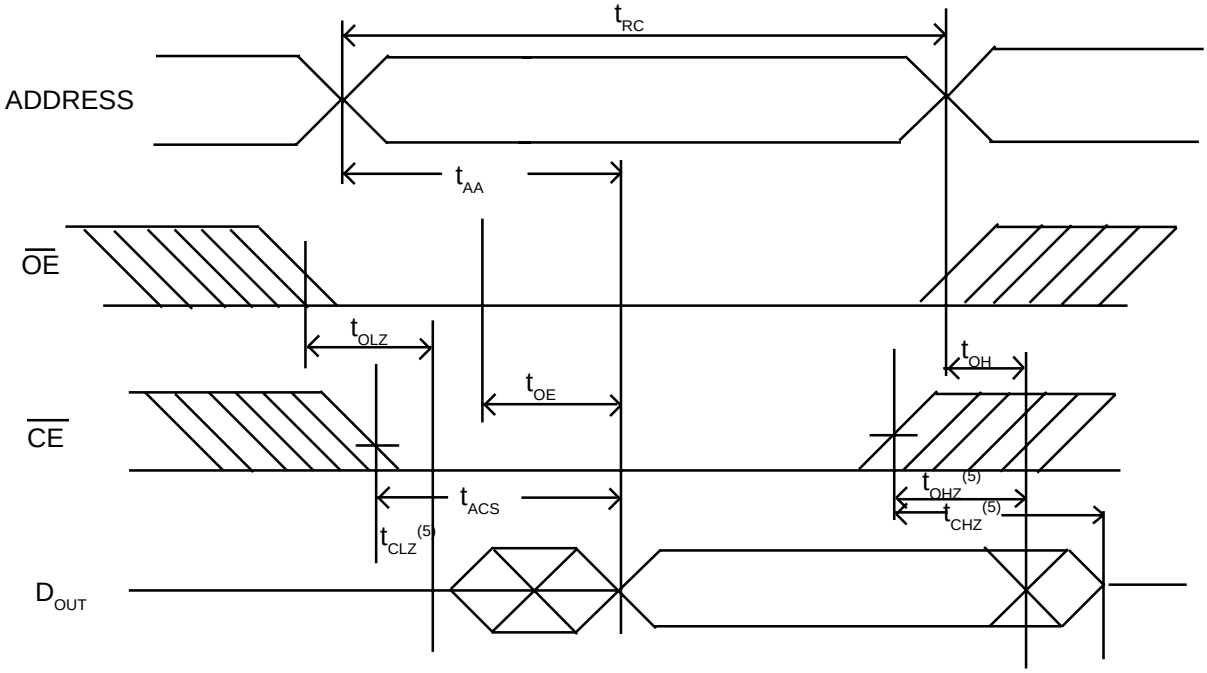
READ CYCLE1



READ CYCLE2



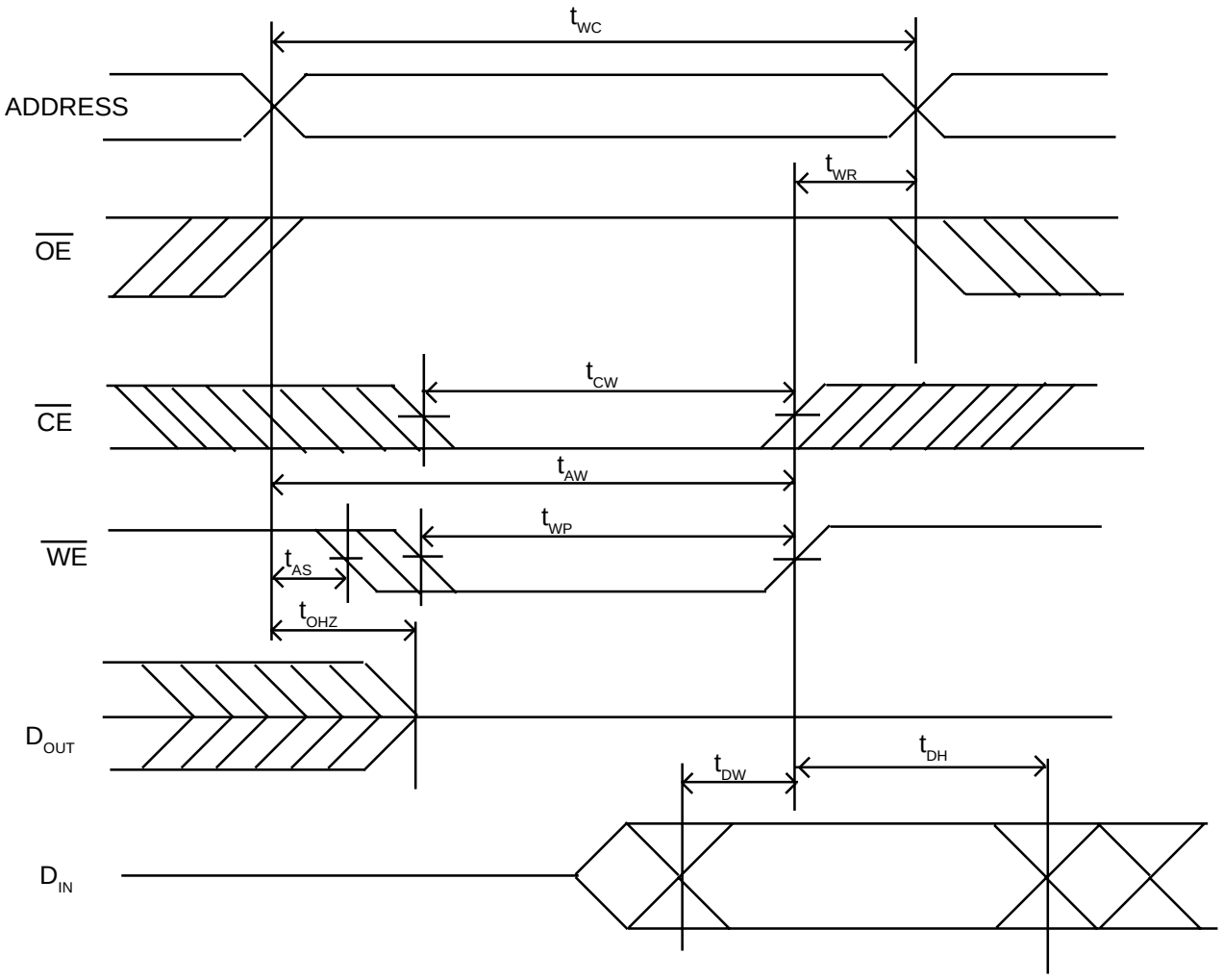
READ CYCLE3



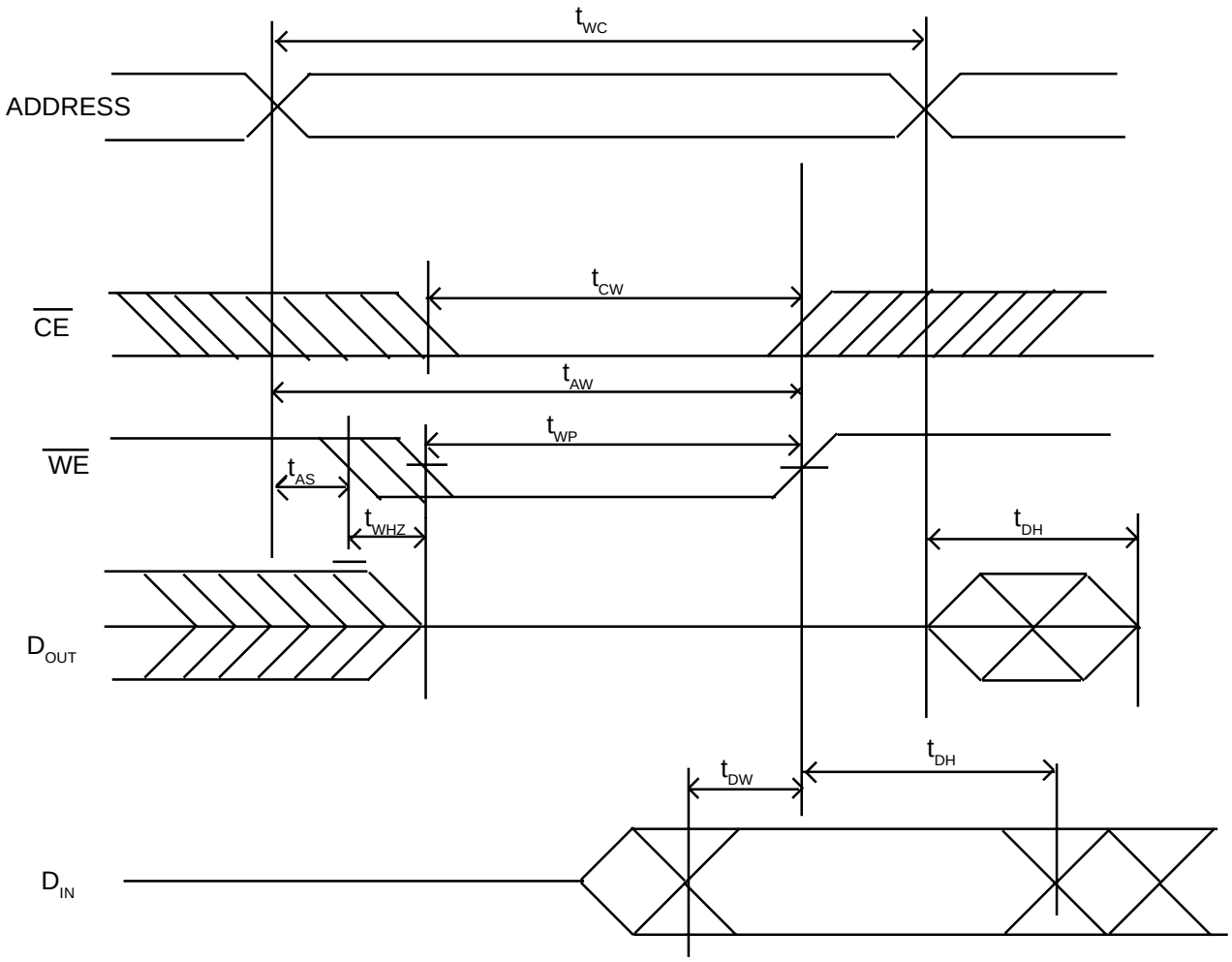
NOTES :
1. WE is high for read Cycle.
2. Device is continously selected when CE = $V_{IL.}$
3. Address valid prior to or coincident with CE transition low.
4. OE =V_{IL}.
5. Transition is measured +500mV from steady state with C_L = 5pF.

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1[1]

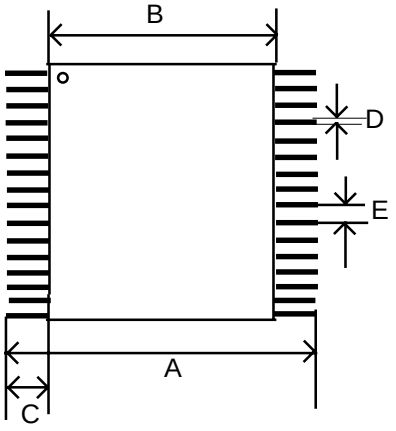


WRITE CYCLE2



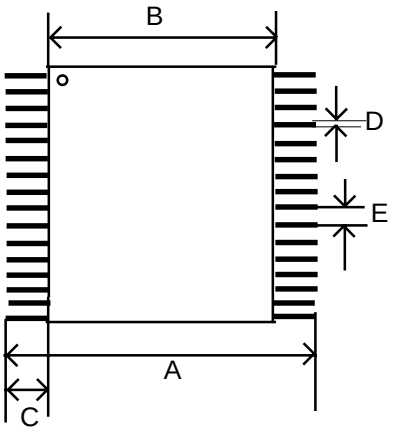
NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be reference to the second transition edge of the signal taht terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE}$ and $\overline{WE}$ going high at the end off write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If th $\overline{CE}$ low transition occurs simultaneously with the WE low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is contiously low($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CE}$ is low during this period,I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied.
9. T_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.
10.D_{OUT} is the read data of next address.

PACKAGE DIAGRAM



TOP VIEW (TSOP - 32)

DIMENSION IN INCHES	MIN.	MAX.
A	0.787	0.795
B	0.465	0.469
C	0.009	0.011
D	0.020	0.024
E	0.0315	0.0319



TOP VIEW (STSOP - 32)

DIMENSION IN INCHES	MIN.	MAX.
A	0.528	0.536
B	0.465	0.469
C	0.009	0.011
D	0.020	0.004
E	0.0315	0.0319